Abstract

WAFER LEVEL PACKAGE INTEGRATION AND METHOD

In a wafer level chip scale package, a wafer level interconnect structure is formed on a dummy substrate with temperatures in excess of 200°C. First semiconductor die are mounted on the wafer level interconnect structure. The wafer level interconnect structure provides a complete electrical interconnect between the semiconductor die and one or more of the solder bumps according to the function of the semiconductor device. A second semiconductor die can be mounted to the first semiconductor die. A first encapsulant is formed over the semiconductor die. A second encapsulant is formed over the first encapsulant. The dummy substrate is removed. A first UBM is formed in electrical contact with the first conductive layer. Solder bumps are made in electrical contact with the first UBM. A second UBM is formed to electrically connect the semiconductor die to the wafer level interconnect structure. (Fig. 3)