

CLAIMS

The invention claimed is:

1. A memory array comprising a plurality of memory cell units; the array comprising multiple elevational levels of wordlines, and planes through each level; the areas of the individual memory cell units along the planes being less than $4F^2$ relative to wordlines, bitlines, and spaces consumed by the memory cell units.
2. The memory array of claim 1 wherein the areas of the individual memory cell units along the planes are $2F^2$ relative to wordlines, bitlines, and spaces consumed by the memory cell units.
3. The memory array of claim 1 wherein the memory cell units comprise phase change material, and are directly between wordlines and bitlines; and wherein the only material directly between the wordlines and bitlines is the phase change material.
4. The memory array of claim 1 comprising:
 - global bitlines extending along a first horizontal direction; the global bitlines comprising a first series at a first elevational level, and a second series at a second elevational level which is different from the first elevational level; the global bitlines of the first series alternating with the global bitlines of the second series;
 - vertical local bitlines extending perpendicularly to the global bitlines;
 - wordlines extending along a second horizontal direction which is perpendicular to the first horizontal direction; the wordlines being stacked in a two-dimensional array comprising vertical columns and horizontal rows; the vertical columns of the wordline array comprising two or more wordlines; the vertical local bitlines extending through the wordline array so that vertical local bitlines are between adjacent vertical columns of the wordline array; and
 - memory cell material between the wordlines and the vertical local bitlines; the memory cell material forming memory cells of the memory cell units, with individual memory cells being uniquely addressed by wordline/global bitline combinations.
5. The memory array of claim 4 wherein the global bitlines of the first series are on an opposite side of the wordlines as the global bitlines of the second series.

6. The memory array of claim 4 wherein the global bitlines of the first series are on a common side of the wordlines as the global bitlines of the second series.

7. A memory array, comprising:
global bitlines extending along a first horizontal direction; the global bitlines comprising a first series at a first elevational level, and a second series at a second elevational level which is different from the first elevational level; the global bitlines of the first series alternating with the global bitlines of the second series;
vertical local bitlines extending perpendicularly to the global bitlines;
wordlines extending along a second horizontal direction which is perpendicular to the first horizontal direction; the wordlines being stacked in a two-dimensional array comprising vertical columns and horizontal rows; the vertical columns of the wordline array comprising two or more wordlines; the vertical local bitlines extending through the wordline array so that vertical local bitlines are between adjacent vertical columns of the wordline array; and
memory cell material directly between the wordlines and the vertical local bitlines; the memory cell material forming a plurality of memory cells uniquely addressed by wordline/global bitline combinations.

8. The memory array of claim 7 wherein the global bitlines of the first series are on an opposite side of the wordlines as the global bitlines of the second series.

9. The memory array of claim 8 wherein the global bitlines of the first series are directly over the global bitlines of the second series.

10. The memory array of claim 8 wherein the global bitlines of the first series are not directly over the global bitlines of the second series.

11. The memory array of claim 7 wherein the global bitlines of the first series are on a common side of the wordlines as the global bitlines of the second series.

12. The memory array of claim 7 wherein the memory cell material is the only material directly between the wordlines and the vertical local bitlines.

13. The memory array of claim 12 wherein the memory cell material is a phase change material.

14. The memory array of claim 7 wherein non-linear access devices are directly between the wordlines and the bitlines together with the memory cell material.

15. The memory array of claim 7 wherein ovonic threshold switches are directly between the wordlines and the bitlines together with the memory cell material.

16. The memory array of claim 7 wherein non-linear access devices are directly between the global bitlines and the vertical local bitlines.

17. The memory array of claim 7 wherein ovonic threshold switches are directly between the global bitlines and the vertical local bitlines.

18. A memory array, comprising:
a plurality of bitline combs; the individual combs comprising a horizontally-extending global bitline and a plurality of vertically-extending bitline pillars electrically connected to the global bitline; the bitline combs comprising a first series and a second series; the second series being vertically offset relative to the first series; the bitline combs of the first series alternating with the bitline combs of the second series to form a staggered arrangement of the vertically-extending bitline pillars; the horizontally-extending global bitlines being parallel to one another;
wordlines extending orthogonally to the global bitlines; the wordlines being stacked in a two-dimensional array comprising vertical columns and horizontal rows; the vertical columns of the wordline array comprising two or more wordlines; the bitline pillars extending through the wordline array so that bitline pillars are between adjacent vertical columns of the wordline array; and
memory cell material directly between the wordlines and the bitline pillars; the memory cell material forming a plurality of memory cells uniquely addressed by wordline/global bitline combinations.

19. The memory array of claim 18 wherein the vertical pillars of the first series of bitline combs extend downwardly from the global bitlines, and the vertical pillars of the second series of bitline combs extend upwardly from the global bitlines.
20. The memory array of claim 19 wherein individual global bitlines of the first series of bitline combs are directly over individual global bitlines of the second series of bitline combs.
21. The memory array of claim 19 wherein individual global bitlines of the first series of bitline combs are offset from being directly over individual global bitlines of the second series of bitline combs.
22. The memory array of claim 18 wherein the vertical pillars of the first and second series of bitline combs extend upwardly from the global bitlines.
23. The memory array of claim 18 wherein the vertical pillars of the bitline combs are ohmically connected to the global bitlines.
24. The memory array of claim 18 wherein the vertical pillars of the bitline combs are connected to the global bitlines through access devices that respond non-linearly to increasing voltage.
25. The memory array of claim 18 wherein the vertical pillars of the bitline combs are connected to the global bitlines through ovonic threshold switches.
26. The memory array of claim 18 wherein the memory cell material of multiple memory cells associated with an individual vertical pillar is non-contiguous across a surface of the vertical pillar.
27. The memory array of claim 26 wherein the memory cell material is phase change material.

28. The memory array of claim 18 wherein the memory cell material of multiple memory cells associated with an individual vertical pillar is contiguous across a surface of the vertical pillar.

29. The memory array of claim 28 wherein the memory cell material is phase change material.

CLAIMS:

1. A memory array, comprising:

global bitlines extending along a first horizontal direction; the global bitlines comprising a first series at a first elevational level, and a second series at a second elevational level which is different from the first elevational level; the global bitlines of the first series alternating with the global bitlines of the second series;

vertical local bitlines extending perpendicularly to the global bitlines;

wordlines extending along a second horizontal direction which is perpendicular to the first horizontal direction; the wordlines being stacked in a two-dimensional array comprising vertical columns and horizontal rows; the vertical columns of the wordline array comprising two or more wordlines; the vertical local bitlines extending through the wordline array so that vertical local bitlines are between adjacent vertical columns of the wordline array; and memory cell material directly between the wordlines and the vertical local bitlines; the memory cell material forming a plurality of memory cells uniquely addressed by wordline/global bitline combinations.

2. The memory array of claim 1 wherein the global bitlines of the first series are on an opposite side of the wordlines as the global bitlines of the second series.

3. The memory array of claim 2 wherein the global bitlines of the first series are directly over the global bitlines of the second series.

4. The memory array of claim 2 wherein the global bitlines of the first series are not directly over the global bitlines of the second series.

5. The memory array of claim 1 wherein the global bitlines of the first series are on a common side of the wordlines as the global bitlines of the second series.

6. The memory array of claim 1 wherein the memory cell material is the only material directly between the wordlines and the vertical local bitlines.

7. The memory array of claim 6 wherein the memory cell material is a phase change material.

8. The memory array of claim 1 wherein non-linear access devices are directly between the wordlines and the bitlines together with the memory cell material.

9. The memory array of claim 1 wherein ovonic threshold switches are directly between the wordlines and the bitlines together with the memory cell material.

10. The memory array of claim 1 wherein non-linear access devices are directly between the global bitlines and the vertical local bitlines.

11. The memory array of claim 1 wherein ovonic threshold switches are directly between the global bitlines and the vertical local bitlines.

12. The memory array of claim 1 wherein the global bitlines of the first series are on an opposite side of the wordlines as the global bitlines of the second series; wherein the memory cell material is the only material directly between the wordlines and the vertical local bitlines; and wherein the memory cell material is phase change material.