

METHOD OF FORMING SHALLOW TRENCH ISOLATION STRUCTURES

Technical Field of the Invention

The present invention relates to Shallow Trench Isolation (STI) structures and a
5 method for creating them, for example in Logic and Local Interconnect Layer (LIL)
Devices.

Background of the Invention

Shallow Trench Isolation (STI) is used as Complementary Metal-Oxide
10 Semiconductor (CMOS) technologies are scaled down below the 0.25 μm generation
due to the inevitable requirements to shrink design rules while still maintaining
sufficient oxide thickness for isolation.

STI acts to isolate transistors in an active substrate. It achieves scaling and
isolation between transistors at the expense of process complexity relative to its Local
15 Oxidation of Silicon (LOCOS) predecessor. STI significantly shrinks the area needed to
isolate transistors while offering latch-up immunity, smaller channel width
encroachment and better planarity. STI is also highly scalable; the trench-fill
capabilities being the only major challenge to scaling. However, STI requires a
planarization procedure that increases the process complexity. Since STI electrically
20 isolates active device regions, it eliminates problems traditionally associated with
LOCOS, while enabling an active area with higher density. Additionally, the flatness of
the resulting wafer enables more precise pattern definition for subsequent layers.

As pitch lengths continue to be scaled down, the distance between transistor
active areas and STI side walls also narrows. Therefore critical regions such as
25 junctions continue to approach the more highly stressed regions at the side wall
interface. The abrupt transient edge region and the stress between the channel and
the isolation region have an undesirable influence on electrical performance and
reliability.

Several steps within a conventional manufacturing method for forming STI are
30 shown in the schematic cross sectional views in Figures 1A to 1H.

Prior to Figure 1A, a thin layer of pad silicon oxide is first grown on a clean
silicon substrate. A thicker Silicon Nitride layer is then deposited by Low Pressure
Chemical Vapour Deposition (CVD), on top of the oxide layer. A patterned active area
resist is formed atop the Silicon Nitride layer. The nitride layer is subsequently
35 patterned and a trench is etched through the oxide layer into the silicon substrate,
according to the pattern in the active area resist. The depth of the trench depends on

the etch process and technology. Trenches of arbitrary depths can be fabricated by varying the etch time. Deeper trenches increase latch-up immunity, decrease junction capacitance, and decrease junction leakage. In practice, the aspect ratio of the trench (ratio of height to width) is limited by the trench fill capability of the oxide. The trench is
5 implanted to increase field threshold voltage and growth of linear oxide for passivation and smoothing. After resist stripping (resist not shown), the trench side walls are passivated so that the walls become a thin layer of thermal oxide. The Trench is subsequently planarized using Chemical-Mechanical Polishing (CMP), stopping part way through the nitride layer.

10 Figure 1A represents the process after CMP. The silicon substrate 102 has a trench 104 within it. The trench walls 106 are a thin layer of thermal oxide. A plug of silicon dioxide 108 fills the trench. The top surface of the silicon substrate 102 is still covered by a thin pad oxide layer 110.

A wet etching process is used to remove the pad oxide layer 110. During this
15 process, recess areas 112 are formed at the top edges of the trench 104 and plug 108, as shown in Figure 1B.

A layer of sacrificial oxide (not shown) is then grown on top of the substrate 102 and plug 108. This is followed by steps such as well implant and Vth implant. The sacrificial oxide layer is then removed by wet etching, leaving the trench structure
20 generally as shown in Figure 1B again.

The growth of gate oxide 120 and the deposit of poly silicon 122 follow subsequently. These are patterned and the excess poly silicon removed in a poly etch process, as shown in Figure 1C (the gate oxide 120 being shown much thicker relative to the poly silicon 122, than it is in fact in practice).

25 As is shown in Figure 1B, the pad oxide etching step creates shallow recesses 118 between the oxide 108 in the trench 104 and the substrate 102. These recesses persist in the further steps and during poly silicon deposit are filled with poly silicon. However, the poly silicon etch is incapable of removing all the poly silicon from the recesses 112. As a result, the trench 104 may be left with a stringer of poly silicon 124.
30 This is known as trench oxide grooving. It can cause poly-gate current leakage and other problems leading to circuit failure or poor performance.

The size of these recesses 112 and therefore the number of stringers varies according to the density of the features, that is dense versus isolated. Thus, for example in flash memories, which use STIs, the active areas are more dense and thus
35 suffer from greater residue. Additionally, the flash part of a flash memory (as opposed to the logic part) goes through fewer cleaning cycles than the logic part and thus the

step height of the trenches (the level of the trench oxide 108 above the silicon substrate 102) remains greater. Thus residue is more likely in such areas and any residue is less likely to be removed.

A further problem results during later processing, from the addition of a local interconnect layer (LIL), and shown with reference to Figure 2. An oxide or nitride spacer 130 is provided on either side of the poly structures 122 on the silicon substrate 102. An undoped inter layer dielectric (ILD) 132 is added as is an additional oxide (e.g. BPSG or HDP) inter layer dielectric (ILD) 134. This top ILD 134 is reduced to an appropriate level by CMP. Contacts are then opened up by contact etching. The LIL metal is then deposited to form local interconnect layer slits 136 and holes 138. However, during contact etching, the contact etch eats even further into the oxide 108 in the trenches, resulting in abnormal contact between the LIL and the STI. This abnormal contact can also result in IDDQ failure. Other possible failure includes Source and Drain (S/D) leakage current and short circuit between adjacent transistors.

Published US Patent No. 6,277,710 relates to a method of forming STIs, in which the problem of trench oxide grooving due to etch stop etching is recognised. The problem is addressed by forming a polysilicon layer between the pad oxide and silicon nitride layers and an extended liner oxidation layer to form a protective oxidation overlying the polysilicon and pad oxide layers. This requires some changes in the circuit design and increases the complexity and cost of the process.

Summary of the Invention

The present invention relates to a new process for providing Shallow Trench Isolation (STI) structures which overcome or at least partially alleviate at least some of the problems with the prior art.

According to a first aspect of the present invention, there is provided a method for use during the formation of shallow trench isolation structures, the method using a structure comprising: a substrate having a trench therein, a first oxide layer on the substrate and an oxide structure in the trench, with the top of the oxide structure having at least one recess therein, the method comprising the steps of:

- depositing a spacer layer on top of the first oxide layer and trench oxide structure, including within said at least one recess;

- removing the spacer layer, although leaving some of the spacer layer in said at least one recess as remnant spacer layer;

- removing the first oxide layer; and

3a

wherein at least a portion of the trench oxide structure remains substantially underneath the remnant spacer layer.

According to another aspect of the present invention, there is provided a

method of forming shallow trench isolation structures comprising the method of the first aspect above and, prior to said depositing step, the steps of:

providing a second oxide layer on said substrate and a nitride layer on the second oxide layer;

5 forming a trench through said second oxide layer, said nitride layer and into said substrate;

oxidising the walls of said trench;

filling the trench with said oxide structure; and

removing the nitride layer.

10 In either above aspect, there may be provided, after the step of removing the first oxide layer, the steps of:

providing a gate oxide layer on the substrate, the trench oxide structure and the remnant spacer layer;

providing a poly-silicon layer on the gate oxide layer; and

15 patterning the poly-silicon and gate oxide layers.

The spacer layer and the first oxide layer are preferably etched away together. The spacer layer is preferably a layer of a nitride of silicon, for instance silicon nitride or silicon oxi-nitride.

The invention also includes a method of making a flash memory, including any
20 of the above methods. Another aspect includes a semiconductor structure including a structure produced according to any of the above methods.

According to a further aspect of the present invention, there is provided a shallow trench isolation structure comprising:

a substrate;

25 a trench in the substrate;

an oxide structure in the trench;

a gate oxide and poly-silicon structure on the substrate; and

spacer material on upper surfaces of the trench oxide structure.

Preferably the spacer material is a nitride of silicon, for instance silicon nitride
30 or silicon oxi-nitride.

A further aspect of the invention provides a flash memory including a semiconductor structure above or a plurality of shallow trench isolation structures, ones of which are as above.

Thus, the invention provides the possibility, when forming Shallow Trench
35 Isolation (STI) structures, for example in Local Interconnect Layer (LIL) devices, of preventing deep recess areas at the top edges of the trenches, by depositing silicon

nitride onto the oxide in the trenches before the sacrificial oxide layer is removed.

Brief Description of the drawings

The invention will be further described by way of non-limitative example, with
5 reference to the accompanying drawings, in which:

Figures 1A – 1C are schematic drawings of process steps involved in a conventional method of forming Shallow Trench Isolation structures;

Figure 2 is a schematic drawing indicating showing a prior art STI structure in an LIL.

10 Figures 3A to 3C are schematic drawings of process steps involved in a method of the invention of forming STI structures according to an embodiment.

Detailed Description

The present invention builds on many of the steps in the prior art, in particular
15 Figure 1A and the process preceding it. The earlier description of that process is hereby incorporated by reference into the description of the invention.

Figures 3A to 3C are schematic drawings relating to a specific process embodying the present invention. This embodiment follows the prior art including the wet etching step that results in a structure schematically shown in Figure 1B. A silicon
20 substrate 202 has a trench 204. The walls of the trench are lined with a liner and it contains trench oxide 208. Recesses 212 are present between the edges of the trench and the trench oxide 208. As before, the structure of Figure 1B is further processed, growing a layer of sacrificial oxide 214 on top of the substrate 202 and trench oxide 208 with such steps as well implant and Vth implant. The sacrificial oxide layer 214
25 becomes indistinguishable from the trench oxide 208 already in the trench.

However, as is shown in Figure 3A, rather than simply removing the sacrificial oxide layer 214, a further silicon nitride (or silicon oxi-nitride) layer 216 is deposited on top of the sacrificial oxide layer 214 by Low Pressure Chemical Vapour Deposition (LPCVD). Thus the sacrificial oxide layer 214 is covered by the silicon nitride layer
30 216, including in the recesses 212.

This further silicon nitride layer 216 is subsequently blanket etched to remove it, with the end point on the sacrificial oxide. However, the blanket etch fails to remove all the silicon nitride from within the recesses 212.

A wet etch is then used to remove the sacrificial oxide layer 214. However,
35 silicon nitride is a good etch stopping material. Where it has not been removed, that is in the trenches, it acts as a spacer between the etching chemicals and the silicon

dioxide 208 in the trench, thus preventing the recesses in the trench oxide being made deeper. The resulting structure is shown in Figure 3B, with remnant silicon nitride 218 in the recesses.

5 The growth of gate oxide 220 and the deposit of poly silicon 222 follow subsequently. These are patterned, as shown in Figure 3C. The resulting structure differs significantly from the prior art in that there is no stringer of poly silicon remaining in the top of the trench, just silicon nitride remnants 218.

10 The STI structures so produced are further processed into other semiconductor structures, with particular use with local-interconnect layers (LILs) and in flash memories.

The results of this embodiment of the present invention include that

The recess depth is reduced, due to the nitride acting as a spacer in the recess areas. The nitride that fills up the recess areas preventing any poly residue.

15 There will be no poly or oxide residue that will cause the Source and Drain leakage (S/D) failure. Thus, in this regard, Source and Drain leakage failure will be minimised.

20 The contact etch is prevented from further recessing the trench due to the continued presence of the silicon nitride remnants, resulting in IDDQ failures being reduced.

25 A single embodiment of the present invention has been described, relating to a specific method of making STI structures. However, the additional spacer layer of the invention can find uses in other methods of constructing STI structures. For instance the spacer would also remain after relevant etching if the recesses were in the form of corners between adjacent surfaces. The aim is to reduce destruction of the trench contents, for instance by delaying the time to contact between the etch chemicals and the trench contents, especially at the point of contact between the trench walls and the trench contents.

CLAIMS

1. A method for use during the formation of shallow trench isolation structures, the method using a structure comprising: a substrate having a trench therein, a first oxide layer on the substrate and an oxide structure in the trench, with the top of the oxide structure having at least one recess therein, the method comprising the steps of:
 - depositing a spacer layer on top of the first oxide layer and trench oxide structure, including within said at least one recess;
 - removing the spacer layer, although leaving some of the spacer layer in said at least one recess as remnant spacer layer;
 - removing the first oxide layer; and
 - wherein at least a portion of the trench oxide structure remains substantially underneath the remnant spacer layer.
2. A method of forming shallow trench isolation structures comprising the method of claim 1 and, prior to said depositing step, the steps of:
 - providing a second oxide layer on said substrate and a nitride layer on the second oxide layer;
 - forming said trench through said second oxide layer and said nitride layer and into said substrate;
 - oxidising the walls of said trench;
 - filling the trench with said oxide structure; and
 - removing the nitride layer.
3. A method according to claim 1 or 2, further comprising, after the step of removing the first oxide layer, the steps of:
 - providing a gate oxide layer on the substrate, the trench oxide structure and the remnant spacer layer;
 - providing a poly-silicon layer on the gate oxide layer; and
 - patterning the poly-silicon and gate oxide layers.
4. A method as claimed in claim 3, wherein the remnant spacer layers in the recesses act as a spacer between the trench oxide structure and etching chemicals used in the patterning of the poly-silicon and gate oxide layers to prevent the recesses in the trench oxide structure from being made deeper.

5. A method according to any one of the preceding claims, wherein the spacer layer and the first oxide layer are removed separately by etching.
6. A method according to any one of the preceding claims, wherein the spacer layer is a layer of a nitride of silicon.
7. A method according to any one of the preceding claims, wherein the trench oxide structure and first oxide layer are silicon dioxide and the substrate is silicon.
8. A method according to any one of the preceding claims, wherein the first oxide layer is directly on the substrate.
9. A method of making a semiconductor device comprising:
a method according to any one of the preceding claims; and
forming local interconnect layers on the substrate.
10. A method of making a flash memory, including the method of any one of the preceding claims.
11. A semiconductor structure including a structure produced according to the method of any one of claims 1 to 8.
12. A shallow trench isolation structure comprising:
a substrate;
a trench in the substrate;
an oxide structure in the trench;
a gate oxide and poly-silicon structure on the substrate; and
spacer material on at least one upper surface of the trench oxide structure.
13. A shallow trench isolation structure according to claim 11, wherein the spacer material is a nitride of silicon.
14. A flash memory including a semiconductor structure according to claim 10 or a plurality of shallow trench isolation structures, ones of which are as defined in claim 11 or 12.

15. A shallow trench isolation structure constructed and arranged substantially as hereinbefore described with reference to and as illustrated in Figures 3A to 3C of the accompanying drawings.

16. A method for use during the formation of shallow trench isolation structures, substantially as hereinbefore described with reference to and as illustrated in Figures 3A to 3C of the accompanying drawings.