

SELECTIVE PARTITIONING OF VIA STRUCTURES IN PRINTED CIRCUIT BOARDS

TECHNICAL FIELD

5 Embodiments herein relates to a method for selective partitioning of via structures in printed circuit boards.

BACKGROUND

To allow signals to travel between different conductive layers in a multilayer printed circuit board PCB, plated via
10 structures are used. Often the plating is done to the whole inner surface of the via, but the plating can also be done selectively at certain parts within the same via to allow for more efficient use of conductive layers in the PCB.

Figures 1A and 1B illustrate two examples of selective
15 partitioning of via structures known patent application US 2006/199390 A1.

Figure 1A illustrates a multilayer PCB 100 with a plurality of conductive layers 101-106 sandwiched with a plurality of dielectric layers 111-113,121-122. Figure 1A also
20 illustrates a via structure 140 in the PCB 100. The via 140 comprises two plated electrically conductive portions 141 and 142 and between the two plated portions is an electrically isolating portion 145.

Figure 1B illustrates another multilayer PCB 200 with a
25 plurality of conductive layers 151-156 sandwiched with a plurality of dielectric layers 161-163,171-172 and a via structure 190. The via 190 also comprises two plated conductive portions 191 and 192 but between the two plated portions is an electrically isolating portion 195 that is
30 larger than in Figure 1A.

The electrically isolated portions 145 and 195 are produced by using plating resist layers 143 and 193 of different thickness.

5 A disadvantage with using a relatively thin plating resist layer 143 as in Figure 1A is that the distance between the two plated portions 141 and 142 may be insufficient in order to achieve a valid isolation distance, especially for high voltage electronics.

10 A disadvantage with a thick plating resist layer 193 as in Figure 1B is that the manufacturing process is more work intensive as the PCB need a number of additional preparation steps such as milling open portions in the dielectric layers before the thick plating resist layer 193 can be applied.

15 US patent application 2012/234587 discloses an embodiment of a method for partitioning a via in a multilayer printed circuit comprising conductive layers and insulating layers as to produce an electrically isolating portion between two electrically conducting portions within the via (Figure 16). The size of the electrically isolating portion in the via is
20 limited to the thickness of the isolating layer.

Japanese patent application JP 2002 026522, US patent application 2003/121699 and US patent 6,541,712 disclose similar methods where again the size of the resulting electrically isolating portion in the via is limited to the
25 thickness of a single plating resist layer or isolating layer.

SUMMARY

With this background it is the object to obviate at least some of the disadvantages mentioned above.

30 The object is achieved by an improved method to partition a via structure by using two plating resist layers in the PCB

separated by at least one dielectric layer as to produce an electrically isolating portion of the via structure between two electrically conducting portions of said via structure.

One advantage of using the improved method is that only one
5 drilling operation is needed when drilling the holes for the via. There is no need for high tolerance back drilling or sequential laminations with separate drilling for each sequential configuration.

Another advantage is that using two (or more) plating resist
10 layers an arbitrary size of the conductive portions and the isolating/non-conductive portions of the via can be created allowing for more flexible circuit design.

The method allows to create non-conductive portions of different sizes in the via using the same type and thickness
15 of the plating resist layers. This has the additional advantage of simplifying the manufacturing process and there is no need to keep plating resist layers with different thickness in stock.

The invention embodiments will now be described in more
20 detail and with preferred embodiments and referring to accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures **1A** and **1B** are block diagrams illustrating partitioned via structures.

25 Figures **2A**, **2B** and **3** are block diagrams illustrating a PCB and the method steps for producing an improved via structure within said PCB.

Figures **4** and **5** are block diagrams illustrating other embodiments of improved via structures.

Figure 6 is a flow chart illustrating the method steps for producing the improved via structures.

DETAILED DESCRIPTION

5 An embodiment of a method for producing an improved via structure is illustrated in Figures 2A, 2B, 3 and 6. Figure 2A illustrates four steps of the method applied on one and the same PCB 200. The PCB 200 has a plurality of conductive layers (normally copper layers) 201-208 and sandwiched between the copper layers 201-208 are dielectric layers as
10 prepreg layers 211-214 and laminate layers 221-223 respectively. Prepreg which is an abbreviation for pre impregnated is a fiber weave impregnated with a resin bonding agent.

Before lamination, islands of at least two plating resist
15 layers 231-234 are added at predetermined places on the copper layers 203-206 on the laminates 221-223 in step 1 (as shown in Figure 6).

The plating resist layer can also be added directly on the laminate (not shown in Figure 2A). In the lamination
20 process, the islands of the plating resist layers are embedded in the prepreg layers 212 and 213 as seen in step 2 (as shown in Figure 6). In step 3 (as shown in Figure 6) a through hole 240 is drilled in the PCB 200 through the copper layers 201-208 and the plating resist layers 231-234.
25 In step 4 (as shown in Figure 6) and before plating, a thin layer 251 of chemical copper, is added to the inside of through hole 240 by placing the PCB 200 in a seed catalyzing bath. This thin layer 251 adheres to all inner parts of the through hole 240 except for the plating resist layers 231-
30 234 as seen in positions 252 and 253 in Figure 2B. In step 5 (as shown in Figure 3 and 6) the PCB is placed in an electrolytic copper plating bath. As the portion 254 of the thin layer 251 of chemical copper located between the two

plating resist layers 231 and 232 and the portion 255 located between the two plating resist layers 233 and 234 are electrically isolated from the other conductive layers no copper is plated on these portions during the electrolytic plating process. After copper plating of the through hole 240, the thin copper layer that remains on portions 254 and 255 is removed by using micro etch (or an equivalent post processing operation). The resulting via structure is seen in step 6 (as shown in Figure 6) with three conductive portions 301-303 and two non-conductive portions 254 and 255 where the non-conductive portions 254 and 255 have a significant larger isolation distance than when using one thin plating resist layer only.

In the embodiment illustrated in Figures 2A, 2B and 3 the plating resist layers 231 and 232 are embedded in the same prepreg layer 212. The improved method is not limited to this configuration. Figure 4 illustrates an embodiment of a PCB 400 having a plurality of copper layers 401-407 and dielectric layers 411-413 and 421-423. In the PCB 400 the plating resist layers 431 and 432 are embedded in different prepreg layers 412 and 413 apart from each other and where the non-conductive portion 451 becomes larger.

The improved method is not limited to producing through hole vias only but can also be applied to blind vias or vias with different diameters within the same via structure. An example of the latter is illustrated in Figure 5. In Figure 5, a via structure in a PCB 500 is divided into two via portions 530, 535 with different diameters. The narrower via portion 530 is electrically isolated from the broader via portion 535 by using two plating resist layers 541, 542 in the same manner as described above. The broader via portion 535 is produced by an additional step of back drilling with a larger drill before the seed catalyzing bath in step 4. The resulting plated portion 546 of the broader via portion 535 can for example be used for mounting components to the

PCB 500. As the plated portion 545 of the narrower via portion 530 is isolated from the plated portion 546 of the broader via portion 535 it can be used for conducting current between other conductive layers in the PCB 500.

5 The embodiments can be implemented in a apparatus that further includes at least one microprocessor, a computer-readable medium including computer-readable instructions, when executed by the at least one microprocessor, are configured to control fabrication equipment to perform the
10 methods described herein. Embodiments can also be implemented in digital electronic circuitry, in computer hardware, firmware, software, or in combinations thereof. Storage device suitable for embodying the computer program instructions include signals capable of programming a data
15 processing system, all forms of non-volatile memory including, but not limited to: semiconductor memory devices such as EPROM, EEPROM, and flash devices; magnetic disks (fixed, floppy, and removable); other magnetic media such as tape; optical media such as CD-ROM, DVD-ROM, and Blu-ray
20 disks; and magneto-optic devices. Any of the foregoing may be supplemented by, or incorporated in, specially-designed application-specific integrated circuits (ASIC) or suitably programmed field programmable gate arrays (FPGAs).

CLAIMS

1. A method of partitioning a via in a multilayer printed circuit board (200) as to produce an electrically isolating portion between two electrically conducting portions in said via, the method comprising the steps of:
- placing (1) at least one island of a first plating resist layer (233) on a first layered structure comprising a first conductive layer (205) and a first dielectric layer (222) and placing (1) at least one island of a second plating resist layer (234) on a second layered structure comprising a second conductive layer (206) and a second dielectric layer (223);
 - laminating (2) the first and second layered structures with a third intermediate layered structure comprising at least one third dielectric layer (213) adapted so that the islands of the first and second plating resist layers (233,234) become embedded in the at least one third dielectric layer (213);
 - drilling (3) a first hole (240) in the printed circuit board (200) so that the first hole (240) passes through the islands of the first and the second plating resist layer (233,234);
 - placing (4) said printed circuit board (200) in a copper seed catalyzing bath so that copper is placed on the interior of the first hole (240) except for the portions (252,253) with the plating resist layer (233,234);
 - placing (5) the printed circuit board (200) in a electrolytic copper plating bath where the copper

- placed on the at least one third dielectric layer portion (255) of the first hole (240) is electrically isolated from the first and second conductive layers (205,206) so that additional copper is placed on the interior of the first hole (240) except for the portions (252,253) of the first and second plating resist layers (233,234) and except for the portion (255) of the at least one third dielectric layer (213);
- 10 - removing (6) the copper placed on the at least one third dielectric layer portion (255) of the first hole (240).
2. A method of claim 1 wherein the third processing step of removing copper from the at least one third dielectric layer portion (255) of the first hole (240) is done by micro etching.
- 15 3. A method of any of the preceding claims wherein the at least one third dielectric layer (213) is made of an impregnated fiber weave adapted to embed the islands of the first and second plating resist layers (233,234).
- 20 4. A method of any of the preceding claims wherein the first hole (240) is partly penetrating the printed circuit board (200).
- 25 5. A method of any of the claims 1-3 wherein the first hole (240) is a through hole through the printed circuit board (200).
- 30 6. A method of claim 5 where the step of drilling (3) the first hole comprises the additional step of drilling with a larger drill from the opposite side of the printed circuit board (500) as to produce two portions (530, 535) of the via with different

diameters and where the two via portions (530, 535) meet each other in a position between the first and second plating resist layers (541,542).

- 5 7. An apparatus comprising at least one
 microprocessor and a computer-readable medium
 including computer-readable instructions, when
 executed by the at least one microprocessor, are
 configured to control fabrication equipment to
10 perform the method steps described in any of the
 preceding claims.