Cross-Coupled Transistor Layouts in Restricted Gate Level Layout Architecture

by inventor

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BACKGROUND

[0001] A push for higher performance and smaller die size drives the semiconductor industry to reduce circuit chip area by approximately 50% every two years. The chip area reduction provides an economic benefit for migrating to newer technologies. The 50% chip area reduction is achieved by reducing the feature sizes between 25% and 30%. The reduction in feature size is enabled by improvements in manufacturing equipment and materials. For example, improvement in the lithographic process has enabled smaller feature sizes to be achieved, while improvement in chemical mechanical polishing (CMP) has in-part enabled a higher number of interconnect layers.

[0002] In the evolution of lithography, as the minimum feature size approached the wavelength of the light source used to expose the feature shapes, unintended interactions occurred between neighboring features. Today minimum feature sizes are approaching 45 nm (nanometers), while the wavelength of the light source used in the photolithography process remains at 193 nm. The difference between the minimum feature size and the wavelength of light used in the photolithography process is defined as the lithographic gap. As the lithographic gap grows, the resolution capability of the lithographic process decreases.

[0003] An interference pattern occurs as each shape on the mask interacts with the light. The interference patterns from neighboring shapes can create constructive or destructive interference. In the case of constructive interference, unwanted shapes may be inadvertently created. In the case of destructive interference, desired shapes may be inadvertently removed. In either case, a particular shape is printed in a different manner than intended, possibly causing a device failure. Correction methodologies, such as optical proximity correction (OPC), attempt to predict the impact from neighboring shapes and modify the mask such that the printed shape is fabricated as desired. The quality of the light interaction prediction is declining as process geometries shrink and as the light interactions become more complex.

[0004] In view of the foregoing, a solution is needed for managing lithographic gap issues as technology continues to progress toward smaller semiconductor device features sizes.

SUMMARY

[0005] In one embodiment, a cross-coupled transistor configuration within a semiconductor chip is disclosed. The cross-coupled transistor configuration includes a first P channel transistor having a first gate electrode defined in a gate level of the chip. The cross-coupled transistor configuration also includes a first N channel transistor having a second gate electrode defined in the gate level of the chip. The second gate electrode of the first N channel transistor is electrically connected to the first gate electrode of the first P channel transistor. The cross-coupled transistor configuration further includes a second P channel transistor having a third gate electrode defined in the gate level of the chip. Also, the cross-coupled transistor configuration includes a second N channel transistor having a fourth gate electrode defined in the gate level of the chip. The fourth gate electrode of the second N channel transistor is electrically connected to the third gate electrode of the second P channel transistor. Each of the first P channel transistor, first N channel transistor, second P channel transistor, and second N channel transistor has a respective diffusion terminal electrically connected to a common node. Also, each of the first, second, third, and fourth gate electrodes corresponds to a portion of a respective gate level feature defined within a gate level feature layout channel. Each gate level feature is defined within its gate level feature layout channel without physically contacting another gate level feature defined within an adjoining gate level feature layout channel.

[0006] In one embodiment, a cross-coupled transistor layout is disclosed. The cross-coupled transistor layout includes a first P channel transistor having a first gate electrode defined in a gate level of the chip. The cross-coupled transistor layout also includes a first N channel transistor having a second gate electrode defined in the gate level of the chip. The second gate electrode of the first N channel transistor is electrically connected to the first gate electrode of the first P channel transistor. The cross-coupled transistor layout further includes a second P channel transistor having a third gate electrode defined in the gate level of the chip. Also, the cross-coupled transistor layout includes a second N channel transistor having a fourth gate electrode defined in the gate level of the chip. The fourth gate electrode of the second N channel transistor is electrically connected to the third gate electrode of the second P channel transistor. Each of the first P channel transistor, first N channel transistor, second P channel transistor, and second N channel transistor has a respective diffusion terminal electrically connected to a common node. Also, each of the first, second, third, and fourth gate electrodes corresponds to a portion of a respective gate level feature defined within a gate level feature layout channel. Each gate

level feature is defined within its gate level feature layout channel without physically contacting another gate level feature defined within an adjoining gate level feature layout channel.

[0007] In another embodiment, a semiconductor chip is disclosed. The chip includes a first P channel transistor defined by a corresponding gate electrode. The chip also includes a first N channel transistor defined by a corresponding gate electrode. The chip also includes a second P channel transistor defined by a corresponding gate electrode. The chip also includes a second N channel transistor defined by a corresponding gate electrode. Each of the gate electrodes of the first P channel, first N channel, second P channel, and second N channel transistors is defined within a gate level of the chip and is electrically connected to a common diffusion node. The gate electrode of the first P channel transistor is electrically connected to the gate electrode of the first N channel transistor. The gate electrode of the second P channel transistor is electrically connected to the gate electrode of the second N channel transistor. Each of the first, second, third, and fourth gate electrodes corresponds to a portion of a respective gate level feature defined within a gate level feature layout channel. Also, each gate level feature is defined within its gate level feature layout channel without physically contacting another gate level feature defined within an adjoining gate level feature layout channel.

[0008] Other aspects and advantages of the invention will become more apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A shows an SRAM bit cell circuit, in accordance with the prior art;

Figure 1B shows the SRAM bit cell of Figure 1A with the inverters expanded to reveal their respective internal transistor configurations, in accordance with the prior art;

Figure 2 shows a cross-coupled transistor configuration, in accordance with one embodiment of the present invention;

Figure 3A shows an example of gate electrode tracks defined within the restricted gate level layout architecture, in accordance with one embodiment of the present invention;

Figure 3B shows the exemplary restricted gate level layout architecture of Figure 3A with a number of exemplary gate level features defined therein, in accordance with one embodiment of the present invention;

Figure 4 shows diffusion and gate level layouts of a cross-coupled transistor configuration, in accordance with one embodiment of the present invention;

Figure 5 shows a variation of the cross-coupled transistor configuration of Figure 4 in which the cross-coupled transistor configuration is defined on three gate electrode tracks with crossing gate electrode connections;

Figure 6 shows a variation of the cross-coupled transistor configuration of Figure 4 in which the cross-coupled transistor configuration is defined on four gate electrode tracks with crossing gate electrode connections;

Figure 7 shows a variation of the cross-coupled transistor configuration of Figure 4 in which the cross-coupled transistor configuration is defined on two gate electrode tracks without crossing gate electrode connections;

Figure 8 shows a variation of the cross-coupled transistor configuration of Figure 4 in which the cross-coupled transistor configuration is defined on three gate electrode tracks without crossing gate electrode connections;

Figure 9 shows a variation of the cross-coupled transistor configuration of Figure 4 in which the cross-coupled transistor configuration is defined on four gate electrode tracks without crossing gate electrode connections;

Figure 10 shows a multi-level layout including a cross-coupled transistor configuration defined on three gate electrode tracks with crossing gate electrode connections, in accordance with one embodiment of the present invention;

Figure 11 shows a multi-level layout including a cross-coupled transistor configuration defined on four gate electrode tracks with crossing gate electrode connections, in accordance with one embodiment of the present invention;

Figure 12 shows a multi-level layout including a cross-coupled transistor configuration defined on two gate electrode tracks without crossing gate electrode connections, in accordance with one embodiment of the present invention;

Figure 13 shows a multi-level layout including a cross-coupled transistor configuration defined on three gate electrode tracks without crossing gate electrode connections, in accordance with one embodiment of the present invention;

Figure 14A shows a generalized multiplexer circuit in which all four cross-coupled transistors are directly connected to the common node, in accordance with one embodiment of the present invention;

Figure 14B shows an exemplary implementation of the multiplexer circuit of Figure 14A with a detailed view of the pull up logic, and the pull down logic, in accordance with one embodiment of the present invention;

Figure 14C shows a multi-level layout of the multiplexer circuit of Figure 14B implemented using a restricted gate level layout architecture cross-coupled transistor layout, in accordance with one embodiment of the present invention;

Figure 15A shows the multiplexer circuit of Figure 14A in which two cross-coupled transistors remain directly connected to the common node, and in which two cross-coupled transistors are positioned outside the pull up logic and pull down logic, respectively, relative to the common node, in accordance with one embodiment of the present invention;

Figure 15B shows an exemplary implementation of the multiplexer circuit of Figure 15A with a detailed view of the pull up logic and the pull down logic, in accordance with one embodiment of the present invention;

Figure 15C shows a multi-level layout of the multiplexer circuit of Figure 15B implemented using a restricted gate level layout architecture cross-coupled transistor layout, in accordance with one embodiment of the present invention;

Figure 16A shows a generalized multiplexer circuit in which the cross-coupled transistors are connected to form two transmission gates to the common node, in accordance with one embodiment of the present invention;

Figure 16B shows an exemplary implementation of the multiplexer circuit of Figure 16A with a detailed view of the driving logic, in accordance with one embodiment of the present invention;

Figure 16C shows a multi-level layout of the multiplexer circuit of Figure 16B implemented using a restricted gate level layout architecture cross-coupled transistor layout, in accordance with one embodiment of the present invention;

Figure 17A shows a generalized multiplexer circuit in which two transistors of the four cross-coupled transistors are connected to form a transmission gate to the common node, in accordance with one embodiment of the present invention;

Figure 17B shows an exemplary implementation of the multiplexer circuit of Figure 17A with a detailed view of the driving logic, in accordance with one embodiment of the present invention;

Figure 17C shows a multi-level layout of the multiplexer circuit of Figure 17B implemented using a restricted gate level layout architecture cross-coupled transistor layout, in accordance with one embodiment of the present invention;

Figure 18A shows a generalized latch circuit implemented using the cross-coupled transistor configuration, in accordance with one embodiment of the present invention;

Figure 18B shows an exemplary implementation of the latch circuit of Figure 18A with a detailed view of the pull up driver logic, the pull down driver logic, the pull up feedback logic, and the pull down feedback logic, in accordance with one embodiment of the present invention;

Figure 18C shows a multi-level layout of the latch circuit of Figure 18B implemented using a restricted gate level layout architecture cross-coupled transistor layout, in accordance with one embodiment of the present invention;

Figure 19A shows the latch circuit of Figure 18A in which two cross-coupled transistors remain directly connected to the common node, and in which two cross-coupled transistors are positioned outside the pull up driver logic and pull down driver logic, respectively, relative to the common node, in accordance with one embodiment of the present invention;

Figure 19B shows an exemplary implementation of the latch circuit of Figure 19A with a detailed view of the pull up driver logic, the pull down driver logic, the pull up feedback logic, and the pull down feedback logic, in accordance with one embodiment of the present invention;

Figure 19C shows a multi-level layout of the latch circuit of Figure 19B implemented using a restricted gate level layout architecture cross-coupled transistor layout, in accordance with one embodiment of the present invention;

Figure 20A shows the latch circuit of Figure 18A in which two cross-coupled transistors remain directly connected to the common node, and in which two cross-coupled transistors are positioned outside the pull up feedback logic and pull down feedback logic, respectively, relative to the common node, in accordance with one embodiment of the present invention;

Figure 20B shows an exemplary implementation of the latch circuit of Figure 20A with a detailed view of the pull up driver logic, the pull down driver logic, the pull up feedback logic, and the pull down feedback logic, in accordance with one embodiment of the present invention;

Figure 20C shows a multi-level layout of the latch circuit of Figure 20B implemented using a restricted gate level layout architecture cross-coupled transistor layout, in accordance with one embodiment of the present invention;

Figure 21A shows a generalized latch circuit in which cross-coupled transistors are connected to form two transmission gates to the common node, in accordance with one embodiment of the present invention;

Figure 21B shows an exemplary implementation of the latch circuit of Figure 21A with a detailed view of the driving logic and the feedback logic, in accordance with one embodiment of the present invention;

Figure 21C shows a multi-level layout of the latch circuit of Figure 21B implemented using a restricted gate level layout architecture cross-coupled transistor layout, in accordance with one embodiment of the present invention;

Figure 22A shows a generalized latch circuit in which two transistors of the four cross-coupled transistors are connected to form a transmission gate to the common node, in accordance with one embodiment of the present invention;

Figure 22B shows an exemplary implementation of the latch circuit of Figure 22A with a detailed view of the driving logic, the pull up feedback logic, and the pull down feedback logic, in accordance with one embodiment of the present invention; and

Figure 22C shows a multi-level layout of the latch circuit of Figure 22B implemented using a restricted gate level layout architecture cross-coupled transistor layout, in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

[0009] In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art that the present invention may be practiced without some or all of these specific details. In other instances, well known process operations have not been described in detail in order not to unnecessarily obscure the present invention.

[0010] SRAM Bit Cell Configuration

[0011] Figure 1A shows an SRAM (Static Random Access Memory) bit cell circuit, in accordance with the prior art. The SRAM bit cell includes two cross-coupled inverters 106 and 102. Specifically, an output 106B of inverter 106 is connected to an input 102A of inverter 102, and an output 102B of inverter 102 is connected to an input 106A of inverter 106. The SRAM bit cell further includes two NMOS pass transistors 100 and 104. The

NMOS pass transistor 100 is connected between a bit-line 103 and a node 109 corresponding to both the output 106B of inverter 106 and the input 102A of inverter 102. The NMOS pass transistor 104 is connected between a bit-line 105 and a node 111 corresponding to both the output 102B of inverter 102 and the input 106A of inverter 106. Also, the respective gates of NMOS pass transistors 100 and 104 are each connected to a word line 107, which controls access to the SRAM bit cell through the NMOS pass transistors 100 and 104. The SRAM bit cell requires bi-directional write, which means that when bit-line 103 is driven high, bit-line 105 is driven low, vice-versa. It should be understood by those skilled in the art that a logic state stored in the SRAM bit cell is maintained in a complementary manner by nodes 109 and 111.

[0012] Figure 1B shows the SRAM bit cell of Figure 1A with the inverters 106 and 102 expanded to reveal their respective internal transistor configurations, in accordance with the prior art. The inverter 106 include a PMOS transistor 115 and an NMOS transistor 113. The respective gates of the PMOS and NMOS transistors 115, 113 are connected together to form the input 106A of inverter 106. Also, each of PMOS and NMOS transistors 115, 113 have one of their respective terminals connected together to form the output 106B of inverter 106. A remaining terminal of PMOS transistor 115 is connected to a power supply 117. A remaining terminal of NMOS transistor 113 is connected to a ground potential 119. Therefore, PMOS and NMOS transistors 115, 113 are activated in a complementary manner. When a high logic state is present at the input 106A of the inverter 106, the NMOS transistor 113 is turned on and the PMOS transistor 115 is turned off, thereby causing a low logic state to be generated at output 106B of the inverter 106. When a low logic state is present at the input 106A of the inverter 106, the NMOS transistor 113 is turned off and the PMOS transistor 115 is turned on, thereby causing a high logic state to be generated at output 106B of the inverter 106.

[0013] The inverter 102 is defined in an identical manner to inverter 106. The inverter 102 include a PMOS transistor 121 and an NMOS transistor 123. The respective gates of the PMOS and NMOS transistors 121, 123 are connected together to form the input 102A of inverter 102. Also, each of PMOS and NMOS transistors 121, 123 have one of their respective terminals connected together to form the output 102B of inverter 102. A remaining terminal of PMOS transistor 121 is connected to the power supply 117. A remaining terminal of NMOS transistor 123 is connected to the ground potential 119. Therefore, PMOS and NMOS transistors 121, 123 are activated in a complementary manner. When a high logic state is present at the input 102A of the inverter 102, the

NMOS transistor 123 is turned on and the PMOS transistor 121 is turned off, thereby causing a low logic state to be generated at output 102B of the inverter 102. When a low logic state is present at the input 102A of the inverter 102, the NMOS transistor 123 is turned off and the PMOS transistor 121 is turned on, thereby causing a high logic state to be generated at output 102B of the inverter 102.

[0014] Cross-Coupled Transistor Configuration

[0015] Figure 2 shows a cross-coupled transistor configuration, in accordance with one embodiment of the present invention. The cross-coupled transistor configuration includes four transistors: a PMOS transistor 401, an NMOS transistor 405, a PMOS transistor 403, and an NMOS transistor 407. The PMOS transistor 401 has one terminal connected to pull up logic 209A, and its other terminal connected to a common node 495. The NMOS transistor 405 has one terminal connected to pull down logic 211A, and its other terminal connected to the common node 495. The PMOS transistor 403 has one terminal connected to pull up logic 209B, and its other terminal connected to the common node 495. The NMOS transistor 407 has one terminal connected to pull down logic 211B, and its other terminal connected to the common node 495. Respective gates of the PMOS transistor 401 and the NMOS transistor 407 are both connected to a gate node 491. Respective gates of the NMOS transistor 405 and the PMOS transistor 403 are both connected to a gate node 493. The gate nodes 491 and 493 are also referred to as control nodes 491 and 493, respectively. Moreover, each of the common node 495, the gate node 491, and the gate node 493 can be referred to as an electrical connection 495, 491, 493, respectively.

[0016] Based on the foregoing, the cross-coupled transistor configuration includes four transistors: 1) a first PMOS transistor, 2) a first NMOS transistor, 3) a second PMOS transistor, and 4) a second NMOS transistor. Furthermore, the cross-coupled transistor configuration includes three required electrical connections: 1) each of the four transistors has one of its terminals connected to a same common node, 2) gates of one PMOS transistor and one NMOS transistor are both connected to a first gate node, and 3) gates of the other PMOS transistor and the other NMOS transistor are both connected to a second gate node.

[0017] It should be understood that the cross-coupled transistor configuration of Figure 2 represents a basic configuration of cross-coupled transistors. In other embodiments, additional circuitry components can be connected to any node within the cross-coupled transistor configuration of Figure 2. Moreover, in other embodiments, additional circuitry components can be inserted between any one or more of the cross-coupled transistors (401,

405, 403, 407) and the common node 495, without departing from the cross-coupled transistor configuration of Figure 2.

[0018] Difference Between SRAM Bit Cell and Cross-Coupled Transistor Configurations

[0019] It should be understood that the SRAM bit cell of Figures 1A-1B does not include a cross-coupled transistor configuration. In particular, it should be understood that the cross-coupled "inverters" 106 and 102 within the SRAM bit cell neither represent nor infer a cross-coupled "transistor" configuration. As discussed above, the cross-coupled transistor configuration requires that each of the four transistors has one of its terminals electrically connected to the same common node. This does not occur in the SRAM bit cell.

[0020] With reference to the SRAM bit cell in Figure 1B, the terminals of PMOS transistor 115 and NMOS transistor 113 are connected together at node 109, but the terminals of PMOS transistor 121 and NMOS transistor 123 are connected together at node 111. More specifically, the terminals of PMOS transistor 115 and NMOS transistor 113 that are connected together at the output 106B of the inverter are connected to the gates of each of PMOS transistor 121 and NMOS transistor 123, and therefore are not connected to both of the terminals of PMOS transistor 121 and NMOS transistor 123. Therefore, the SRAM bit cell does not include four transistors (two PMOS and two NMOS) that each have one of its terminals connected together at a same common node. Consequently, the SRAM bit cell does represent or include a cross-coupled transistor configuration, such as described with regard to Figure 2.

[0021] Restricted Gate Level Layout Architecture

[0022] The present invention implements a restricted gate level layout architecture within a portion of a semiconductor chip. For the gate level, a number of parallel virtual lines are defined to extend across the layout. These parallel virtual lines are referred to as gate electrode tracks, as they are used to index placement of gate electrodes of various transistors within the layout. In one embodiment, the parallel virtual lines which form the gate electrode tracks are defined by a perpendicular spacing therebetween equal to a specified gate electrode pitch. Therefore, placement of gate electrode segments on the gate electrode tracks corresponds to the specified gate electrode pitch. In another embodiment the gate electrode tracks are spaced at variable pitches greater than or equal to a specified gate electrode pitch.

[0023] Figure 3A shows an example of gate electrode tracks 301A-301E defined within the restricted gate level layout architecture, in accordance with one embodiment of the present invention. Gate electrode tracks 301A-301E are formed by parallel virtual lines

that extend across the gate level layout of the chip, with a perpendicular spacing therebetween equal to a specified gate electrode pitch 307. For illustrative purposes, complementary diffusion regions 303 and 305 are shown in Figure 3A. It should be understood that the diffusion regions 303 and 305 are defined in the diffusion level below the gate level. Also, it should be understood that the diffusion regions 303 and 305 are provided by way of example and in no way represent any limitation on diffusion region size, shape, and/or placement within the diffusion level relative to the restricted gate level layout architecture.

[0024] Within the restricted gate level layout architecture, a gate level feature layout channel is defined about a given gate electrode track so as to extend between gate electrode tracks adjacent to the given gate electrode track. For example, gate level feature layout channels 301A-1 through 301E-1 are defined about gate electrode tracks 301A through 301E, respectively. It should be understood that each gate electrode track has a corresponding gate level feature layout channel. Also, for gate electrode tracks positioned adjacent to an edge of a prescribed layout space, e.g., adjacent to a cell boundary, the corresponding gate level feature layout channel extends as if there were a virtual gate electrode track outside the prescribed layout space, as illustrated by gate level feature layout channels 301A-1 and 301E-1. It should be further understood that each gate level feature layout channel is defined to extend along an entire length of its corresponding gate electrode track. Thus, each gate level feature layout channel is defined to extend across the gate level layout within the portion of the chip to which the gate level layout is associated.

[0025] Within the restricted gate level layout architecture, gate level features associated with a given gate electrode track are defined within the gate level feature layout channel associated with the given gate electrode track. A contiguous gate level feature can include both a portion which defines a gate electrode of a transistor, and a portion that does not define a gate electrode of a transistor. Thus, a contiguous gate level feature can extend over both a diffusion region and a dielectric region of an underlying chip level. In one embodiment, each portion of a gate level feature that forms a gate electrode of a transistor is positioned to be substantially centered upon a given gate electrode track. Furthermore, in this embodiment, portions of the gate level feature that do not form a gate electrode of a transistor can be positioned within the gate level feature layout channel associated with the given gate electrode track. Therefore, a given gate level feature can be defined essentially anywhere within a given gate level feature layout channel, so long as gate electrode portions of the given gate level feature are centered upon the gate electrode track

corresponding to the given gate level feature layout channel, and so long as the given gate level feature complies with design rule spacing requirements relative to other gate level features in adjacent gate level layout channels. Additionally, physical contact is prohibited between gate level features defined in gate level feature layout channels that are associated with adjacent gate electrode tracks.

[0026] Figure 3B shows the exemplary restricted gate level layout architecture of Figure 3A with a number of exemplary gate level features 309-323 defined therein, in accordance with one embodiment of the present invention. The gate level feature 309 is defined within the gate level feature layout channel 301A-1 associated with gate electrode track 301A. The gate electrode portions of gate level feature 309 are substantially centered upon the gate electrode track 301A. Also, the non-gate electrode portions of gate level feature 309 maintain design rule spacing requirements with gate level features 311 and 313 defined within adjacent gate level feature layout channel 301B-1. Similarly, gate level features 311-323 are defined within their respective gate level feature layout channel, and have their gate electrode portions substantially centered upon the gate electrode track corresponding to their respective gate level feature layout channel. Also, it should be appreciated that each of gate level features 311-323 maintains design rule spacing requirements with gate level features defined within adjacent gate level feature layout channels, and avoids physical contact with any another gate level feature defined within adjacent gate level feature layout channels.

[0027] A gate electrode corresponds to a portion of a respective gate level feature that extends over a diffusion region, wherein the respective gate level feature is defined in its entirety within a gate level feature layout channel. Each gate level feature is defined within its gate level feature layout channel without physically contacting another gate level feature defined within an adjoining gate level feature layout channel. As illustrated by the example gate level feature layout channels 301A-1 through 301E-1 of Figure 3B, each gate level feature layout channel is associated with a given gate electrode track and corresponds to a layout region that extends along the given gate electrode track and perpendicularly outward in each opposing direction from the given gate electrode track to a closest of either an adjacent gate electrode track or a virtual gate electrode track outside a layout boundary.

[0028] Some gate level features may have one or more contact head portions defined at any number of locations along their length. A contact head portion of a given gate level feature is defined as a segment of the gate level feature having a height and a width of

sufficient size to receive a gate contact structure, wherein "width" is defined across the substrate in a direction perpendicular to the gate electrode track of the given gate level feature, and wherein "height" is defined across the substrate in a direction parallel to the gate electrode track of the given gate level feature. It should be appreciated that a contact head of a gate level feature, when viewed from above, can be defined by essentially any layout shape, including a square or a rectangle. Also, depending on layout requirements and circuit design, a given contact head portion of a gate level feature may or may not have a gate contact defined thereabove.

[0029] A gate level of the various embodiments disclosed herein is defined as a restricted gate level, as discussed above. Some of the gate level features form gate electrodes of transistor devices. Others of the gate level features can form conductive segments extending between two points within the gate level. Also, others of the gate level features may be non-functional with respect to integrated circuit operation. It should be understood that the each of the gate level features, regardless of function, is defined to extend across the gate level within their respective gate level feature layout channels without physically contacting other gate level features defined with adjacent gate level feature layout channels.

[0030] In one embodiment, the gate level features are defined to provide a finite number of controlled layout shape-to-shape lithographic interactions which can be accurately predicted and optimized for in manufacturing and design processes. In this embodiment, the gate level features are defined to avoid layout shape-to-shape spatial relationships which would introduce adverse lithographic interaction within the layout that cannot be accurately predicted and mitigated with high probability. However, it should be understood that changes in direction of gate level features within their gate level layout channels are acceptable when corresponding lithographic interactions are predictable and manageable.

[0031] It should be understood that each of the gate level features, regardless of function, is defined such that no gate level feature along a given gate electrode track is configured to connect directly within the gate level to another gate level feature defined along a different gate electrode track without utilizing a non-gate level feature. Moreover, each connection between gate level features that are placed within different gate level layout channels associated with different gate electrode tracks is made through one or more non-gate level features, which may be defined in higher interconnect levels, i.e., through one or more interconnect levels above the gate level, or by way of local interconnect features at or below the gate level.

[0032] Cross-Coupled Transistor Layouts

[0033] As discussed above, the cross-coupled transistor configuration includes four transistors (2 PMOS transistors and 2 NMOS transistors). In various embodiments of the present invention, gate electrodes defined in accordance with the restricted gate level layout architecture are respectively used to form the four transistors of a cross-coupled transistor configuration layout. Figure 4 shows diffusion and gate level layouts of a cross-coupled transistor configuration, in accordance with one embodiment of the present invention. The cross-coupled transistor layout of Figure 4 includes the first PMOS transistor 401 defined by a gate electrode 401A extending along a gate electrode track 450 and over a p-type diffusion region 480. The first NMOS transistor 407 is defined by a gate electrode 407A extending along a gate electrode track 456 and over an n-type diffusion region 486. The second PMOS transistor 403 is defined by a gate electrode 403A extending along the gate electrode track 456 and over a p-type diffusion region 482. The second NMOS transistor 405 is defined by a gate electrode 405A extending along the gate electrode track 450 and over an n-type diffusion region 484.

[0034] The gate electrodes 401A and 407A of the first PMOS transistor 401 and first NMOS transistor 407, respectively, are electrically connected to the first gate node 491 so as to be exposed to a substantially equivalent gate electrode voltage. Similarly, the gate electrodes 403A and 405A of the second PMOS transistor 403 and second NMOS transistor 405, respectively, are electrically connected to the second gate node 493 so as to be exposed to a substantially equivalent gate electrode voltage. Also, each of the four transistors 401, 403, 405, 407 has a respective diffusion terminal electrically connected to the common output node 495.

[0035] The cross-coupled transistor layout can be implemented in a number of different ways within the restricted gate level layout architecture. In the exemplary embodiment of Figure 4, the gate electrodes 401A and 405A of the first PMOS transistor 401 and second NMOS transistor 405 are positioned along the same gate electrode track 450. Similarly, the gate electrodes 403A and 407A of the second PMOS transistor 403 and second NMOS transistor 407 are positioned along the same gate electrode track 456. Thus, the particular embodiment of Figure 4 can be characterized as a cross-coupled transistor configuration defined on two gate electrode tracks with crossing gate electrode connections.

[0036] Figure 5 shows a variation of the cross-coupled transistor configuration of Figure 4 in which the cross-coupled transistor configuration is defined on three gate electrode tracks with crossing gate electrode connections. Specifically, the gate electrode 401A of the first

PMOS transistor 401 is defined on the gate electrode track 450. The gate electrode 403A of the second PMOS transistor 403 is defined on the gate electrode track 456. The gate electrode 407A of the first NMOS transistor 407 is defined on a gate electrode track 456. And, the gate electrode 405A of the second NMOS transistor 405 is defined on a gate electrode track 448. Thus, the particular embodiment of Figure 5 can be characterized as a cross-coupled transistor configuration defined on three gate electrode tracks with crossing gate electrode connections.

[0037] Figure 6 shows a variation of the cross-coupled transistor configuration of Figure 4 in which the cross-coupled transistor configuration is defined on four gate electrode tracks with crossing gate electrode connections. Specifically, the gate electrode 401A of the first PMOS transistor 401 is defined on the gate electrode track 450. The gate electrode 403A of the second PMOS transistor 403 is defined on the gate electrode track 456. The gate electrode 407A of the first NMOS transistor 407 is defined on a gate electrode track 458. And, the gate electrode 405A of the second NMOS transistor 405 is defined on a gate electrode track 454. Thus, the particular embodiment of Figure 6 can be characterized as a cross-coupled transistor configuration defined on four gate electrode tracks with crossing gate electrode connections.

[0038] Figure 7 shows a variation of the cross-coupled transistor configuration of Figure 4 in which the cross-coupled transistor configuration is defined on two gate electrode tracks without crossing gate electrode connections. Specifically, the gate electrode 401A of the first PMOS transistor 401 is defined on the gate electrode track 450. The gate electrode 407A of the first NMOS transistor 407 is also defined on a gate electrode track 450. The gate electrode 403A of the second PMOS transistor 403 is defined on the gate electrode track 456. And, the gate electrode 405A of the second NMOS transistor 405 is also defined on a gate electrode track 456. Thus, the particular embodiment of Figure 7 can be characterized as a cross-coupled transistor configuration defined on two gate electrode tracks without crossing gate electrode connections.

[0039] Figure 8 shows a variation of the cross-coupled transistor configuration of Figure 4 in which the cross-coupled transistor configuration is defined on three gate electrode tracks without crossing gate electrode connections. Specifically, the gate electrode 401A of the first PMOS transistor 401 is defined on the gate electrode track 450. The gate electrode 407A of the first NMOS transistor 407 is also defined on a gate electrode track 450. The gate electrode 403A of the second PMOS transistor 403 is defined on the gate electrode track 454. And, the gate electrode 405A of the second NMOS transistor 405 is defined on a

gate electrode track 456. Thus, the particular embodiment of Figure 8 can be characterized as a cross-coupled transistor configuration defined on three gate electrode tracks without crossing gate electrode connections.

[0040] Figure 9 shows a variation of the cross-coupled transistor configuration of Figure 4 in which the cross-coupled transistor configuration is defined on four gate electrode tracks without crossing gate electrode connections. Specifically, the gate electrode 401A of the first PMOS transistor 401 is defined on the gate electrode track 450. The gate electrode 403A of the second PMOS transistor 403 is defined on the gate electrode track 454. The gate electrode 407A of the first NMOS transistor 407 is defined on a gate electrode track 452. And, the gate electrode 405A of the second NMOS transistor 405 is defined on a gate electrode track 456. Thus, the particular embodiment of Figure 9 can be characterized as a cross-coupled transistor configuration defined on four gate electrode tracks without crossing gate electrode connections.

[0041] It should be appreciated that although the cross-coupled transistors 401, 403, 405, 407 of Figures 4-9 are depicted as having their own respective diffusion region 480, 482, 484, 486, respectively, other embodiments may utilize a contiguous p-type diffusion region for PMOS transistors 401 and 403, and/or utilize a contiguous n-type diffusion region for NMOS transistors 405 and 407. Moreover, although the example layouts of Figures 4-9 depict the p-type diffusion regions 480 and 482 in a vertically aligned position, it should be understood that the p-type diffusion regions 480 and 482 may not be vertically aligned in other embodiments. Similarly, although the example layouts of Figures 4-9 depict the n-type diffusion regions 484 and 486 in a vertically aligned position, it should be understood that the n-type diffusion regions 484 and 486 may not be vertically aligned in other embodiments.

[0042] In Figures 4-9, the gate electrode connections are electrically represented by lines 491 and 493, and the common node electrical connection is represented by line 495. It should be understood that in layout space each of the gate electrode electrical connections 491, 493, and the common node electrical connection 495 can be structurally defined by a number of layout shapes extending through multiple chip levels. Figures 10-13 show examples of how the gate electrode electrical connections 491, 493, and the common node electrical connection 495 can be defined in different embodiments. It should be understood that the example layouts of Figures 10-13 are provided by way of example and in no way represent an exhaustive set of possible multi-level connections that can be utilized for the

gate electrode electrical connections 491, 493, and the common node electrical connection 495.

[0043] Figure 10 shows a multi-level layout including a cross-coupled transistor configuration defined on three gate electrode tracks with crossing gate electrode connections, in accordance with one embodiment of the present invention. The layout of Figure 10 represents an exemplary implementation of the cross-coupled transistor embodiment of Figure 5. The electrical connection 491 between the gate electrode 401A of the first PMOS transistor 401 and the gate electrode 407A of the first NMOS transistor 407 is formed by a multi-level connection that includes a gate contact 1001, a (two-dimensional) metal-1 structure 1003, and a gate contact 1005. The electrical connection 493 between the gate electrode 403A of the second PMOS transistor 403 and the gate electrode 405A of the second NMOS transistor 405 is formed by a multi-level connection that includes a gate contact 1007, a (two-dimensional) metal-1 structure 1009, and a gate contact 1011. The output node electrical connection 495 is formed by a multi-level connection that includes a diffusion contact 1013, a (two-dimensional) metal-1 structure 1015, a diffusion contact 1017, and a diffusion contact 1019.

[0044] Figure 11 shows a multi-level layout including a cross-coupled transistor configuration defined on four gate electrode tracks with crossing gate electrode connections, in accordance with one embodiment of the present invention. The layout of Figure 11 represents an exemplary implementation of the cross-coupled transistor embodiment of Figure 6. The electrical connection 491 between the gate electrode 401A of the first PMOS transistor 401 and the gate electrode 407A of the first NMOS transistor 407 is formed by a multi-level connection that includes a gate contact 1101, a (two-dimensional) metal-1 structure 1103, and a gate contact 1105. The electrical connection 493 between the gate electrode 403A of the second PMOS transistor 403 and the gate electrode 405A of the second NMOS transistor 405 is formed by a multi-level connection that includes a gate contact 1107, a (one-dimensional) metal-1 structure 1109, a via 1111, a (one-dimensional) metal-2 structure 1113, a via 1115, a (one-dimensional) metal-1 structure 1117, and a gate contact 1119. The output node electrical connection 495 is formed by a multi-level connection that includes a diffusion contact 1121, a (two-dimensional) metal-1 structure 1123, a diffusion contact 1125, and a diffusion contact 1127.

[0045] Figure 12 shows a multi-level layout including a cross-coupled transistor configuration defined on two gate electrode tracks without crossing gate electrode

connections, in accordance with one embodiment of the present invention. The layout of Figure 12 represents an exemplary implementation of the cross-coupled transistor embodiment of Figure 7. The gate electrodes 401A and 407A of the first PMOS transistor 401 and first NMOS transistor 407, respectively, are formed by a contiguous gate level structure placed on the gate electrode track 450. Therefore, the electrical connection 491 between the gate electrodes 401A and 407A is made directly within the gate level along the single gate electrode track 450. Similarly, the gate electrodes 403A and 405A of the second PMOS transistor 403 and second NMOS transistor 405, respectively, are formed by a contiguous gate level structure placed on the gate electrode track 456. Therefore, the electrical connection 493 between the gate electrodes 403A and 405A is made directly within the gate level along the single gate electrode track 456. The output node electrical connection 495 is formed by a multi-level connection that includes a diffusion contact 1205, a (one-dimensional) metal-1 structure 1207, and a diffusion contact 1209.

[0046] Further with regard to Figure 12, it should be noted that when the gate electrodes 401A and 407A of the first PMOS transistor 401 and first NMOS transistor 407, respectively, are formed by a contiguous gate level structure, and when the gate electrodes 403A and 405A of the second PMOS transistor 403 and second NMOS transistor 405, respectively, are formed by a contiguous gate level structure, the corresponding cross-coupled transistor layout may include electrical connections between diffusion regions associated with the four cross-coupled transistors 401, 407, 403, 405, that cross in layout space without electrical communication therebetween. For example, diffusion region 1220 of PMOS transistor 403 is electrically connected to diffusion region 1222 of NMOS transistor 407 as indicated by electrical connection 1224, and diffusion region 1230 of PMOS transistor 401 is electrically connected to diffusion region 1232 of NMOS transistor 405 as indicated by electrical connection 1234, wherein electrical connections 1224 and 1234 cross in layout space without electrical communication therebetween.

[0047] Figure 13 shows a multi-level layout including a cross-coupled transistor configuration defined on three gate electrode tracks without crossing gate electrode connections, in accordance with one embodiment of the present invention. The layout of Figure 13 represents an exemplary implementation of the cross-coupled transistor embodiment of Figure 8. The gate electrodes 401A and 407A of the first PMOS transistor 401 and first NMOS transistor 407, respectively, are formed by a contiguous gate level structure placed on the gate electrode track 450. Therefore, the electrical connection 491 between the gate electrodes 401A and 407A is made directly within the gate level along

the single gate electrode track 450. The electrical connection 493 between the gate electrode 403A of the second PMOS transistor 403 and the gate electrode 405A of the second NMOS transistor 405 is formed by a multi-level connection that includes a gate contact 1303, a (one-dimensional) metal-1 structure 1305, and a gate contact 1307. The output node electrical connection 495 is formed by a multi-level connection that includes a diffusion contact 1311, a (one-dimensional) metal-1 structure 1313, and a diffusion contact 1315.

[0048] In one embodiment, electrical connection of the diffusion regions of the cross-coupled transistors to the common node 495 can be made using one or more local interconnect conductors defined at or below the gate level itself. This embodiment may also combine local interconnect conductors with conductors in higher levels (above the gate level) by way of contacts and/or vias to make the electrical connection of the diffusion regions of the cross-coupled transistors to the common node 495. Additionally, in various embodiments, conductive paths used to electrically connect the diffusion regions of the cross-coupled transistors to the common node 495 can be defined to traverse over essentially any area of the chip as required to accommodate a routing solution for the chip.

[0049] Also, it should be appreciated that because the n-type and p-type diffusion regions are physically separate, and because the p-type diffusion regions for the two PMOS transistors of the cross-coupled transistors can be physically separate, and because the n-type diffusion regions for the two NMOS transistors of the cross-coupled transistors can be physically separate, it is possible in various embodiments to have each of the four cross-coupled transistors disposed at arbitrary locations in the layout relative to each other. Therefore, unless necessitated by electrical performance or other layout influencing conditions, it is not required that the four cross-coupled transistors be located within a prescribed proximity to each other in the layout. Although, location of the cross-coupled transistors within a prescribed proximity to each other is not precluded, and may be desirable in certain circuit layouts.

[0050] In the exemplary embodiments disclosed herein, it should be understood that diffusion regions are not restricted in size. In other words, any given diffusion region can be sized in an arbitrary manner as required to satisfy electrical and/or layout requirements. Additionally, any given diffusion region can be shaped in an arbitrary manner as required to satisfy electrical and/or layout requirements. Also, it should be understood that the four transistors of the cross-coupled transistor configuration, as defined in accordance with the restricted gate level layout architecture, are not required to be the same size. In different

embodiments, the four transistors of the cross-coupled transistor configuration can either vary in size (transistor width or transistor gate length) or have the same size, depending on the applicable electrical and/or layout requirements.

[0051] Additionally, it should be understood that the four transistors of the cross-coupled transistor configuration are not required to be placed in close proximity to each, although they may be closely placed in some embodiments. More specifically, because connections between the transistors of the cross-coupled transistor configuration can be made by routing through as least one higher interconnect level, there is freedom in placement of the four transistors of the cross-coupled transistor configuration relative to each other. Although, it should be understood that a proximity of the four transistors of the cross-coupled transistor configuration may be governed in certain embodiments by electrical and/or layout optimization requirements.

[0052] It should be appreciated that the cross-coupled transistor configurations and corresponding layouts implemented using the restricted gate level layout architecture, as described with regard to Figures 2-13, and/or variants thereof, can be used to form many different electrical circuits. For example, a portion of a modern semiconductor chip is likely to include a number of multiplexer circuits and/or latch circuits. Such multiplexer and/or latch circuits can be defined using cross-coupled transistor configurations and corresponding layouts based on the restricted gate level layout architecture, as disclosed herein. Example multiplexer embodiments implemented using the restricted gate level layout architecture and corresponding cross-coupled transistor configurations are described with regard to Figures 14A-17C. Example latch embodiments implemented using the restricted gate level layout architecture and corresponding cross-coupled transistor configurations are described with regard to Figures 18A-22C. It should be understood that the multiplexer and latch embodiments described with regard to Figures 14A-22C are provided by way of example and do not represent an exhaustive set of possible multiplexer and latch embodiments.

[0053] Example Multiplexer Embodiments

[0054] Figure 14A shows a generalized multiplexer circuit in which all four cross-coupled transistors 401, 405, 403, 407 are directly connected to the common node 495, in accordance with one embodiment of the present invention. As previously discussed, gates of the first PMOS transistor 401 and first NMOS transistor 407 are electrically connected, as shown by electrical connection 491. Also, gates of the second PMOS transistor 403 and second NMOS transistor 405 are electrically connected, as shown by electrical connection

493. Pull up logic 1401 is electrically connected to the first PMOS transistor 401 at a terminal opposite the common node 495. Pull down logic 1403 is electrically connected to the second NMOS transistor 405 at a terminal opposite the common node 495. Also, pull up logic 1405 is electrically connected to the second PMOS transistor 403 at a terminal opposite the common node 495. Pull down logic 1407 is electrically connected to the first NMOS transistor 407 at a terminal opposite the common node 495.

[0055] Figure 14B shows an exemplary implementation of the multiplexer circuit of Figure 14A with a detailed view of the pull up logic 1401 and 1405, and the pull down logic 1403 and 1407, in accordance with one embodiment of the present invention. The pull up logic 1401 is defined by a PMOS transistor 1401A connected between a power supply (VDD) and a terminal 1411 of the first PMOS transistor 401 opposite the common node 495. The pull down logic 1403 is defined by an NMOS transistor 1403A connected between a ground potential (GND) and a terminal 1413 of the second NMOS transistor 405 opposite the common node 495. Respective gates of the PMOS transistor 1401A and NMOS transistor 1403A are connected together at a node 1415. The pull up logic 1405 is defined by a PMOS transistor 1405A connected between the power supply (VDD) and a terminal 1417 of the second PMOS transistor 403 opposite the common node 495. The pull down logic 1407 is defined by an NMOS transistor 1407A connected between a ground potential (GND) and a terminal 1419 of the first NMOS transistor 407 opposite the common node 495. Respective gates of the PMOS transistor 1405A and NMOS transistor 1407A are connected together at a node 1421. It should be understood that the implementations of pull up logic 1401, 1405 and pull down logic 1403, 1407 as shown in Figure 14B are exemplary. In other embodiments, logic different than that shown in Figure 14B can be used to implement the pull up logic 1401, 1405 and the pull down logic 1403, 1407.

[0056] Figure 14C shows a multi-level layout of the multiplexer circuit of Figure 14B implemented using a restricted gate level layout architecture cross-coupled transistor layout, in accordance with one embodiment of the present invention. The electrical connection 491 between the gate electrode 401A of the first PMOS transistor 401 and the gate electrode 407A of the first NMOS transistor 407 is formed by a multi-level connection that includes a gate contact 1445, a (two-dimensional) metal-1 structure 1447, and a gate contact 1449. The electrical connection 493 between the gate electrode 403A of the second PMOS transistor 403 and the gate electrode 405A of the second NMOS transistor 405 is formed by a multi-level connection that includes a gate contact 1431, a

(one-dimensional) metal-1 structure 1433, a via 1435, a (one-dimensional) metal-2 structure 1436, a via 1437, a (one-dimensional) metal-1 structure 1439, and a gate contact 1441. The common node electrical connection 495 is formed by a multi-level connection that includes a diffusion contact 1451, a (one-dimensional) metal-1 structure 1453, a via 1455, a (one-dimensional) metal-2 structure 1457, a via 1459, a (one-dimensional) metal-1 structure 1461, and a diffusion contact 1463. Respective gates of the PMOS transistor 1401A and NMOS transistor 1403A are connected to the node 1415 by a gate contact 1443. Also, respective gates of the PMOS transistor 1405A and NMOS transistor 1407A are connected to the node 1421 by a gate contact 1465.

[0057] Figure 15A shows the multiplexer circuit of Figure 14A in which the two cross-coupled transistors 401 and 405 remain directly connected to the common node 495, and in which the two cross-coupled transistors 403 and 407 are positioned outside the pull up logic 1405 and pull down logic 1407, respectively, relative to the common node 495, in accordance with one embodiment of the present invention. Pull up logic 1405 is electrically connected between the second PMOS transistor 403 and the common node 495. Pull down logic 1407 is electrically connected between the first NMOS transistor 407 and the common node 495. With the exception of repositioning the PMOS/NMOS transistors 403/407 outside of their pull up/down logic 1405/1407 relative to the common node 495, the circuit of Figure 15A is the same as the circuit of Figure 14A.

[0058] Figure 15B shows an exemplary implementation of the multiplexer circuit of Figure 15A with a detailed view of the pull up logic 1401 and 1405, and the pull down logic 1403 and 1407, in accordance with one embodiment of the present invention. As previously discussed with regard to Figure 14B, the pull up logic 1401 is defined by the PMOS transistor 1401A connected between VDD and the terminal 1411 of the first PMOS transistor 401 opposite the common node 495. Also, the pull down logic 1403 is defined by NMOS transistor 1403A connected between GND and the terminal 1413 of the second NMOS transistor 405 opposite the common node 495. Respective gates of the PMOS transistor 1401A and NMOS transistor 1403A are connected together at the node 1415. The pull up logic 1405 is defined by the PMOS transistor 1405A connected between the second PMOS transistor 403 and the common node 495. The pull down logic 1407 is defined by the NMOS transistor 1407A connected between the first NMOS transistor 407 and the common node 495. Respective gates of the PMOS transistor 1405A and NMOS transistor 1407A are connected together at the node 1421. It should be understood that the implementations of pull up logic 1401, 1405 and pull down logic 1403, 1407 as shown in

Figure 15B are exemplary. In other embodiments, logic different than that shown in Figure 15B can be used to implement the pull up logic 1401, 1405 and the pull down logic 1403, 1407.

[0059] Figure 15C shows a multi-level layout of the multiplexer circuit of Figure 15B implemented using a restricted gate level layout architecture cross-coupled transistor layout, in accordance with one embodiment of the present invention. The electrical connection 491 between the gate electrode 401A of the first PMOS transistor 401 and the gate electrode 407A of the first NMOS transistor 407 is formed by a multi-level connection that includes a gate contact 1501, a (one-dimensional) metal-1 structure 1503, a via 1505, a (one-dimensional) metal-2 structure 1507, a via 1509, a (one-dimensional) metal-1 structure 1511, and a gate contact 1513. The electrical connection 493 between the gate electrode 403A of the second PMOS transistor 403 and the gate electrode 405A of the second NMOS transistor 405 is formed by a multi-level connection that includes a gate contact 1515, a (two-dimensional) metal-1 structure 1517, and a gate contact 1519. The common node electrical connection 495 is formed by a multi-level connection that includes a diffusion contact 1521, a (one-dimensional) metal-1 structure 1523, a via 1525, a (one-dimensional) metal-2 structure 1527, a via 1529, a (one-dimensional) metal-1 structure 1531, and a diffusion contact 1533. Respective gates of the PMOS transistor 1401A and NMOS transistor 1403A are connected to the node 1415 by a gate contact 1535. Also, respective gates of the PMOS transistor 1405A and NMOS transistor 1407A are connected to the node 1421 by a gate contact 1539.

[0060] Figure 16A shows a generalized multiplexer circuit in which the cross-coupled transistors (401, 403, 405, 407) are connected to form two transmission gates 1602, 1604 to the common node 495, in accordance with one embodiment of the present invention. As previously discussed, gates of the first PMOS transistor 401 and first NMOS transistor 407 are electrically connected, as shown by electrical connection 491. Also, gates of the second PMOS transistor 403 and second NMOS transistor 405 are electrically connected, as shown by electrical connection 493. The first PMOS transistor 401 and second NMOS transistor 405 are connected to form a first transmission gate 1602 to the common node 495. The second PMOS transistor 403 and first NMOS transistor 407 are connected to form a second transmission gate 1604 to the common node 495. Driving logic 1601 is electrically connected to both the first PMOS transistor 401 and second NMOS transistor 405 at a terminal opposite the common node 495. Driving logic 1603 is electrically

connected to both the second PMOS transistor 403 and first NMOS transistor 407 at a terminal opposite the common node 495.

[0061] Figure 16B shows an exemplary implementation of the multiplexer circuit of Figure 16A with a detailed view of the driving logic 1601 and 1603, in accordance with one embodiment of the present invention. In the embodiment of Figure 16B, the driving logic 1601 is defined by an inverter 1601A and, the driving logic 1603 is defined by an inverter 1603A. However, it should be understood that in other embodiments, the driving logic 1601 and 1603 can be defined by any logic function, such as a two input NOR gate, a two input NAND gate, AND-OR logic, OR-AND logic, among others, by way of example.

[0062] Figure 16C shows a multi-level layout of the multiplexer circuit of Figure 16B implemented using a restricted gate level layout architecture cross-coupled transistor layout, in accordance with one embodiment of the present invention. The electrical connection 491 between the gate electrode 401A of the first PMOS transistor 401 and the gate electrode 407A of the first NMOS transistor 407 is formed by a multi-level connection that includes a gate contact 1619, a (two-dimensional) metal-1 structure 1621, and a gate contact 1623. The electrical connection 493 between the gate electrode 403A of the second PMOS transistor 403 and the gate electrode 405A of the second NMOS transistor 405 is formed by a multi-level connection that includes a gate contact 1605, a (one-dimensional) metal-1 structure 1607, a via 1609, a (one-dimensional) metal-2 structure 1611, a via 1613, a (one-dimensional) metal-1 structure 1615, and a gate contact 1617. The common node electrical connection 495 is formed by a multi-level connection that includes a diffusion contact 1625, a (one-dimensional) metal-1 structure 1627, a via 1629, a (one-dimensional) metal-2 structure 1631, a via 1633, a (one-dimensional) metal-1 structure 1635, and a diffusion contact 1637. Transistors which form the inverter 1601A are shown within the region bounded by the dashed line 1601AL. Transistors which form the inverter 1603A are shown within the region bounded by the dashed line 1603AL.

[0063] Figure 17A shows a generalized multiplexer circuit in which two transistors (403, 407) of the four cross-coupled transistors are connected to form a transmission gate 1702 to the common node 495, in accordance with one embodiment of the present invention. As previously discussed, gates of the first PMOS transistor 401 and first NMOS transistor 407 are electrically connected, as shown by electrical connection 491. Also, gates of the second PMOS transistor 403 and second NMOS transistor 405 are electrically connected, as shown by electrical connection 493. The second PMOS transistor 403 and first NMOS transistor 407 are connected to form the transmission gate 1702 to the common node 495.

Driving logic 1701 is electrically connected to both the second PMOS transistor 403 and first NMOS transistor 407 at a terminal opposite the common node 495. Pull up driving logic 1703 is electrically connected to the first PMOS transistor 401 at a terminal opposite the common node 495. Also, pull down driving logic 1705 is electrically connected to the second NMOS transistor 405 at a terminal opposite the common node 495.

[0064] Figure 17B shows an exemplary implementation of the multiplexer circuit of Figure 17A with a detailed view of the driving logic 1701, 1703, and 1705, in accordance with one embodiment of the present invention. The driving logic 1701 is defined by an inverter 1701A. The pull up driving logic 1703 is defined by a PMOS transistor 1703A connected between VDD and the first PMOS transistor 401. The pull down driving logic 1705 is defined by an NMOS transistor 1705A connected between GND and the second NMOS transistor 405. Respective gates of the PMOS transistor 1703A and NMOS transistor 1705A are connected together at the node 1707. It should be understood that the implementations of driving logic 1701, 1703, and 1705, as shown in Figure 17B are exemplary. In other embodiments, logic different than that shown in Figure 17B can be used to implement the driving logic 1701, 1703, and 1705.

[0065] Figure 17C shows a multi-level layout of the multiplexer circuit of Figure 17B implemented using a restricted gate level layout architecture cross-coupled transistor layout, in accordance with one embodiment of the present invention. The electrical connection 491 between the gate electrode 401A of the first PMOS transistor 401 and the gate electrode 407A of the first NMOS transistor 407 is formed by a multi-level connection that includes a gate contact 1723, a (two-dimensional) metal-1 structure 1725, and a gate contact 1727. The electrical connection 493 between the gate electrode 403A of the second PMOS transistor 403 and the gate electrode 405A of the second NMOS transistor 405 is formed by a multi-level connection that includes a gate contact 1709, a (one-dimensional) metal-1 structure 1711, a via 1713, a (one-dimensional) metal-2 structure 1715, a via 1717, a (one-dimensional) metal-1 structure 1719, and a gate contact 1721. The common node electrical connection 495 is formed by a multi-level connection that includes a diffusion contact 1729, a (one-dimensional) metal-1 structure 1731, a via 1733, a (one-dimensional) metal-2 structure 1735, a via 1737, a (one-dimensional) metal-1 structure 1739, and a diffusion contact 1741. Transistors which form the inverter 1701A are shown within the region bounded by the dashed line 1701AL. Respective gates of the PMOS transistor 1703A and NMOS transistor 1705A are connected to the node 1707 by a gate contact 1743.

[0066] Example Latch Embodiments

[0067] Figure 18A shows a generalized latch circuit implemented using the cross-coupled transistor configuration, in accordance with one embodiment of the present invention. The gates of the first PMOS transistor 401 and first NMOS transistor 407 are electrically connected, as shown by electrical connection 491. The gates of the second PMOS transistor 403 and second NMOS transistor 405 are electrically connected, as shown by electrical connection 493. Each of the four cross-coupled transistors are electrically connected to the common node 495. It should be understood that the common node 495 serves as a storage node in the latch circuit. Pull up driver logic 1805 is electrically connected to the second PMOS transistor 403 at a terminal opposite the common node 495. Pull down driver logic 1807 is electrically connected to the first NMOS transistor 407 at a terminal opposite the common node 495. Pull up feedback logic 1809 is electrically connected to the first PMOS transistor 401 at a terminal opposite the common node 495. Pull down feedback logic 1811 is electrically connected to the second NMOS transistor 405 at a terminal opposite the common node 495. Additionally, the common node 495 is connected to an input of an inverter 1801. An output of the inverter 1801 is electrically connected to a feedback node 1803. It should be understood that in other embodiments the inverter 1801 can be replaced by any logic function, such as a two input NOR gate, a two input NAND gate, among others, or any complex logic function.

[0068] Figure 18B shows an exemplary implementation of the latch circuit of Figure 18A with a detailed view of the pull up driver logic 1805, the pull down driver logic 1807, the pull up feedback logic 1809, and the pull down feedback logic 1811, in accordance with one embodiment of the present invention. The pull up driver logic 1805 is defined by a PMOS transistor 1805A connected between VDD and the second PMOS transistor 403 opposite the common node 495. The pull down driver logic 1807 is defined by an NMOS transistor 1807A connected between GND and the first NMOS transistor 407 opposite the common node 495. Respective gates of the PMOS transistor 1805A and NMOS transistor 1807A are connected together at a node 1804. The pull up feedback logic 1809 is defined by a PMOS transistor 1809A connected between VDD and the first PMOS transistor 401 opposite the common node 495. The pull down feedback logic 1811 is defined by an NMOS transistor 1811A connected between GND and the second NMOS transistor 405 opposite the common node 495. Respective gates of the PMOS transistor 1809A and NMOS transistor 1811A are connected together at the feedback node 1803. It should be understood that the implementations of pull up driver logic 1805, pull down driver logic

1807, pull up feedback logic 1809, and pull down feedback logic 1811 as shown in Figure 18B are exemplary. In other embodiments, logic different than that shown in Figure 18B can be used to implement the pull up driver logic 1805, the pull down driver logic 1807, the pull up feedback logic 1809, and the pull down feedback logic 1811.

[0069] Figure 18C shows a multi-level layout of the latch circuit of Figure 18B implemented using a restricted gate level layout architecture cross-coupled transistor layout, in accordance with one embodiment of the present invention. The electrical connection 491 between the gate electrode 401A of the first PMOS transistor 401 and the gate electrode 407A of the first NMOS transistor 407 is formed by a multi-level connection that includes a gate contact 1813, a (one-dimensional) metal-1 structure 1815, a via 1817, a (one-dimensional) metal-2 structure 1819, a via 1821, a (one-dimensional) metal-1 structure 1823, and a gate contact 1825. The electrical connection 493 between the gate electrode 403A of the second PMOS transistor 403 and the gate electrode 405A of the second NMOS transistor 405 is formed by a multi-level connection that includes a gate contact 1827, a (two-dimensional) metal-1 structure 1829, and a gate contact 1831. The common node electrical connection 495 is formed by a multi-level connection that includes a diffusion contact 1833, a (one-dimensional) metal-1 structure 1835, a via 1837, a (one-dimensional) metal-2 structure 1839, a via 1841, a (two-dimensional) metal-1 structure 1843, and a diffusion contact 1845. Transistors which form the inverter 1801 are shown within the region bounded by the dashed line 1801L.

[0070] Figure 19A shows the latch circuit of Figure 18A in which the two cross-coupled transistors 401 and 405 remain directly connected to the output node 495, and in which the two cross-coupled transistors 403 and 407 are positioned outside the pull up driver logic 1805 and pull down driver logic 1807, respectively, relative to the common node 495, in accordance with one embodiment of the present invention. Pull up driver logic 1805 is electrically connected between the second PMOS transistor 403 and the common node 495. Pull down driver logic 1807 is electrically connected between the first NMOS transistor 407 and the common node 495. With the exception of repositioning the PMOS/NMOS transistors 403/407 outside of their pull up/down driver logic 1805/1807 relative to the common node 495, the circuit of Figure 19A is the same as the circuit of Figure 18A.

[0071] Figure 19B shows an exemplary implementation of the latch circuit of Figure 19A with a detailed view of the pull up driver logic 1805, pull down driver logic 1807, pull up feedback logic 1809, and pull down feedback logic 1811, in accordance with one

embodiment of the present invention. As previously discussed with regard to Figure 18B, the pull up feedback logic 1809 is defined by the PMOS transistor 1809A connected between VDD and the first PMOS transistor 401 opposite the common node 495. Also, the pull down feedback logic 1811 is defined by NMOS transistor 1811A connected between GND and the second NMOS transistor 405 opposite the common node 495. Respective gates of the PMOS transistor 1809A and NMOS transistor 1811A are connected together at the feedback node 1803. The pull up driver logic 1805 is defined by the PMOS transistor 1805A connected between the second PMOS transistor 403 and the common node 495. The pull down driver logic 1807 is defined by the NMOS transistor 1807A connected between the first NMOS transistor 407 and the common node 495. Respective gates of the PMOS transistor 1805A and NMOS transistor 1807A are connected together at the node 1804. It should be understood that the implementations of pull up driver logic 1805, pull down driver logic 1807, pull up feedback logic 1809, and pull down feedback logic 1811 as shown in Figure 19B are exemplary. In other embodiments, logic different than that shown in Figure 19B can be used to implement the pull up driver logic 1805, the pull down driver logic 1807, the pull up feedback logic 1809, and the pull down feedback logic 1811.

[0072] Figure 19C shows a multi-level layout of the latch circuit of Figure 19B implemented using a restricted gate level layout architecture cross-coupled transistor layout, in accordance with one embodiment of the present invention. The electrical connection 491 between the gate electrode 401A of the first PMOS transistor 401 and the gate electrode 407A of the first NMOS transistor 407 is formed by a multi-level connection that includes a gate contact 1901, a (one-dimensional) metal-1 structure 1903, a via 1905, a (one-dimensional) metal-2 structure 1907, a via 1909, a (one-dimensional) metal-1 structure 1911, and a gate contact 1913. The electrical connection 493 between the gate electrode 403A of the second PMOS transistor 403 and the gate electrode 405A of the second NMOS transistor 405 is formed by a multi-level connection that includes a gate contact 1915, a (two-dimensional) metal-1 structure 1917, and a gate contact 1919. The common node electrical connection 495 is formed by a multi-level connection that includes a diffusion contact 1921, a (one-dimensional) metal-1 structure 1923, a via 1925, a (one-dimensional) metal-2 structure 1927, a via 1929, a (two-dimensional) metal-1 structure 1931, and a diffusion contact 1933. Transistors which form the inverter 1801 are shown within the region bounded by the dashed line 1801L.

[0073] Figure 20A shows the latch circuit of Figure 18A in which the two cross-coupled transistors 403 and 407 remain directly connected to the output node 495, and in which the

two cross-coupled transistors 401 and 405 are positioned outside the pull up feedback logic 1809 and pull down feedback logic 1811, respectively, relative to the common node 495, in accordance with one embodiment of the present invention. Pull up feedback logic 1809 is electrically connected between the first PMOS transistor 401 and the common node 495. Pull down feedback logic 1811 is electrically connected between the second NMOS transistor 405 and the common node 495. With the exception of repositioning the PMOS/NMOS transistors 401/405 outside of their pull up/down feedback logic 1809/1811 relative to the common node 495, the circuit of Figure 20A is the same as the circuit of Figure 18A.

[0074] Figure 20B shows an exemplary implementation of the latch circuit of Figure 20A with a detailed view of the pull up driver logic 1805, pull down driver logic 1807, pull up feedback logic 1809, and pull down feedback logic 1811, in accordance with one embodiment of the present invention. The pull up feedback logic 1809 is defined by the PMOS transistor 1809A connected between the first PMOS transistor 401 and the common node 495. Also, the pull down feedback logic 1811 is defined by NMOS transistor 1811A connected between the second NMOS transistor 405 and the common node 495. Respective gates of the PMOS transistor 1809A and NMOS transistor 1811A are connected together at the feedback node 1803. The pull up driver logic 1805 is defined by the PMOS transistor 1805A connected between VDD and the second PMOS transistor 403. The pull down driver logic 1807 is defined by the NMOS transistor 1807A connected between GND and the first NMOS transistor 407. Respective gates of the PMOS transistor 1805A and NMOS transistor 1807A are connected together at the node 1804. It should be understood that the implementations of pull up driver logic 1805, pull down driver logic 1807, pull up feedback logic 1809, and pull down feedback logic 1811 as shown in Figure 20B are exemplary. In other embodiments, logic different than that shown in Figure 20B can be used to implement the pull up driver logic 1805, the pull down driver logic 1807, the pull up feedback logic 1809, and the pull down feedback logic 1811.

[0075] Figure 20C shows a multi-level layout of the latch circuit of Figure 20B implemented using a restricted gate level layout architecture cross-coupled transistor layout, in accordance with one embodiment of the present invention. The electrical connection 491 between the gate electrode 401A of the first PMOS transistor 401 and the gate electrode 407A of the first NMOS transistor 407 is formed by a multi-level connection that includes a gate contact 2001, a (one-dimensional) metal-1 structure 2003, a via 2005, a (one-dimensional) metal-2 structure 2007, a via 2009, a (one-dimensional)

metal-1 structure 2011, and a gate contact 2013. The electrical connection 493 between the gate electrode 403A of the second PMOS transistor 403 and the gate electrode 405A of the second NMOS transistor 405 is formed by a multi-level connection that includes a gate contact 2015, a (one-dimensional) metal-1 structure 2017, and a gate contact 2019. The common node electrical connection 495 is formed by a multi-level connection that includes a diffusion contact 2021, a (two-dimensional) metal-1 structure 2023, and a diffusion contact 2025. Transistors which form the inverter 1801 are shown within the region bounded by the dashed line 1801L.

[0076] Figure 21A shows a generalized latch circuit in which the cross-coupled transistors (401, 403, 405, 407) are connected to form two transmission gates 2103, 2105 to the common node 495, in accordance with one embodiment of the present invention. As previously discussed, gates of the first PMOS transistor 401 and first NMOS transistor 407 are electrically connected, as shown by electrical connection 491. Also, gates of the second PMOS transistor 403 and second NMOS transistor 405 are electrically connected, as shown by electrical connection 493. The first PMOS transistor 401 and second NMOS transistor 405 are connected to form a first transmission gate 2103 to the common node 495. The second PMOS transistor 403 and first NMOS transistor 407 are connected to form a second transmission gate 2105 to the common node 495. Feedback logic 2109 is electrically connected to both the first PMOS transistor 401 and second NMOS transistor 405 at a terminal opposite the common node 495. Driving logic 2107 is electrically connected to both the second PMOS transistor 403 and first NMOS transistor 407 at a terminal opposite the common node 495. Additionally, the common node 495 is connected to the input of the inverter 1801. The output of the inverter 1801 is electrically connected to a feedback node 2101. It should be understood that in other embodiments the inverter 1801 can be replaced by any logic function, such as a two input NOR gate, a two input NAND gate, among others, or any complex logic function.

[0077] Figure 21B shows an exemplary implementation of the latch circuit of Figure 21A with a detailed view of the driving logic 2107 and feedback logic 2109, in accordance with one embodiment of the present invention. The driving logic 2107 is defined by an inverter 2107A. Similarly, the feedback logic 2109 is defined by an inverter 2109A. It should be understood that in other embodiments, the driving logic 2107 and/or 2109 can be defined by logic other than an inverter.

[0078] Figure 21C shows a multi-level layout of the latch circuit of Figure 21B implemented using a restricted gate level layout architecture cross-coupled transistor

layout, in accordance with one embodiment of the present invention. The electrical connection 491 between the gate electrode 401A of the first PMOS transistor 401 and the gate electrode 407A of the first NMOS transistor 407 is formed by a multi-level connection that includes a gate contact 2111, a (one-dimensional) metal-1 structure 2113, a via 2115, a (one-dimensional) metal-2 structure 2117, a via 2119, a (one-dimensional) metal-1 structure 2121, and a gate contact 2123. The electrical connection 493 between the gate electrode 403A of the second PMOS transistor 403 and the gate electrode 405A of the second NMOS transistor 405 is formed by a multi-level connection that includes a gate contact 2125, a (two-dimensional) metal-1 structure 2127, and a gate contact 2129. The common node electrical connection 495 is formed by a multi-level connection that includes a diffusion contact 2131, a (one-dimensional) metal-1 structure 2133, a via 2135, a (one-dimensional) metal-2 structure 2137, a via 2139, a (two-dimensional) metal-1 structure 2141, and a diffusion contact 2143. Transistors which form the inverter 2107A are shown within the region bounded by the dashed line 2107AL. Transistors which form the inverter 2109A are shown within the region bounded by the dashed line 2109AL. Transistors which form the inverter 1801 are shown within the region bounded by the dashed line 1801L.

[0079] Figure 22A shows a generalized latch circuit in which two transistors (403, 407) of the four cross-coupled transistors are connected to form a transmission gate 2105 to the common node 495, in accordance with one embodiment of the present invention. As previously discussed, gates of the first PMOS transistor 401 and first NMOS transistor 407 are electrically connected, as shown by electrical connection 491. Also, gates of the second PMOS transistor 403 and second NMOS transistor 405 are electrically connected, as shown by electrical connection 493. The second PMOS transistor 403 and first NMOS transistor 407 are connected to form the transmission gate 2105 to the common node 495. Driving logic 2201 is electrically connected to both the second PMOS transistor 403 and first NMOS transistor 407 at a terminal opposite the common node 495. Pull up feedback logic 2203 is electrically connected to the first PMOS transistor 401 at a terminal opposite the common node 495. Also, pull down feedback logic 2205 is electrically connected to the second NMOS transistor 405 at a terminal opposite the common node 495.

[0080] Figure 22B shows an exemplary implementation of the latch circuit of Figure 22A with a detailed view of the driving logic 2201, the pull up feedback logic 2203, and the pull down feedback logic 2205, in accordance with one embodiment of the present invention. The driving logic 2201 is defined by an inverter 2201A. The pull up feedback logic 2203 is defined by a PMOS transistor 2203A connected between VDD and the first

PMOS transistor 401. The pull down feedback logic 2205 is defined by an NMOS transistor 2205A connected between GND and the second NMOS transistor 405. Respective gates of the PMOS transistor 2203A and NMOS transistor 2205A are connected together at the feedback node 2101. It should be understood that in other embodiments, the driving logic 2201 can be defined by logic other than an inverter. Also, it should be understood that in other embodiments, the pull up feedback logic 2203 and/or pull down feedback logic 2205 can be defined logic different than what is shown in Figure 22B.

[0081] Figure 22C shows a multi-level layout of the latch circuit of Figure 22B implemented using a restricted gate level layout architecture cross-coupled transistor layout, in accordance with one embodiment of the present invention. The electrical connection 491 between the gate electrode 401A of the first PMOS transistor 401 and the gate electrode 407A of the first NMOS transistor 407 is formed by a multi-level connection that includes a gate contact 2207, a (one-dimensional) metal-1 structure 2209, a via 2211, a (one-dimensional) metal-2 structure 2213, a via 2215, a (one-dimensional) metal-1 structure 2217, and a gate contact 2219. The electrical connection 493 between the gate electrode 403A of the second PMOS transistor 403 and the gate electrode 405A of the second NMOS transistor 405 is formed by a multi-level connection that includes a gate contact 2221, a (two-dimensional) metal-1 structure 2223, and a gate contact 2225. The common node electrical connection 495 is formed by a multi-level connection that includes a diffusion contact 2227, a (one-dimensional) metal-1 structure 2229, a via 2231, a (one-dimensional) metal-2 structure 2233, a via 2235, a (two-dimensional) metal-1 structure 2237, and a diffusion contact 2239. Transistors which form the inverter 2201A are shown within the region bounded by the dashed line 2201AL. Transistors which form the inverter 1801 are shown within the region bounded by the dashed line 1801L.

[0082] Exemplary Embodiments

[0083] In one embodiment, a cross-coupled transistor configuration is defined within a semiconductor chip. This embodiment is illustrated in part with regard to Figure 2. In this embodiment, a first P channel transistor (401) is defined to include a first gate electrode (401A) defined in a gate level of the chip. Also, a first N channel transistor (407) is defined to include a second gate electrode (407A) defined in the gate level of the chip. The second gate electrode (407A) of the first N channel transistor (407) is electrically connected to the first gate electrode (401A) of the first P channel transistor (401). Further, a second P channel transistor (403) is defined to include a third gate electrode (403A) defined in the

gate level of a chip. Also, a second N channel transistor (405) is defined to include a fourth gate electrode (405A) defined in the gate level of the chip. The fourth gate electrode (405A) of the second N channel transistor (405) is electrically connected to the third gate electrode (403A) of the second P channel transistor (403). Additionally, each of the first P channel transistor (401), first N channel transistor (407), second P channel transistor (403), and second N channel transistor (405) has a respective diffusion terminal electrically connected to a common node (495).

[0084] It should be understood that in some embodiments, one or more of the first P channel transistor (401), the first N channel transistor (407), the second P channel transistor (403), and the second N channel transistor (405) can be respectively implemented by a number of transistors electrically connected in parallel. In this instance, the transistors that are electrically connected in parallel can be considered as one device corresponding to either of the first P channel transistor (401), the first N channel transistor (407), the second P channel transistor (403), and the second N channel transistor (405). It should be understood that electrical connection of multiple transistors in parallel to form a given transistor of the cross-coupled transistor configuration can be utilized to achieve a desired drive strength for the given transistor.

[0085] In one embodiment, each of the first (401A), second (407A), third (403A), and fourth (405A) gate electrodes is defined to extend along any of a number of gate electrode tracks, such as described with regard to Figure 3. The number of gate electrode tracks extend across the gate level of the chip in a parallel orientation with respect to each other. Also, it should be understood that each of the first (401A), second (407A), third (403A), and fourth (405A) gate electrodes corresponds to a portion of a respective gate level feature defined within a gate level feature layout channel. Each gate level feature is defined within its gate level feature layout channel without physically contacting another gate level feature defined within an adjoining gate level feature layout channel. Each gate level feature layout channel is associated with a given gate electrode track and corresponds to a layout region that extends along the given gate electrode track and perpendicularly outward in each opposing direction from the given gate electrode track to a closest of either an adjacent gate electrode track or a virtual gate electrode track outside a layout boundary, such as described with regard to Figure 3B.

[0086] In various implementations of the above-described embodiment, such as in the exemplary layouts of Figures 10, 11, 14C, 15C, 16C, 17C, 18C, 19C, 20C, 21C, 22C, the second gate electrode (407A) is electrically connected to the first gate electrode (401A)

through at least one electrical conductor defined within any chip level other than the gate level. And, the fourth gate electrode (405A) is electrically connected to the third gate electrode (403A) through at least one electrical conductor defined within any chip level other than the gate level.

[0087] In various implementations of the above-described embodiment, such as in the exemplary layout of Figure 13, both the second gate electrode (407A) and the first gate electrode (401A) are formed from a single gate level feature that is defined within a same gate level feature layout channel that extends along a single gate electrode track over both a p type diffusion region and an n type diffusion region. And, the fourth gate electrode (405A) is electrically connected to the third gate electrode (403A) through at least one electrical conductor defined within any chip level other than the gate level.

[0088] In various implementations of the above-described embodiment, such as in the exemplary layouts of Figure 12, both the second gate electrode (407A) and the first gate electrode (401A) are formed from a first gate level feature that is defined within a first gate level feature layout channel that extends along a first gate electrode track over both a p type diffusion region and an n type diffusion region. And, both the fourth gate electrode (405A) and the third gate electrode (403A) are formed from a second gate level feature that is defined within a second gate level feature layout channel that extends along a second gate electrode track over both a p type diffusion region and an n type diffusion region.

[0089] In one embodiment, the above-described gate electrode cross-coupled transistor configuration is used to implement a multiplexer having no transmission gates. This embodiment is illustrated in part with regard to Figures 14-15. In this embodiment, a first configuration of pull-up logic (1401) is electrically connected to the first P channel transistor (401), a first configuration of pull-down logic (1407) electrically connected to the first N channel transistor (407), a second configuration of pull-up logic (1405) electrically connected to the second P channel transistor (403), and a second configuration of pull-down logic (1403) electrically connected to the second N channel transistor (405).

[0090] In the particular embodiments of Figures 14B and 15B, the first configuration of pull-up logic (1401) is defined by a third P channel transistor (1401A), and the second configuration of pull-down logic (1403) is defined by a third N channel transistor (1403A). Respective gates of the third P channel transistor (1401A) and third N channel transistor (1403A) are electrically connected together so as to receive a substantially equivalent electrical signal. Moreover, the first configuration of pull-down logic (1407) is defined by a fourth N channel transistor (1407A), and the second configuration of pull-up logic (1405)

is defined by a fourth P channel transistor (1405A). Respective gates of the fourth P channel transistor (1405A) and fourth N channel transistor (1407A) are electrically connected together so as to receive a substantially equivalent electrical signal.

[0091] In one embodiment, the above-described gate electrode cross-coupled transistor configuration is used to implement a multiplexer having one transmission gate. This embodiment is illustrated in part with regard to Figure 17. In this embodiment, a first configuration of pull-up logic (1703) is electrically connected to the first P channel transistor (401), a first configuration of pull-down logic (1705) electrically connected to the second N channel transistor (405), and mux driving logic (1701) is electrically connected to both the second P channel transistor (403) and the first N channel transistor (407).

[0092] In the exemplary embodiment of Figure 17B, the first configuration of pull-up logic (1703) is defined by a third P channel transistor (1703A), and the first configuration of pull-down logic (1705) is defined by a third N channel transistor (1705A). Respective gates of the third P channel transistor (1703A) and third N channel transistor (1705A) are electrically connected together so as to receive a substantially equivalent electrical signal. Also, the mux driving logic (1701) is defined by an inverter (1701A).

[0093] In one embodiment, the above-described gate electrode cross-coupled transistor configuration is used to implement a latch having no transmission gates. This embodiment is illustrated in part with regard to Figures 18-20. In this embodiment, pull-up driver logic (1805) is electrically connected to the second P channel transistor (403), pull-down driver logic (1807) is electrically connected to the first N channel transistor (407), pull-up feedback logic (1809) is electrically connected to the first P channel transistor (401), and pull-down feedback logic (1811) is electrically connected to the second N channel transistor (405). Also, the latch includes an inverter (1801) having an input connected to the common node (495) and an output connected to a feedback node (1803). Each of the pull-up feedback logic (1809) and pull-down feedback logic (1811) is connected to the feedback node (1803).

[0094] In the exemplary embodiments of Figures 18B, 19B, and 20B, the pull-up driver logic (1805) is defined by a third P channel transistor (1805A), and the pull-down driver logic (1807) is defined by a third N channel transistor (1807A). Respective gates of the third P channel transistor (1805A) and third N channel transistor (1807A) are electrically connected together so as to receive a substantially equivalent electrical signal. Additionally, the pull-up feedback logic (1809) is defined by a fourth P channel transistor

(1809A), and the pull-down feedback logic (1811) is defined by a fourth N channel transistor (1811A). Respective gates of the fourth P channel transistor (1809A) and fourth N channel transistor (1811A) are electrically connected together at the feedback node (1803).

[0095] In one embodiment, the above-described gate electrode cross-coupled transistor configuration is used to implement a latch having two transmission gates. This embodiment is illustrated in part with regard to Figure 21. In this embodiment, driving logic (2107) is electrically connected to both the second P channel transistor (403) and the first N channel transistor (407). Also, feedback logic (2109) is electrically connected to both the first P channel transistor (401) and the second N channel transistor (405). The latch further includes a first inverter (1801) having an input connected to the common node (495) and an output connected to a feedback node (2101). The feedback logic (2109) is electrically connected to the feedback node (2101). In the exemplary embodiment of Figure 21B, the driving logic (2107) is defined by a second inverter (2107A), and the feedback logic (2109) is defined by a third inverter (2109A).

[0096] In one embodiment, the above-described gate electrode cross-coupled transistor configuration is used to implement a latch having one transmission gate. This embodiment is illustrated in part with regard to Figure 22. In this embodiment, driving logic (2201) is electrically connected to both the second P channel transistor (403) and the first N channel transistor (407). Also, pull up feedback logic (2203) is electrically connected to the first P channel transistor (401), and pull down feedback logic (2205) electrically connected to the second N channel transistor (405). The latch further includes a first inverter (1801) having an input connected to the common node (495) and an output connected to a feedback node (2101). Both the pull up feedback logic (2203) and pull down feedback logic (2205) are electrically connected to the feedback node (2101). In the exemplary embodiment of Figure 22B, the driving logic (2201) is defined by a second inverter (2201A). Also, the pull up feedback logic (2203) is defined by a third P channel transistor (2203A) electrically connected between the first P channel transistor (401) and the feedback node (2101). The pull down feedback logic (2205) is defined by a third N channel transistor (2205A) electrically connected between the second N channel transistor (405) and the feedback node (2101).

[0097] It should be understood that the cross-coupled transistor layouts implemented within the restricted gate level layout architecture as disclosed herein can be stored in a tangible form, such as in a digital format on a computer readable medium. Also, the

invention described herein can be embodied as computer readable code on a computer readable medium. The computer readable medium is any data storage device that can store data which can thereafter be read by a computer system. Examples of the computer readable medium include hard drives, network attached storage (NAS), read-only memory, random-access memory, CD-ROMs, CD-Rs, CD-RWs, magnetic tapes, and other optical and non-optical data storage devices. The computer readable medium can also be distributed over a network of coupled computer systems so that the computer readable code is stored and executed in a distributed fashion.

[0098] Any of the operations described herein that form part of the invention are useful machine operations. The invention also relates to a device or an apparatus for performing these operations. The apparatus may be specially constructed for the required purpose, such as a special purpose computer. When defined as a special purpose computer, the computer can also perform other processing, program execution or routines that are not part of the special purpose, while still being capable of operating for the special purpose. Alternatively, the operations may be processed by a general purpose computer selectively activated or configured by one or more computer programs stored in the computer memory, cache, or obtained over a network. When data is obtained over a network the data maybe processed by other computers on the network, e.g., a cloud of computing resources.

[0099] The embodiments of the present invention can also be defined as a machine that transforms data from one state to another state. The data may represent an article, that can be represented as an electronic signal and electronically manipulate data. The transformed data can, in some cases, be visually depicted on a display, representing the physical object that results from the transformation of data. The transformed data can be saved to storage generally, or in particular formats that enable the construction or depiction of a physical and tangible object. In some embodiments, the manipulation can be performed by a processor. In such an example, the processor thus transforms the data from one thing to another. Still further, the methods can be processed by one or more machines or processors that can be connected over a network. Each machine can transform data from one state or thing to another, and can also process data, save data to storage, transmit data over a network, display the result, or communicate the result to another machine.

[00100] While this invention has been described in terms of several embodiments, it will be appreciated that those skilled in the art upon reading the preceding specifications and studying the drawings will realize various alterations, additions, permutations and equivalents thereof. Therefore, it is intended that the present invention includes all such

alterations, additions, permutations, and equivalents as fall within the true spirit and scope of the invention.

What is claimed is:

CLAIMS

1. A cross-coupled transistor configuration within a semiconductor chip, comprising:

a first P channel transistor including a first gate electrode defined in a gate level of a chip;

a first N channel transistor including a second gate electrode defined in the gate level of the chip, wherein the second gate electrode of the first N channel transistor is electrically connected to the first gate electrode of the first P channel transistor;

a second P channel transistor including a third gate electrode defined in the gate level of a chip;

a second N channel transistor including a fourth gate electrode defined in the gate level of the chip, wherein the fourth gate electrode of the second N channel transistor is electrically connected to the third gate electrode of the second P channel transistor; and

wherein each of the first P channel transistor, first N channel transistor, second P channel transistor, and second N channel transistor has a respective diffusion terminal electrically connected to a common node,

wherein each of the first, second, third, and fourth gate electrodes corresponds to a portion of an associated gate level feature defined within a corresponding gate level feature layout channel,

wherein each gate level feature is defined within its gate level feature layout channel without physically contacting another gate level feature defined within an adjoining gate level feature layout channel,

wherein both the first and second gate electrodes are formed from a single gate level feature, and

wherein the third gate electrode is electrically connected to the fourth gate electrode through at least one electrical conductor defined within a chip level other than the gate level.

2. The cross-coupled transistor configuration within a semiconductor chip as recited in claim 1, wherein each of the first, second, third, and fourth gate electrodes is defined to extend along an associated gate electrode track, wherein each gate electrode track extends across the gate level of the chip in a first direction.

3. The cross-coupled transistor configuration within a semiconductor chip as recited in claim 2, wherein each gate level feature layout channel is associated with a given gate electrode track and corresponds to a layout region that extends along the given gate electrode track and perpendicularly outward in each opposing direction from the given gate electrode track to a closest of either an adjacent gate electrode track or a virtual gate electrode track outside a layout boundary.

4. The cross-coupled transistor configuration within a semiconductor chip as recited in claim 3, wherein the single gate level feature that forms both the first and second gate electrodes is defined within a gate level feature layout channel that extends over both a p type diffusion region and an n type diffusion region.

5. The cross-coupled transistor configuration within a semiconductor chip as recited in claim 1, further comprising:

a first configuration of pull-up logic electrically connected to the first P channel transistor;

a first configuration of pull-down logic electrically connected to the first N channel transistor;

a second configuration of pull-up logic electrically connected to the second P channel transistor; and

a second configuration of pull-down logic electrically connected to the second N channel transistor.

6. The cross-coupled transistor configuration within a semiconductor chip as recited in claim 5, wherein the first configuration of pull-up logic is defined by a third P channel transistor,

wherein the second configuration of pull-down logic is defined by a third N channel transistor, wherein respective gates of the third P channel transistor and third N channel transistor are electrically connected together so as to receive a substantially equivalent electrical signal,

wherein the first configuration of pull-down logic is defined by a fourth N channel transistor, and

wherein the second configuration of pull-up logic is defined by a fourth P channel transistor, wherein respective gates of the fourth P channel transistor and fourth N channel transistor are electrically connected together so as to receive a substantially equivalent electrical signal.

7. The cross-coupled transistor configuration within a semiconductor chip as recited in claim 1, further comprising:

a first configuration of pull-up logic electrically connected to the first P channel transistor;

a first configuration of pull-down logic electrically connected to the second N channel transistor;

mux driving logic electrically connected to both the second P channel transistor and the first N channel transistor.

8. The cross-coupled transistor configuration within a semiconductor chip as recited in claim 7, wherein the first configuration of pull-up logic is defined by a third P channel transistor,

wherein the first configuration of pull-down logic is defined by a third N channel transistor, wherein respective gates of the third P channel transistor and third N channel transistor are electrically connected together so as to receive a substantially equivalent electrical signal,

wherein the mux driving logic is defined by an inverter.

9. The cross-coupled transistor configuration within a semiconductor chip as recited in claim 1, further comprising:

pull-up driver logic electrically connected to the second P channel transistor;

pull-down driver logic electrically connected to the first N channel transistor;

pull-up feedback logic electrically connected to the first P channel transistor; and

pull-down feedback logic electrically connected to the second N channel transistor; and

an inverter having an input connected to the common node and an output connected to a feedback node, wherein the pull-up feedback logic and pull-down feedback logic are connected to the feedback node.

10. The cross-coupled transistor configuration within a semiconductor chip as recited in claim 9, wherein the pull-up driver logic is defined by a third P channel transistor,

wherein the pull-down driver logic is defined by a third N channel transistor, wherein respective gates of the third P channel transistor and third N channel transistor are electrically connected together so as to receive a substantially equivalent electrical signal,

wherein the pull-up feedback logic is defined by a fourth P channel transistor,

wherein the pull-down feedback logic is defined by a fourth N channel transistor, wherein respective gates of the fourth P channel transistor and fourth N channel transistor are electrically connected together at the feedback node.

11. The cross-coupled transistor configuration within a semiconductor chip as recited in claim 1, further comprising:

driving logic electrically connected to both the second P channel transistor and the first N channel transistor;

feedback logic electrically connected to both the first P channel transistor and the second N channel transistor; and

a first inverter having an input connected to the common node and an output connected to a feedback node, wherein the feedback logic is electrically connected to the feedback node.

12. The cross-coupled transistor configuration within a semiconductor chip as recited in claim 11, wherein the driving logic is defined by a second inverter, and wherein the feedback logic is defined by a third inverter.

13. The cross-coupled transistor configuration within a semiconductor chip as recited in claim 1, further comprising:

driving logic electrically connected to both the second P channel transistor and the first N channel transistor;

pull up feedback logic electrically connected to the first P channel transistor;

pull down feedback logic electrically connected to the second N channel transistor; and

a first inverter having an input connected to the common node and an output connected to a feedback node, wherein both the pull up feedback logic and pull down feedback logic are electrically connected to the feedback node.

14. The cross-coupled transistor configuration within a semiconductor chip as recited in claim 13, wherein the driving logic is defined by a second inverter,

wherein the pull up feedback logic is defined by a third P channel transistor electrically connected between the first P channel transistor and the feedback node,

wherein the pull down feedback logic is defined by a third N channel transistor electrically connected between the second N channel transistor and the feedback node.

15. A cross-coupled transistor configuration within a semiconductor chip, comprising:

a first P channel transistor including a first gate electrode defined in a gate level of a chip;

a first N channel transistor including a second gate electrode defined in the gate level of the chip, wherein the second gate electrode of the first N channel transistor is electrically connected to the first gate electrode of the first P channel transistor;

a second P channel transistor including a third gate electrode defined in the gate level of a chip;

a second N channel transistor including a fourth gate electrode defined in the gate level of the chip, wherein the fourth gate electrode of the second N channel transistor is electrically connected to the third gate electrode of the second P channel transistor; and

wherein each of the first P channel transistor, first N channel transistor, second P channel transistor, and second N channel transistor has a respective diffusion terminal electrically connected to a common node, and

wherein each of the first, second, third, and fourth gate electrodes corresponds to a portion of an associated gate level feature defined within a corresponding gate level feature layout channel, and

wherein each gate level feature is defined within its gate level feature layout channel without physically contacting another gate level feature defined within an adjoining gate level feature layout channel, and

wherein the first gate electrode is electrically connected to the second gate electrode through at least one electrical conductor defined within a chip level other than the gate level, and

wherein both the first and second P channel transistors are physically separated from each of the first and second N channel transistors.

16. The cross-coupled transistor configuration within the semiconductor chip as recited in claim 15, wherein each of the first, second, third, and fourth gate electrodes is defined to extend along an associated gate electrode track, wherein each gate electrode track extends across the gate level of the chip in a first direction.

17. The cross-coupled transistor configuration within the semiconductor chip as recited in claim 16, wherein each gate level feature layout channel is associated with a given gate electrode track and corresponds to a layout region that extends along the given gate electrode track and perpendicularly outward in each opposing direction from the given gate electrode track to a closest of either an adjacent gate electrode track or a virtual gate electrode track outside a layout boundary.

18. The cross-coupled transistor configuration within the semiconductor chip as recited in claim 15,

wherein each of the first, second, third, and fourth gate electrodes is defined to extend lengthwise in a first direction, and

wherein the first and fourth gate electrodes are substantially co-aligned in the first direction.

19. The cross-coupled transistor configuration within the semiconductor chip as recited in claim 18, wherein the second and third gate electrodes are substantially co-aligned in the first direction.

20. The cross-coupled transistor configuration within the semiconductor chip as recited in claim 15, wherein the third gate electrode is electrically connected to the fourth gate electrode through at least one electrical conductor defined within a chip level other than the gate level.

21. The cross-coupled transistor configuration within the semiconductor chip as recited in claim 15, wherein the first and fourth gate electrodes extend along different lines in the first direction, and wherein the second and third gate electrodes extend along different lines in the first direction.

22. A semiconductor chip, comprising:

a first P channel transistor defined by a first gate electrode;

a first N channel transistor defined by a second gate electrode;

a second P channel transistor defined by a third gate electrode; and

a second N channel transistor defined by a fourth gate electrode,

wherein each of the first, second, third, and fourth gate electrodes is defined within a gate level of the semiconductor chip and is electrically associated with a common diffusion node,

wherein the first gate electrode of the first P channel transistor is electrically connected to the second gate electrode of the first N channel transistor,

wherein the third gate electrode of the second P channel transistor is electrically connected to the fourth gate electrode of the second N channel transistor,

wherein each of the first, second, third, and fourth gate electrodes corresponds to a portion of an associated gate level feature defined within a corresponding gate level feature layout channel,

wherein each gate level feature is defined within its gate level feature layout channel without physically contacting another gate level feature defined within an adjoining gate level feature layout channel,

wherein each of the first, second, third, and fourth gate electrodes is defined to extend lengthwise in a first direction, and

wherein the first and fourth gate electrodes are substantially co-aligned in the first direction, and

wherein both the first and second P channel transistors are physically separated from each of the first and second N channel transistors.

23. The semiconductor chip as recited in claim 22, wherein each of the first, second, third, and fourth gate electrodes is defined to extend along an associated gate electrode track, wherein each gate electrode track extends across the gate level of the chip in the first direction.

24. The semiconductor chip as recited in claim 23, wherein each gate level feature layout channel is associated with a given gate electrode track and corresponds to a layout region that extends along the given gate electrode track and perpendicularly outward in each opposing direction from the given gate electrode track to a closest of either an adjacent gate electrode track or a virtual gate electrode track outside a layout boundary.

25. The semiconductor chip as recited in claim 22, wherein the second and third gate electrodes are substantially co-aligned in the first direction.

26. The semiconductor chip as recited in claim 22, wherein the first gate electrode is electrically connected to the second gate electrode through at least one electrical conductor defined within a chip level other than the gate level.

27. The semiconductor chip as recited in claim 22, wherein the second and third gate electrodes extend along different lines in the first direction.

28. The semiconductor chip as recited in claim 22, wherein the third gate electrode is electrically connected to the fourth gate electrode through at least one electrical conductor defined within a chip level other than the gate level.

29. The semiconductor chip as recited in claim 23, wherein adjacent gate electrode tracks are separated by a substantially equal spacing as measured in a second direction perpendicular to the first direction.

30. A semiconductor chip, comprising:

a first transistor of a first transistor type defined by a first gate electrode and a first diffusion region of a first diffusion type electrically connected to a common diffusion node;

a first transistor of a second transistor type defined by a second gate electrode and a first diffusion region of a second diffusion type electrically connected to the common diffusion node;

a second transistor of the first transistor type defined by a third gate electrode and a second diffusion region of the first diffusion type electrically connected to the common diffusion node;

a second transistor of the second transistor type defined by a fourth gate electrode and a second diffusion region of the second diffusion type electrically connected to the common diffusion node,

wherein the first and fourth gate electrodes are electrically connected to each other,

wherein the second and third gate electrodes are electrically connected to each other,

wherein each of the first, second, third, and fourth gate electrodes corresponds to a portion of an associated gate level feature defined within a corresponding gate level feature layout channel,

wherein each gate level feature is defined within its gate level feature layout channel without physically contacting another gate level feature defined within an adjoining gate level feature layout channel,

wherein the first, second, third, and fourth gate electrodes are respectively formed from physically separate gate level features, and

wherein the first and second diffusion regions of the first diffusion type are physically separated from each of the first and second diffusion regions of the second diffusion type.

31. The semiconductor chip as recited in claim 30, wherein each of the first, second, third, and fourth gate electrodes is defined to extend along an associated gate electrode track, wherein each gate electrode track extends across the gate level of the chip in the first direction.

32. The semiconductor chip as recited in claim 31, wherein each gate level feature layout channel is associated with a given gate electrode track and corresponds to a layout region that extends along the given gate electrode track and perpendicularly outward in each opposing direction from the given gate electrode track to a closest of either an adjacent gate electrode track or a virtual gate electrode track outside a layout boundary.

33. The semiconductor chip as recited in claim 30, wherein each of the first, second, third, and fourth gate electrodes is defined to extend lengthwise in a first direction, and wherein the first and fourth gate electrodes are substantially co-aligned in the first direction.

34. The semiconductor chip as recited in claim 33, wherein the second and third gate electrodes are substantially co-aligned in the first direction.

35. The semiconductor chip as recited in claim 30, wherein each of the first, second, third, and fourth gate electrodes is defined to extend lengthwise in a first direction, and wherein the first gate electrode is defined to extend along a different line in the first direction than each of the second and fourth gate electrodes.

36. The semiconductor chip as recited in claim 35, wherein the third gate electrode is defined to extend along a same line in the first direction as either of the second or fourth gate electrodes.

37. The semiconductor chip as recited in claim 35, wherein the third gate electrode is defined to extend along a different line in the first direction than each of the second or fourth gate electrodes.