

PATENT SPECIFICATION

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(54) IMPROVEMENTS IN OR RELATING TO ELECTRONIC TIMEPIECES

(71) We, KABUSHIKI KAISHA DAINI SEIKOSHA, a Japanese company, of 31-1, 6-chome, Kameido, Koto-ku, Tokyo, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to electronic timepieces and more specifically to electronic timepieces with digital display of time by means of light emitting diodes (LEDs). Although not limited exclusively to its application thereto, the invention is especially advantageous for and primarily intended for wrist watches.

The use of LEDs to display time digitally in a timepiece has many practical advantages over other available types of light emitting displays. However, LEDs have the disadvantage of relatively large power consumption. This disadvantage is especially serious in the case of battery powered electronic watches for the space available in the watch to house the battery is severely limited. In fact, with conventional wrist watches of conveniently small size it is, in practice, difficult to the point of impossibility, to fit a battery which will have an acceptably long useful life (a minimum of one year's life is a usual requirement) if the LED display is continuously in operation. For this reason it is customary, in such wrist watches, to have the LED display normally out of use and to provide the watch with a switch which the user operates when he wishes to see the time and which, when operated, brings the display into use. This is a disadvantage since it involves the need to actuate the switch whenever the user wants to see the time and, because the user may have both hands occupied, can be a positive nuisance.

The main object of the present invention is so to reduce the power consumption of an

electronic timepiece with a LED digital time display that the display can be left normally in use, even in the case of a battery driven wrist watch, without running down the battery in an unacceptably short time, thus avoiding the need of a switch to bring the display into operation whenever the user wishes to see the time. As will be seen later the invention achieves this object while still providing a display which is satisfactory to the user.

According to this invention there is provided an electronic timepiece having an LED digital time display and time-keeping means providing time-representative signals for operating said display wherein the digital display segment electrodes in said display are operated by said signals in time-shared manner by means including an electronic scanning switch circuit arrangement which provides time-shared energisation of said segment electrodes by energising pulses; means for detecting the number of segment electrodes to be energised to produce from a multi-segment numeric element in the display the display of a particular numeral thereby; and means for controlling the energising pulse widths applied to the display segment electrodes in dependence upon the detected number so as to produce substantially the same brightness from any numeral displayed.

The electronic scanning switch circuit arrangement may be connected to receive a plurality of time-representative signals from said time-keeping means and supplies output signals for utilisation by the display under the control of pulsed signals, of high frequency in relation to said time-representative signals, to secure said time-shared energisation. Preferably said pulse signals are derived from said time-keeping means.

The timepiece may include means for selectively driving the display segment electrodes under the control of a numeral select-

ing signal, by translating said numeral selecting signal into a plurality of numeral pulse groups and utilising said pulse groups to drive said electrodes.

5 The invention is illustrated in and further explained in connection with the accompanying drawings in which:—

Figure 1 is a block diagram of one embodiment of the invention;

10 Figure 2 shows one form of LED lighting pulse generating circuit which may be used in the embodiment of Figure 1;

Figures 3 (A) and (B) show output wave forms obtained from the circuit of Figure 2;

15 Figure 4 is a block diagram of a second embodiment;

Figure 5 is an explanatory wave form diagram;

20 Figure 6 is a block diagram of another embodiment of the invention;

Figure 7 shows one form of figure width control pulse generating circuit which can be used in the embodiment of Figure 6; and

25 Figure 8 is another explanatory wave form diagram.

Referring to Figure 1, a time-standard relatively high frequency oscillator, such as a quartz crystal controlled oscillator, is represented at 1. Its oscillations are fed to a frequency divider 2 which produces therefrom a 1Hz output. This is fed to a second counter 3, followed by a minutes counter 4, in turn followed by an hours counter 5. Block 6 is a LED lighting pulse generating circuit for intermittently lighting a LED display. 7 is a timing circuit for controlling the timing of an electronic scanning switch circuit arrangement 8. 9 is a decoder for decoding the output from the circuit arrangement 8, and 10 is a driver circuit driving an LED display 11.

Figure 2 shows the circuitry of the LED lighting pulse generating circuit 6 of Figure 1. In Figure 2, 12 is a clock input terminal. 13a, 13b, 13c, 13d and 13e are D-type flip-flops (FFs), the clock input terminals of which receive clock input from terminal 12. The Q output from the fifth flip-flop stage 13e is applied to the data input terminal D of the first flip-flop stage 13a. The Q outputs (at Q_1 , Q_2 , Q_3 and Q_4) of the flip-flops 13a, 13b, 13c and 13d are respectively applied to the data input terminals D of the following flip-flops 13b, 13c, 13d and 13e.

30 The Q output at Q_5 of the last flip-flop 13e is applied to the one input terminal of a NOR gate 14 to the other input of which is applied the Q output, at Q_1 , of the flip-flop 13a. The two inputs of a NOR gate 15 are respectively fed from the $\bar{Q}$ output of 13a and the Q output at Q_2 of 13b; and the two inputs of a further NOR gate 16 are respectively fed from the $\bar{Q}$ output of

13b and the Q output, at Q_3 , of 13c.

The output from NOR gate 14 is applied to one input of each of three OR gates 17, 18 and 19 of which 18 is a three-input gate, the others being two-input gates. Gate 17 receives its second input gate 15 the output of which is also applied to a second input of gate 18. The remaining inputs of gates 18 and 19 are fed from the output of gate 16. The outputs from the NOR gates 14, 15 and 16 are indicated by the references Q_A , Q_B and Q_C respectively. The terminals referenced 20, 21, 22 and 23 receive respectively the outputs from NOR gate 14 and OR gates 17, 18 and 19.

Figure 3 shows at A the clock pulse at terminal 12 and the wave forms at Q_A , Q_B and Q_C of Figure 2; and at B the wave forms at terminals 20, 21 and 23 of Figure 2, and also how they are constituted. Times, in seconds, are represented in Figure 3 on the assumption that the clock pulse frequency is 0.25Hz.

The signal from the oscillator circuit 1 is divided down by the divider 2 to produce a 1Hz signal which is applied to the seconds counter 3 which produces minute signals. The 1-minute signals are applied to the minutes counter 4 which produces hours signals which are applied to the hours counter 5. The output contents of the seconds, minutes and hours counters 3, 4 and 5 are applied to the electronic scanning switch circuit arrangement 8 where they are time-shared under the control of the output frequency from the timing circuit 7.

The output from the LED lighting pulse generating circuit 6 controls the output of the said timing circuit 7. The time display by the LED display device 11 is obtained via the decoder 9 and driver 10.

For the operation of the LED lighting pulse generating circuit 6 consider Figure 2. The Q output of flip-flop 13e is applied to the data input D of the flip-flop 13a. Therefore, if the $\bar{Q}$ output of 13e is "1" the Q output of flip-flop 13a changes from "0" to "1" when a clock signal is applied thereto. At this time if a clock signal is applied to the block input terminals of the flip-flops 13b to 13e, the conditions of the data input terminals of said flip-flops are maintained at "0" and the Q outputs thereof are at "0".

On the application of a second clock signal at 12, the Q output of flip-flop 13b is changed from "0" to "1" as a result of the changing of the Q output of flip-flop 13a by the preceding (i.e. the first) clock pulse. A similar operation occurs at each successive clock pulse appearing at 12 so that, after five successive clock pulses have been applied, the logic conditions at the Q output terminals (Q_1 to Q_5) are as follows:

Clock Pulse No.	1	2	3	4	5
Output at Q_1	1	1	1	1	1
Output at Q_2	0	1	1	1	1
Output at Q_3	0	1	1	1	1
Output at Q_4	0	0	0	1	1
Output at Q_5	0	0	0	0	1

After the fifth input clock pulse the $\bar{Q}$ output of flip-flop 13e is changed from "1" to "0" and the data input D of flip-flop 13a is changed from "1" to "0". When the sixth clock pulse arrives, the Q output (at Q_1) of the first flip-flop 13a is changed from "1" to "0".

Similar operations continue until 10 clock pulses are fed in when the outputs at all the Q terminals Q_1 to Q_5 becomes "0". The successive states at the terminals Q_1 to Q_5 are as shown below, each pulse re-establishing the states established 5 pulses earlier.

Clock Pulse No.	1	2	3	4	5	6	7	8	9	10	11	12	13
Q_1	1	1	1	1	1	0	0	0	0	0	1	1	1
Q_2	0	1	1	1	1	1	0	0	0	0	0	1	1
Q_3	0	0	1	1	1	1	1	0	0	0	0	0	1
Q_4	0	0	0	1	1	1	1	1	0	0	0	0	0
Q_5	0	0	0	0	1	1	1	1	1	0	0	0	0

As already stated, Figure 3 shows at B the wave forms produced at terminals 20 to 23 of Figure 2 from the wave forms at Q_A , Q_B and Q_C by the OR gates 17, 18, 19 if a 0.25 sec. clock signal (i.e. one of 4Hz frequency) is employed. This clock frequency is taken, as indicated in Figure 1, from a stage of the divider 2. As shown in Figure 3 the output signals at 20, 21, 22 and 23 respectively are Q_A , combination $Q_A + Q_B$, combination $Q_A + Q_B + Q_C$ and combination $Q_A + Q_C$. These outputs are used for causing lighting of the LED display. When signal Q_A is used the LED display is energised for 0.5 second, and de-energised for four seconds: when the signal of $Q_A + Q_B$ is used, the LED display is energised for 1 second and de-energised for 3.5 seconds; when $Q_A + Q_B + Q_C$ is used the display is energised for 1.5 seconds and de-energised for 3 seconds; and when $Q_A + Q_C$ is employed the display is energised twice in succession with a de-energised interval of 0.5 seconds between two successive energised periods and a 3 second interval between the

second of these periods and the next energised period, making a total of 1 second energised and $3\frac{1}{2}$ seconds de-energised in each cycle of operations. Because of the effect of persistence of vision, the appearance of the display to the user is that of a substantially continuous and easily read display. Forms of circuitry other than that shown in Figure 2 and producing times of cyclic operation differing from those produced by the circuit of Figure 2 but capable of providing times of display energisation such as will enable the display to be, in practice, continuously read, may be employed in place of Figure 2.

Figures 4 and 5 show a second embodiment. In Figure 4, 1 is again the time standard oscillator, 2 is a divider giving a 1Hz output and block 33 is a counter group including seconds, minutes and hours counters. 44 is an electronic scanning switch circuit arrangement producing a pair of BCD (Binary Coded Decimal) signals synchronised by a numeral selecting signal and combining a plurality of count outputs. 55 is a

numeral selecting signal generating circuit for generating a signal corresponding with a display numeral and receiving as input a suitably chosen output from the divider 2. Block 66 is a seven segments decoder-driver for generating signals by means of which a digital time display 8 incorporating a plurality of seven-segment numeral displays, as known per se and each capable of displaying any number from 0 to 9, is driven. Block 77 is a numeral selecting signal changing circuit for changing the numeral selecting signal from 55 to a pulse signal of relatively small pulse width. It has two inputs, one from a suitably chosen stage of the divider 2 and the other from the numeral selecting signal generating circuit 55.

The operation of Figure 4 will now be described with the assistance of Figure 5. The relatively high frequency signal, e.g. of 32,768Hz, from oscillator 1 is applied to the divider 2, the output from which is fed to the counter group 33 which produces the BCD signals applied to the circuit arrangement 44. The numeral selecting signal generating circuit 55 which generates pulse signals corresponding with the selected numerals is a ring counter of n -bits. These pulse signals have different respective phases. The input frequency to circuit 55 is chosen to be a frequency high enough to produce no flicker to the human eye. Preferably a frequency of several hundreds Hz is chosen.

The seven segment decoder-driver 66 produces seven signals corresponding to seven segments (a to g) of a seven-segment numeral display. It is driven by the BCD signal applied thereto and changes it, in manner known per se, to seven-segment signals for driving the display 88. The signals of different respective phases and of a frequency higher than that of the input signal to the numeral selecting signal generating circuit 55 are applied to the numeral selecting signal changing circuit 77.

In a conventional known timepiece of the general nature of that shown in Figure 4 the output of the numeral selecting signal generating circuit 55 would be directly applied to the display for operating the same. In Figure 4, on the other hand, the numeral selecting signal changing circuit 77 changes each output of the numeral selecting signal generating circuit 55 to a plurality of pulse signals of higher frequency than the input frequency fed to said numeral selecting signal generating circuit 55. This higher frequency is applied to the input of said numeral selecting signal changing circuit 77 from divider 2. In this way what may be termed AND-operation is attained. For example, if a 256Hz signal is applied to the numeral selecting signal generating circuit 55 a frequency of 2048Hz signal may be applied to the numeral selecting signal changing circuit 77 whereby AND-operation due to a combining effect of said two fre-

quencies is attained. This is illustrated in Figure 5 (for the numerals 1 and 4, taken as examples) from which it will be seen that the numeral selecting pulse is changed into a plurality of narrow pulses the total effective width of which is reduced to about one half of what it would be in a conventional arrangement. Accordingly the periods in which the LED display is energised are reduced with consequent reduction of power consumption to about one half. It is possible to reduce the display energising pulse width to less than one half, e.g. to one quarter or one eighth by suitably chosen AND and OR operation. For example, it is possible to reduce the width of the figure selecting pulse to a quarter by satisfying the following logic equations:—

$$\begin{aligned}\text{Numeral 1} &= Q2048 \cdot \overline{Q1024} \cdot QD1 \\ \text{Numeral 2} &= Q2048 \cdot \overline{Q1024} \cdot QD2\end{aligned}$$

$$\text{Numeral 4} = Q2048 \cdot \overline{Q1024} \cdot QD4$$

The numeral pulse signals corresponding to the various numerals are, of course, applied to the LED display 88 to cause it to display the time in accordance with the segment signals fed to it from the decoder-driver 66. In this way use is made of numeral selecting pulses composed of pulse trains such that the actual display energised time is reduced, and the power consumption correspondingly reduced. The result is increased useful life for the LED display and therefore of the timepiece as a whole, since the display is operated for a reduced overall time. Also, because of the reduced power consumption, a smaller battery can be used than would otherwise be satisfactorily employed and this enables the timepiece to be made smaller—an important matter if the timepiece is a wrist watch. If a little flickering due to the reduction in the width of the numeral selecting pulse is objected to it can be avoided by stepping up the frequency fed from divider 2 to block 77. Although reduction of pulse width to an even integral fraction (one half, one quarter, one eighth) is mentioned above, reduction to an odd integral fraction e.g. one third or one fifth, can obviously be obtained, if preferred.

A third embodiment of the invention will now be described with reference to Figures 6, 7 and 8.

In Figure 6, 1 is again the time standard oscillator, 2 is a divider for producing one-second pulses therefrom. 333 is a counter group for producing seconds, minutes, hours, day and date counts and includes 1/60, 1/12, 1/7 and 1/31 counters. The divider 2 is also used to provide clock pulses (represented as 2048Hz) and to provide a frequency (as shown 256Hz) for a numeral pulse generat-

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ing circuit 777. 444 is an electronic scanning switch circuit arrangement which receives outputs from the counters in the group 333 and also outputs from the numeral pulse generating circuit 777. Block 555 is a decoder for decoding the binary output of the multiplex circuit 444. Block 666 comprises a display driver and LED seven segment numeric displays. The numeral pulse generating circuit 777 receives the 256Hz output from the divider 2. 28 is a numeral control pulse generating circuit which receives the clock input (2048Hz) from the divider 2. Block 99 is a selected segment number control circuit the purpose of which will be clear later, which receives output from the circuit arrangement 444. This control circuit 99 supplies outputs to a width control pulse generating circuit 100 which controls the pulse width of the numeral pulses and is controlled by the output signals from the figure control pulse generating circuit 28. Block 110 is a numeral signal dividing circuit. It receives the same signals as the circuit arrangement 444 from the numeral pulse generating circuit 777 and a signal f_c (the derivation of which will be described later) from the numeral width control pulse generating circuit 100 and supplies its outputs to the terminals D_1 to D_4 of the display driver and display unit 666.

The 32,768Hz signal is applied to the divider 2 which generates a 1Hz signal for the counter group 333, a 256Hz signal for the numeral pulse generating circuit 777 and a 2048Hz clock signal for the numeral control pulse generating circuit 28. The one second pulses from the divider 2 are fed to the counters in the counter group 333 by which time counting is effected and which supplies

BCD outputs to the multiplex circuit 444. The numeral pulse generating circuit 777 to which the 256Hz signal is applied has a number of output terminals. For example, as shown, it may be a 4-bits ring counter providing four differently phased outputs which are applied to the multiplex circuit 444. The multiplex circuit 444 changes the plurality of BCD input signals from counter group 333 into BCD signals Q_A , Q_B , Q_C and Q_D which are applied to the terminals so referenced in the decoder 555. This decoder has seven outputs which are applied to the seven numeral segment terminals a to g of the driver-display unit 666. The BCD signals from the circuit arrangement 444 are also applied to the selected segment number control circuit 99.

In order to obtain equal overall brightness from any displayed numeral it is necessary to control the energisation of the segments energised to produce a numeral in accordance with the number of segments energised to produce that numeral. This is shown by the following Table I. In this table the top line shows the numerals (0 to 9) which can be displayed by a seven-segment display, the left-hand column (a to g) identifies the segment in the display, the "1" entries signify the segments energised and the "0" entries signify segments not energised. Thus, to produce the numeral 3, five segments are energised and two are not. The bottom row shows the ratio of energisation required in each case, to the energisation required when a minimum number of segments is energised, in order to produce equal brightness from any numeral. Thus, for the numeral 3 the ratio is 5 to 1.

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TABLE I

		DISPLAY									
		0	1	2	3	4	5	6	7	8	9
S.	a	1	0	1	1	0	1	1	1	1	1
E.	b	1	1	1	1	1	0	0	1	1	1
G	c	1	1	0	1	1	1	1	1	1	1
M	d	1	0	1	1	0	1	1	0	1	1
E.	e	1	0	1	0	0	0	1	0	1	0
N	f	1	0	0	0	1	1	1	0	1	1
T	g	0	0	1	1	1	1	1	0	1	1
Number of segments energised		6	2	5	5	4	5	6	3	7	6
Ratio to minimum number of segments		3.0	1	2.5	2.5	2.0	2.5	3.0	1.5	3.5	3.0

From Table I it will be seen that there is an energisation difference of 3.5 times required between the display of numeral 1 (which has the smallest number of segments energised) and the display of numeral 8 (which has the largest number of segments energised) in order to obtain equal overall

brightness with both these numerals. An acceptably close approximation to the theoretical requirement can be obtained by dividing the possible different numbers of segments energised (1 to 7) for any numeral into three groups as follows:—

TABLE II

	Numerals displayed	Number of segments energised
Group 1	1, 7	2 or 3
Group 2	2, 3, 4, 5	4 or 5
Group 3	0, 6, 8, 9	6 or 7

The BCD outputs required from the multiplex circuit 444 to display the numerals 0 to 9 are shown by Table III.

(15)

TABLE III

Numeral	Q_D	Q_C	Q_B	Q_A	Logic Formula
0	0	0	0	0	$f_0 = \bar{Q}_A \bar{Q}_B \bar{Q}_C \bar{Q}_D$
1	0	0	0	1	$f_1 = Q_A \bar{Q}_B \bar{Q}_C \bar{Q}_D$
2	0	0	1	0	$f_2 = \bar{Q}_A Q_B \bar{Q}_C \bar{Q}_D$
3	0	0	1	1	$f_3 = Q_A Q_B \bar{Q}_C \bar{Q}_D$
4	0	1	0	0	$f_4 = \bar{Q}_A \bar{Q}_B Q_C \bar{Q}_D$
5	0	1	0	1	$f_5 = Q_A \bar{Q}_B Q_C \bar{Q}_D$
6	0	1	1	0	$f_6 = \bar{Q}_A Q_B Q_C \bar{Q}_D$
7	0	1	1	1	$f_7 = Q_A Q_B Q_C \bar{Q}_D$
8	1	0	0	0	$f_8 = \bar{Q}_A \bar{Q}_B \bar{Q}_C Q_D$
9	1	0	0	1	$f_9 = Q_A \bar{Q}_B \bar{Q}_C Q_D$

From this it will be seen that the numerals in Group 1 are covered by $f_1 + f_7$ in this table; those in Group 2 are covered by $f_2 + f_3 + f_4 + f_5$ and those in Group 3 are covered by $f_6 + f_7 + f_8 + f_9$. Thus:

$$Q_1 = f_1 + f_7 = Q_A \bar{Q}_B \bar{Q}_C \bar{Q}_D + Q_A Q_B Q_C \bar{Q}_D \quad (\text{Group 1})$$

$$Q_2 = f_2 + f_3 + f_4 + f_5 = Q_B \bar{Q}_C \bar{Q}_D + \bar{Q}_B Q_C \bar{Q}_D \quad (\text{Group 2})$$

$$Q_3 = f_6 + f_7 + f_8 + f_9 = \bar{Q}_A Q_B Q_C \bar{Q}_D + Q_A \bar{Q}_B \bar{Q}_C + \bar{Q}_B \bar{Q}_C Q_D \quad (\text{Group 3})$$

5 The above combinations, satisfying the division into three groups as above, are achieved by the selected segment number control circuit 99. The control pulse generating circuit 28 receives the 2048Hz signal from divider 2 as a clock input signal and provides therefrom eight inverted output signals $\bar{T}_1$ to $\bar{T}_8$ of different phases. The pulse width of the outputs $\bar{T}_1$ to $\bar{T}_8$ are at most equal to and preferably less than the numeral pulse width from the numeral pulse generating circuit 777. The said control pulse generating circuit 28 may be, for example, an 8-bit counting ring counter and supplies its

outputs to the width control pulse generating circuit 100 which also receives the Q_1 , Q_2 and Q_3 outputs from the selected segment control circuit 99. At any given time one of the outputs $\bar{T}_1$ to $\bar{T}_8$ from 28 and one of the outputs Q_1 to Q_3 from 99 are applied to the numeral width control pulse generating circuit 100.

Suitable circuitry for the numeral width control pulse generating circuit 100 is shown in Figure 7.

The output Q_3 from the circuit 99 is applied to the input terminal of an inverter 121; the output Q_2 from said circuit is applied

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to one input of a NAND gate 122; and the output Q_1 from 99 is applied to one input of another NAND gate 123. The output signal $\bar{f}_1$ from circuit 28 is applied to the remaining input of NAND gate 122 and the signals $\bar{f}_2$ and $\bar{f}_3$ from circuit 28 are applied to the respective inputs of a further NAND gate 124, the output from which is fed through an inverter 126 to the remaining input of gate 123. The outputs of the NAND gates 121, 122 and 123 are connected to the respective inputs of a three-input NAND gate 125 from which an output f_0 is obtained.

The wave forms occurring in Figure 7 are shown in Figure 8. The signal Q_3 applied to the inverter 121 is a signal falling in Group 3 as defined above and this, inverted as shown at D_1 in Figure 8, is applied to one input of gate 125. When the fourth pulse $\bar{f}_4$ appears the Q_3 signal, which is a Group 2 signal, is "1" so that the output signal from gate 122 is applied to the second input of the NAND gate 125. This wave form is shown at D_2 in Figure 8. NAND gate 123 is opened when the Q_1 signal is "1", and the third and fifth pulses $\bar{f}_3$ and $\bar{f}_5$ appear and the resulting signal is shown at D_3 in Figure 8. The gate 125 produces an output f_0 as indicated in Figure 8 which also shows, in separate lines, the outputs from the gates 121, 122, 123. The outputs from the circuit 777 and the output f_0 from circuit 100 are applied to said numeral signal dividing circuit 110 which divides the numeral signals and applies them to the display driver in block 666. The signals applied to the terminals D_1 , D_2 , D_3 and D_4 of the display driver are shown by lines Q_{D1} , Q_{D2} , Q_{D3} and Q_{D4} respectively of Figure 8.

In this way, as will now be seen, the number of segments energised to produce a numeral to be displayed at any time is detected, the resultant classified in groups and the time of energisation of the display LEDs correspondingly controlled in such manner as to achieve a good approximation to uniform overall brightness or lighting no matter how many segments have to be lit to produce the numeral in question. Despite the substantial reduction achieved in power consumption, due to the relatively long periods in which display segments are not energised, the resultant display is satisfactory, appearing (due to persistence of vision) substantially continuous and with no noticeable flutter and having substantially the same total illumination for all numerals displayed.

WHAT WE CLAIM IS:—

1. An electronic timepiece having an LED digital time display and timekeeping means providing time-representative signals for operating said display wherein the digital display segment electrodes in said display are operated by said signals in time-shared manner by means including an electronic scanning switch circuit arrangement which provides time-shared energisation of said segment electrodes by energising pulses; means for detecting the number of segment electrodes to be energised to produce from a multi-segment numeric element in the display the display of a particular numeral thereby; and means for controlling the energising pulse widths applied to the display segment electrodes in dependence upon the detected number so as to produce substantially the same brightness from any numeral displayed.

2. A timepiece as claimed in claim 1 wherein said electronic scanning switch circuit arrangement is connected to receive a plurality of time-representative signals from said time-keeping means and supplies output signals for utilisation by the display under the control of pulsed signals, of high frequency in relation to said time-representative signals, to secure said time-shared energisation.

3. A timepiece as claimed in claim 2 wherein said pulsed signals are derived from said time-keeping means.

4. A timepiece as claimed in claim 1 and including means for selectively driving the display segment electrodes under the control of a numeral selecting signal, by translating said numeral selecting signal into a plurality of numeral pulse groups and utilising said pulse groups to drive said electrodes.

5. An electronic timepiece substantially as herein described with reference to Figures 1, 2 and 3 of the accompanying drawings.

6. An electronic timepiece substantially as herein described with reference to Figures 4 and 5 of the accompanying drawings.

7. An electronic timepiece substantially as herein described with reference to Figures 6, 7 and 8 of the accompanying drawings.

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to one input of a NAND gate 122; and the output Q_1 from 99 is applied to one input of another NAND gate 123. The output signal $\bar{t}_1$ from circuit 28 is applied to the remaining input of NAND gate 122 and the signals $\bar{t}_3$ and $\bar{t}_5$ from circuit 28 are applied to the respective inputs of a further NAND gate 124, the output from which is fed through an inverter 126 to the remaining input of gate 123. The outputs of the NAND gates 121, 122 and 123 are connected to the respective inputs of a three-input NAND gate 125 from which an output f_0 is obtained.

The wave forms occurring in Figure 7 are shown in Figure 8. The signal Q_3 applied to the inverter 121 is a signal falling in Group 3 as defined above and this, inverted as shown at D_1 in Figure 8, is applied to one input of gate 125. When the fourth pulse $\bar{t}_4$ appears the Q_2 signal, which is a Group 2 signal, is "1" so that the output signal from gate 122 is applied to the second input of the NAND gate 125. This wave form is shown at D_2 in Figure 8. NAND gate 123 is opened when the Q_1 signal is "1", and the third and fifth pulses $\bar{t}_3$ and $\bar{t}_5$ appear and the resulting signal is shown at D_3 in Figure 8. The gate 125 produces an output f_0 as indicated in Figure 8 which also shows, in separate lines, the outputs from the gates 121, 122, 123. The outputs from the circuit 777 and the output f_0 from circuit 100 are applied to said numeral signal dividing circuit 110 which divides the numeral signals and applies them to the display driver in block 666. The signals applied to the terminals D_1 , D_2 , D_3 and D_4 of the display driver are shown by lines Q_{D1} , Q_{D2} , Q_{D3} and Q_{D4} respectively of Figure 8.

In this way, as will now be seen, the number of segments energised to produce a numeral to be displayed at any time is detected, the resultant classified in groups and the time of energisation of the display LEDs correspondingly controlled in such manner as to achieve a good approximation to uniform overall brightness or lighting no matter how many segments have to be lit to produce the numeral in question. Despite the substantial reduction achieved in power consumption, due to the relatively long periods in which display segments are not energised, the resultant display is satisfactory, appearing (due to persistence of vision) substantially continuous and with no noticeable flutter and having substantially the same total illumination for all numerals displayed.

WHAT WE CLAIM IS:—

1. An electronic timepiece having an LED digital time display and timekeeping means providing time-representative signals for operating said display wherein the digital display segment electrodes in said display are operated by said signals in time-shared manner by means including an electronic scanning switch circuit arrangement which provides time-shared energisation of said segment electrodes by energising pulses; means for detecting the number of segment electrodes to be energised to produce from a multi-segment numeric element in the display the display of a particular numeral thereby; and means for controlling the energising pulse widths applied to the display segment electrodes in dependence upon the detected number so as to produce substantially the same brightness from any numeral displayed.

2. A timepiece as claimed in claim 1 wherein said electronic scanning switch circuit arrangement is connected to receive a plurality of time-representative signals from said time-keeping means and supplies output signals for utilisation by the display under the control of pulsed signals, of high frequency in relation to said time-representative signals, to secure said time-shared energisation.

3. A timepiece as claimed in claim 2 wherein said pulsed signals are derived from said time-keeping means.

4. A timepiece as claimed in claim 1 and including means for selectively driving the display segment electrodes under the control of a numeral selecting signal, by translating said numeral selecting signal into a plurality of numeral pulse groups and utilising said pulse groups to drive said electrodes.

5. An electronic timepiece substantially as herein described with reference to Figures 1, 2 and 3 of the accompanying drawings.

6. An electronic timepiece substantially as herein described with reference to Figures 4 and 5 of the accompanying drawings.

7. An electronic timepiece substantially as herein described with reference to Figures 6, 7 and 8 of the accompanying drawings.

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