CLAIMS:

1. An integrated circuit structure, comprising:

a plurality of first interconnects;

a memory component embedded in and electrically connected to the plurality of first interconnects;

a device layer above the plurality of first interconnects, the device layer comprising a device electrically connected to the memory component;

a plurality of second interconnects above the device layer, wherein the plurality of second interconnects is electrically connected to the device of the device layer; and

a plurality of external contact points above plurality of second interconnects, the plurality of external contact points electrically connected to the plurality of second interconnects.

2. The integrated circuit structure of claim 1, wherein the plurality of first interconnects comprise finer pitch interconnects than the plurality of second interconnects.

3. The integrated circuit structure of claim 1, wherein the device gates the memory component to the plurality of second interconnects.

4. The integrated circuit structure of claim 1, wherein the plurality of first interconnects comprise finer pitch interconnects than the plurality of second interconnects, and wherein the device gates the memory component to the plurality of second interconnects.

5. The integrated circuit structure of claim 1, wherein the memory component is a ReRAM component.

6. The integrated circuit structure of claim 1, wherein the memory component is an MRAM component.

7. The integrated circuit structure of claim 1, wherein the memory component is a STT-MRAM component.

8. The integrated circuit structure of claim 1, wherein the device is a FinFET device.

9. A system, comprising:

a board;

a communications chip coupled to the board; and

an integrated circuit structure coupled to the board, the integrated circuit structure comprising:

a plurality of first interconnects;

a memory component embedded in and electrically connected to the plurality of first interconnects;

a device layer above the plurality of first interconnects, the device layer comprising a device electrically connected to the memory component;

a plurality of second interconnects above the device layer, wherein the plurality of second interconnects is electrically connected to the device of the device layer; and

a plurality of external contact points above plurality of second interconnects, the plurality of external contact points electrically connected to the plurality of second interconnects.

10. The system of claim 9, further comprising:

a volatile memory coupled to the board.

11. The system of claim 9, further comprising:

a non-volatile memory coupled to the board.

12. The system of claim 9, further comprising:

a graphics processing unit coupled to the board.

13. The system of claim 9, further comprising:

a digital signal processor coupled to the board.

14. The system of claim 9, further comprising:

a crypto processor coupled to the board.

15. The system of claim 9, further comprising:

a chipset coupled to the board.

16. The system of claim 9, further comprising:

an antenna coupled to the board.

17. The system of claim 9, further comprising:

a display coupled to the board.

18. The system of claim 9, further comprising:

a battery coupled to the board.

19. The system of claim 9, further comprising:

a global positioning system coupled to the board.

20. The system of claim 9, further comprising:

a camera coupled to the board.