CLAIMS

What is claimed is:

1. A semiconductor device comprising a memory array, the memory array comprising a stack of conductive tiers and a stair step structure between first and second portions of the memory array, wherein the stair step structure comprises contact regions for respective conductive tiers of the stack of conductive tiers, and wherein:

the first portion of the memory array comprises a first plurality of select gates, wherein each select gate of the first plurality of select gates extends in a particular direction over the stack of conductive tiers; and

the second portion of the memory array comprises a second plurality of select gates, wherein each select gate of the second plurality of select gates also extends in the particular direction over the stack of conductive tiers.

2. The semiconductor device of claim 1, wherein the contact regions of the stair step structure are aligned in the particular direction.

3. The semiconductor device of claim 1, wherein the first and second pluralities of select gates each have a collective width in another direction that is orthogonal to the particular direction, and wherein the width of the stair step structure in the another direction is less than the collective width.

4. The semiconductor device of claim 1, wherein the contact regions of the stair step structure comprise contact regions for less than all of the conductive tiers of the stack of conductive tiers.

5. The semiconductor device of claim 4, wherein the stair step structure comprises a first stair step structure and the contact regions comprise first contact regions for a first plurality of conductive tiers of the stack of conductive tiers, the semiconductor device further comprising a second stair step structure between the second portion of the memory array and a third portion of the memory array, wherein the second stair step structure comprises second contact regions for a second plurality of conductive tiers of the stack of conductive tiers.

6. The semiconductor device of claim 5, wherein each select gate of the first plurality of select gates is coupled to a respective select gate of the second plurality of select gates.

7. The semiconductor device of claim 5, wherein the third portion of the memory array comprises a third plurality of select gates, wherein each select gate of the third plurality of select gates also extends in the particular direction over the stack of conductive tiers.

8. The semiconductor device of claim 7, wherein each select gate of the first plurality of select gates is coupled to a respective select gate of the second plurality of select gates, and wherein each select gate of the second plurality of select gates is coupled to a respective select gate of the third plurality of select gates.

9. The semiconductor device of claim 5, further comprising a third stair step structure between the third portion of the memory array and a fourth portion of the memory array, wherein the third stair step structure comprises third contact regions for a third plurality of conductive tiers of the stack of conductive tiers.

10. The semiconductor device of claim 9, further comprising:

a first control unit under the first portion of the memory array and coupled to a first portion of the first plurality of conductive tiers;

a second control unit under the second portion of the memory array and coupled to a second portion of the first plurality of conductive tiers;

a third control unit under the second portion of the memory array and coupled to a first portion of the second plurality of conductive tiers ;

a fourth control unit under the third portion of the memory array and coupled to a second portion of the second plurality of conductive tiers;

a fifth control unit under the third portion of the memory array and coupled to a first portion of the third plurality of conductive tiers; and

a sixth control unit under the fourth portion of the memory array and coupled to a second portion of the third plurality of conductive tiers.

11. The semiconductor device of claim 10, wherein each of the first control unit, the second control unit, the third control unit, the fourth control unit, the fifth control unit, and the sixth control unit comprises pass gates.

12. The semiconductor device of claim 9, further comprising a fourth stair step structure between the fourth portion of the memory array and a fifth portion of the memory array, wherein the fourth stair step structure comprises fourth contact regions for a fourth plurality of conductive tiers of the stack of conductive tiers.

13. The semiconductor device of any one of claims 1 through 6, wherein the memory array comprises a memory array block comprising sub-blocks, wherein each of the sub-blocks corresponds to a respective select gate of the first plurality of select gates and a respective select gate of the second plurality of select gates, and wherein the first portion of the memory array further comprises a first plurality of vertical strings of memory cells and wherein the second portion of the memory array further comprises a second plurality of vertical strings of memory cells.

14. The semiconductor device of any one of claims 1 through 6, further comprising:

a first plurality of data lines over the first plurality of select gates, wherein each data line of the first plurality of data lines extends in another direction that is orthogonal to the particular direction; and

a second plurality of data lines over the second plurality of select gates, wherein each data line of the second plurality of data lines also extends in the another direction,

wherein the first plurality of select gates comprise control gates of first select transistors coupled to the first plurality of data lines, and wherein the second plurality of select gates comprise control gates of second select transistors coupled to the second plurality of data lines.

15. A method of forming a semiconductor device structure, the method comprising:

forming a stack of alternating conductive plates and insulating materials;

patterning the stack of alternating conductive plates and insulating materials to form at least one elongated memory array block; and

forming one or more stair step structures between longitudinal ends of the at least one elongated memory array block and between lateral side surfaces of the at least one elongated memory array block to define contact regions of respective conductive plates of the stack of alternating conductive plates and insulating materials.

16. The method of claim 15, wherein forming one or more stair step structures between lateral side surfaces of the at least one elongated memory array block comprises forming the one or more stair step structures along one of the lateral side surfaces of the at least one memory array block.

17. The method of claim 15, further comprising laterally recessing the one or more stair step structures from a plane defined by one of the lateral side surfaces of the at least one memory array block.

18. The method of claim 15, further comprising electrically coupling access lines to respective contact regions defined by the one or more stair step structures.

19. The method of claim 18, further comprising forming the access lines to have a distance between adjacent access lines of at least about 100 nm.

20. The method of any one of claims 15 through 19, wherein:

forming a stack of alternating conductive plates and insulating materials comprises forming at least 32 conductive plates; and

patterning the stack of alternating conductive plates and insulating materials to form at least one elongated memory array block comprises forming the at least one elongated memory array block to have a lateral width of about 5 μm or less.

What is claimed is:

1. A semiconductor device comprising a memory array block, the memory array block comprising a stack of continuous conductive tiers and a stair step structure between first and second portions of the memory array block, wherein the stair step structure comprises contact regions for respective conductive tiers of the stack of continuous conductive tiers, and wherein:

the first portion of the memory array block comprises a first plurality of select gates, wherein each select gate of the first plurality of select gates extends in a particular direction over the stack of continuous conductive tiers; and

the second portion of the memory array block comprises a second plurality of select gates, wherein each select gate of the second plurality of select gates also extends in the particular direction over the stack of continuous conductive tiers.

2. The semiconductor device of claim 1, wherein the contact regions of the stair step structure are aligned in the particular direction.

3. The semiconductor device of claim 1, wherein the first and second pluralities of select gates each have a collective width in another direction that is orthogonal to the particular direction, and wherein the width of the stair step structure in the another direction is less than the collective width.

4. The semiconductor device of claim 1, wherein the contact regions of the stair step structure comprise contact regions for less than all of the conductive tiers of the stack of continuous conductive tiers.

5. The semiconductor device of claim 4, wherein the stair step structure comprises a first stair step structure and the contact regions comprise first contact regions for a first plurality of conductive tiers of the stack of continuous conductive tiers, the semiconductor device further comprising a second stair step structure between the second portion of the memory array block and a third portion of the memory array block, wherein the second stair step structure comprises second contact regions for a second plurality of conductive tiers of the stack of continuous conductive tiers.

6. The semiconductor device of claim 5, wherein each select gate of the first plurality of select gates is coupled to a respective select gate of the second plurality of select gates.

7. The semiconductor device of claim 5, wherein the third portion of the memory array block comprises a third plurality of select gates, wherein each select gate of the third plurality of select gates also extends in the particular direction over the stack of continuous conductive tiers.

8. The semiconductor device of claim 7, wherein each select gate of the first plurality of select gates is coupled to a respective select gate of the second plurality of select gates, and wherein each select gate of the second plurality of select gates is coupled to a respective select gate of the third plurality of select gates.

9. The semiconductor device of claim 5, further comprising a third stair step structure between the third portion of the memory array and a fourth portion of the memory array block, wherein the third stair step structure comprises third contact regions for a third plurality of conductive tiers of the stack of continuous conductive tiers.

10. The semiconductor device of claim 9, further comprising:

a first control unit under the first portion of the memory array block and coupled to a first portion of the first plurality of conductive tiers;

a second control unit under the second portion of the memory array block and coupled to a second portion of the first plurality of conductive tiers;

a third control unit under the second portion of the memory array block and coupled to a first portion of the second plurality of conductive tiers;

a fourth control unit under the third portion of the memory array block and coupled to a second portion of the second plurality of conductive tiers;

a fifth control unit under the third portion of the memory array block and coupled to a first portion of the third plurality of conductive tiers; and

a sixth control unit under the fourth portion of the memory array block and coupled to a second portion of the third plurality of conductive tiers.

11. The semiconductor device of claim 10, wherein each of the first control unit, the second control unit, the third control unit, the fourth control unit, the fifth control unit, and the sixth control unit comprises pass gates.

12. The semiconductor device of claim 9, further comprising a fourth stair step structure between the fourth portion of the memory array block and a fifth portion of the memory array block, wherein the fourth stair step structure comprises fourth contact regions for a fourth plurality of conductive tiers of the stack of continuous conductive tiers.

13. The semiconductor device of any one of claims 1 through 6, wherein the memory array block comprises sub-blocks, wherein each of the sub-blocks corresponds to a respective select gate of the first plurality of select gates and a respective select gate of the second plurality of select gates, and wherein the first portion of the memory array block further comprises a first plurality of vertical strings of memory cells and wherein the second portion of the memory array block further comprises a second plurality of vertical strings of memory cells.

14. The semiconductor device of any one of claims 1 through 6, further comprising:

a first plurality of data lines over the first plurality of select gates, wherein each data line of the first plurality of data lines extends in another direction that is orthogonal to the particular direction; and

a second plurality of data lines over the second plurality of select gates, wherein each data line of the second plurality of data lines also extends in the another direction,

wherein the first plurality of select gates comprise control gates of first select transistors coupled to the first plurality of data lines, and wherein the second plurality of select gates comprise control gates of second select transistors coupled to the second plurality of data lines.

15. A semiconductor device, comprising a memory array block defined by an elongated stack of continuous conductive tiers, the memory array block comprising a stair step structure positioned between longitudinal ends of the memory array block, the stair step structure defining contact regions for electrically contacting respective conductive tiers of the elongated stack of continuous conductive tiers, wherein the stair step structure is positioned longitudinally between a first portion of vertical strings of memory cells of the memory array block and a second portion of vertical strings of memory cells of the memory array block.

16. The semiconductor device of claim 15, wherein the vertical strings of memory cells of the first portion of vertical strings of memory cells of the memory array block and the second portion of vertical strings of memory cells of the memory array block extend through the elongated stack of continuous conductive tiers.

17. The semiconductor device of claim 15, wherein each of the longitudinal ends of the memory array block lacks a stair step structure.

18. The semiconductor device of claim 15, wherein the memory array block comprises longitudinally adjacent alternating memory array regions respectively including the first portion of vertical strings of memory cells and the second portion of vertical strings of memory cells and a stair step region free of vertical strings of memory cells.

19. The semiconductor device of claim 15, wherein the memory array block includes more than one stair step structure.

20. The semiconductor device of claim 19, wherein each stair step structure of the more than one stair step structure defines a contact region for a portion of the conductive tiers of the elongated stack of continuous conductive tiers.

21. The semiconductor device of claim 15, wherein the stair step structure extends laterally only partially across a lateral width of the memory array block.

22. A semiconductor device structure including a three-dimensional memory array, the semiconductor device structure comprising:

elongated memory array blocks laterally adjacent to one another, each of the memory array blocks comprising:

a vertical stack of horizontal conductive tiers separated by electrically insulating material;

a stair step structure defined by portions of the conductive tiers, the stair step structure positioned along a lateral side of the memory array block and between opposing lateral side surfaces of the memory array block for providing electrical access to respective conductive tiers of the vertical stack of horizontal conductive tiers; and

electrically conductive access lines electrically coupling respective conductive tiers of the stair step structure to at least one control unit positioned under the vertical stack of horizontal conductive tiers.

23. The semiconductor device structure of claim 22, wherein each of the electrically conductive access lines comprises a laterally outer vertical portion, a horizontal portion, and a laterally inner vertical portion, the laterally inner vertical portion coupled to a respective conductive tier of the stair step structure.

24. The semiconductor device structure of claim 23, wherein the laterally outer vertical portions of each of the electrically conductive access lines are aligned in a plane that is parallel to a plane defined by the lateral side of the memory array block.

25. The semiconductor device structure of claim 22, wherein adjacent electrically conductive access lines of the electrically conductive access lines are separated by a distance of less than 100 nm.

26. A semiconductor device comprising:

a three-dimensional memory array block elongated in a horizontal direction, the three-dimensional memory array block comprising:

a vertical stack of conductive tiers;

a lateral side surface; and

a stair step structure including contact regions of at least some of the conductive tiers of the vertical stack of conductive tiers, the stair step structure recessed from the lateral side surface of the three-dimensional memory array block, wherein a portion of the vertical stack of conductive tiers laterally adjacent the stair step structure is free of a stair step structure.

27. The semiconductor device of claim 26, further comprising access lines coupled to the contact regions of the stair step structure, the access lines including vertical portions extending from a location under the vertical stack of conductive tiers and along the recessed stair step structure.

28. The semiconductor device of claim 27, wherein the access lines are positioned between a plane defined by the lateral side surface of the three-dimensional memory array block and the stair step structure.

29. The semiconductor device of claim 26, wherein respective tiers of the vertical stack of conductive tiers on opposing sides of the stair step structure are continuous.