

【DESCRIPTION】**【Invention Title】**

SMALL-AREA SYMBOL TIMING-OFFSET SYNCHRONIZER AND DESIGN
5 METHOD FOR SAME

【Technical Field】

The present invention relates to a symbol timing offset synchronizer having a low-area structure and a design method
10 thereof. More specifically, the invention relates to a symbol timing offset synchronizer having a low-area structure in the symbol timing offset synchronizer of IEEE 802.11a WLAN of an OFDM communication method, and a design method thereof.

15 【Background Art】

The basic principle of the Orthogonal Frequency Division Multiplexing (OFDM) method is dividing a data stream of a high-speed transmission rate into a plurality of data streams of a low-speed transmission rate and simultaneously
20 transmitting the low-speed data streams on a plurality of sub-carriers. That is, OFDM is regarded as a special form of a multi-carrier transmission scheme in which a data stream is simultaneously transmitted on a plurality of sub-channels in parallel. Accordingly, the OFDM technique is a
25 "multiplexing" technique in that a high-speed source data stream of one channel is simultaneously transmitted on multiple channels, and the OFDM technique is a "modulation" technique in that a high-speed source data stream of one channel is divided and transmitted on multiple sub-carriers.
30 Waveforms of the sub-carriers are orthogonal on the time axis, but overlapped on the frequency axis.

Recently, such an OFDM modulation method is widely used

in a variety of wired and wireless data transmission systems. The OFDM system efficiently uses frequencies compared with existing single carrier transmission methods, solves the problem of inter symbol interference using a plurality of
5 sub-carriers in an orthogonal relation, and obtains superior performance even in a multi-path fading environment using a guard intervals.

However, the OFDM modulation method is weak to a synchronization algorithm. That is, a carrier frequency
10 offset occurred due to carrier frequency mismatch of a transmitter and a receiver generates inter-carrier interference, and thus synchronization of OFDM symbols is not accurately obtained. Therefore, interference occurs among the symbols, and system performance is degraded.

15 Accordingly, symbol timing synchronization of a signal is extremely important in order to correctly demodulate signals of the OFDM scheme. High-speed data transmission generates a multi-path delay more than tens of times as high as a clock cycle in an indoor wireless environment. A symbol
20 timing offset is generated due to the uncertainty of a symbol arrival time caused by the multi-path delay and difference in sampling frequencies of transmitting and receiving ends. The symbol timing offset rotates phases of sub-carrier signals and generates a synchronization error of the FFT (Fast
25 Fourier Transform) window position, and thus causes inter-symbol interference. Like this, since the symbol synchronization error greatly decreases system performance, symbol timing offset synchronization of the transmitting and receiving ends should be performed before the receiving end
30 of the OFDM system executes a frequency offset synchronization block.

【Disclosure】**【Technical Problem】**

Accordingly, the present invention has been made in order to solve the above problems, and it is an object of the invention to provide a symbol timing offset synchronizer having a low-area structure in the symbol timing offset synchronizer of IEEE 802.11a WLAN of an OFDM communication method, and a design method thereof.

10 【Technical Solution】

In order to accomplish the above objects of the invention, according to one aspect of the invention, there is provided a symbol timing offset synchronizer for converting a direct form filter structure into a transposed direct form filter structure, and converting filter coefficients of the transposed direct form filter structure into coefficients of the canonic signed digit (CSD) form, in which the filter structure is re-designed based on the CSD form coefficients.

Preferably, training symbols of the transposed direct form filter structure are expressed in a 2's complement form, and then the 2's complement form is converted into the CSD form.

Here, the transposed direct form filter structure may comprise four filters of $r_1(n)$, $r_2(n)$, $i_1(n)$, and $i_2(n)$ (here, r denotes a real number (real), and i denotes an imaginary number (image)).

In this case, $r_1(n)$ and $i_1(n)$ may be the same filter, and $r_2(n)$ and $i_2(n)$ are the same filter.

According to another aspect of the invention, there is provided a method of designing a symbol timing offset synchronizer, the method comprising the steps of: converting a direct form filter structure into a transposed direct form

filter structure; converting a filter coefficient of the transposed direct form filter structure into coefficients of the CSD form; and re-designing the filter structure based on the CSD form coefficients.

5 Preferably, the method of designing a symbol timing offset synchronizer further comprises the step of expressing training symbols of the transposed direct form filter structure in a 2's complement form, and symbols expressed in the 2's complement form may be converted into the CSD form.

10 Here, the transposed direct form filter structure may comprise four filters of $r_1(n)$, $r_2(n)$, $i_1(n)$, and $i_2(n)$ (here, r denotes a real number (real), and i denotes an imaginary number (image)).

In this case, $r_1(n)$ and $i_1(n)$ may be the same filter, and
15 $r_2(n)$ and $i_2(n)$ are the same filter.

【Advantageous Effects】

According to an embodiment of the present invention, an adder of the symbol timing offset synchronizer is designed as
20 a concept of a filter. The adder is converted into a transposed direct form structure in the first stage, and then filter coefficients are converted into a CSD form filter in the second stage, and thus a structure of a low-area symbol timing offset synchronizer can be obtained.

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【Description of Drawings】

FIG. 1 is a view showing a preamble structure used in IEEE 802.11a.

FIG. 2 is a block diagram showing a symbol timing offset
30 synchronizer and a frequency offset synchronizer for WLAN.

FIG. 3 is a view showing the structure of a symbol timing offset synchronizer.

FIG. 4 is a view showing the entire structure of a transposed direct form of a symbol timing offset synchronizer according to an embodiment of the present invention.

FIG. 5 is a view showing the structure of a low-area $r_1(n)$ filter redesigned according to an embodiment of the present invention.

FIG. 6 is a view showing the structure of a low-area $r_2(n)$ filter redesigned according to an embodiment of the present invention.

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【Mode for Invention】

Hereinafter, the preferred embodiments of the present invention will be described in detail with reference to the accompanying drawings.

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In the following detailed description, references are made to the accompanying drawings that show, by way of illustration, specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. It is to be understood that the various embodiments of the invention, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein, in connection with one embodiment, may be implemented within other embodiments without departing from the spirit and scope of the invention. In addition, it is to be understood that the location or arrangement of individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, appropriately

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interpreted, along with the full range of equivalents to which the claims are entitled. In the drawings, like numbers refer to the same or similar functionality throughout the several views.

5 References in the specification to "one embodiment", "an embodiment", "an example embodiment", etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or
10 characteristic. Moreover, such phrases are not necessarily referring to the same embodiment. Further, when a particular feature, structure, or characteristic is described in connection with an embodiment, it is submitted that it is within the knowledge of one skilled in the art to effect such
15 feature, structure, or characteristic in connection with other embodiments whether or not explicitly described.

 A packet constructed at a transmitting end of the WLAN (IEEE 802.11a) OFDM wireless communication scheme includes a preamble, a header, and a payload which is data actually
20 desired to transmit. The structure of the preamble used in IEEE 802.11a has 160 samples of a short training symbol and 160 samples of a long training symbol as shown in FIG. 1.

 Here, the short training symbol is used for signal detection, AGC, diversity selection, timing synchronization,
25 and coarse frequency offset estimation. In addition, the long training symbol is used for channel estimation and fine frequency offset estimation.

 Short training sequences are configured of ten identical symbols from s1 to s10, and each symbol has 16 real number
30 parts and 16 imaginary number parts. In addition, long training sequences are configured of two identical symbols of 11 and 12, and each symbol has 64 real number parts and 64

imaginary number parts.

Symbol timing offset synchronization using the preamble is a work of synchronizing timing and correctly finding a start point of a symbol using a training symbol having a periodic characteristic. Timing of a symbol inputting into the FFT/IFFT block is synchronized by correctly informing the frequency offset synchronizer block of the start time. FIG. 2 shows a block diagram of a symbol timing offset synchronizer and a frequency offset synchronizer for WLAN using a preamble.

As shown in FIG. 2, first, I and Q of the short training symbols of s1 to s7 among the preamble should be inputted into the symbol timing offset synchronizer so as to acquire timing synchronization. The mathematical expression shown below is calculated in order to identify a timing offset.

[Mathematical expression 1]

$$R_n = \left| \sum_{n=0}^{15} Y_n X_{15-n}^* \right|$$

In mathematical expression 1, R_n denotes a correlation value calculated in a cross-correlation method, X_{15-n} denotes the 15-n-th value of the training symbols that the receiver knows in advance, * denotes conjugate, and Y_n denotes a received signal. Cross-correlation values of the received signal are values obtained by complex multiplication of the received signal and 16 samples of the short training symbols. Accordingly, if mathematical expression 1 is consecutively performed on the received signal, the correlation value is greatly increased and shows a peak at a time point where 16 repeated real number and imaginary number samples are ended, and thus symbol timing synchronization can be correctly obtained. The operation on the short training symbols previously known to mathematical expression 1 and the input

signal can be expressed in the mathematical expression shown below.

[Mathematical expression 2]

$$\begin{aligned}
 R_n &= |YX^*| \\
 &= \left| \sum (y_r + jy_i)(x_r - jx_i) \right| \\
 &= \left| \sum (y_r x_r - jy_r x_i + jy_i x_r + y_i x_i) \right| \\
 &= \left| \sum [(y_r x_r + y_i x_i) + j(y_i x_r - y_r x_i)] \right| \\
 &= |r(n) + ji(n)| = \sqrt{r^2(n) + i^2(n)}
 \end{aligned}$$

5 In mathematical expression 2, complex signal X denotes a short training symbol previously known to a receiver, x_r denotes a real number, and x_i denotes an imaginary number. Complex signal Y denotes a received signal, y_r denotes a real number, and y_i denotes an imaginary number. A correlation
 10 value is obtained if mathematical expression 2 is executed, and here, since two real number multiplying operation blocks and two imaginary number multiplying operation blocks are needed, four multiplying operation blocks are needed in total. FIG. 3 shows a structure of a symbol timing offset
 15 synchronizer including the four multiplying operation blocks.

 In the structure of the symbol timing offset synchronizer of FIG. 3, y_r denotes the real number of a received signal, and y_i denotes the imaginary number of the received signal. X_{r0} denotes a value of the 0-th real number
 20 sample of a known training symbol, and there are 16 real number samples in total up to the 15-th real number sample. X_{i0} denotes a value of the 0-th imaginary number sample of the training symbol, and there are 16 imaginary number samples in total up to the 15-th imaginary number sample. A
 25 preamble input value is a complex number, and real number y_r and imaginary number y_i are inputted into relevant multiplier parts respectively. The input signal is inputted into shift register D0 and moves to the next shift register at every

clock. There are 15 shift registers D0 to D14 in total. Each multiplier part performs a multiplying operation on the value inputted into each shift register at every clock using X_r and X_i .

5 The real number multiplying operation block of FIG. 3 calculates an addition of a value of $\Sigma y_r x_r$ and a value of $\Sigma y_i x_i$, and the imaginary number multiplying operation block calculates an addition of a value of $\Sigma y_i x_r$ and a value of $\Sigma y_r x_i$. Since the symbol timing synchronizer shown in FIG. 3
10 uses 64 multipliers, the implementation area increases. Accordingly, it needs to propose a structure that can be implemented in a low-area by efficiently designing a multiplier part in the structure of the symbol timing offset synchronizer of FIG. 3.

15 The structure of the symbol timing offset synchronizer according to an embodiment of the present invention is designed by approaching the symbol timing offset synchronizer as a concept of a filter. If it is approached as a concept of a filter, the synchronizer can be regarded as a filter
20 having 16 filter coefficients of a short training symbol of a preamble. For example, the low-area structure for the structure of FIG. 3 can be accomplished by two stages of a stage of designing a transposed direct form structure (a first stage) and a stage of designing CSD coefficients (a
25 second stage).

If a complex number is inputted at every clock, the symbol timing offset synchronizer using 15 multipliers performs a multiplying operation on the inputted complex number with a short training symbol previously known to the
30 receiver. The multiplier part comprises four parts in total including two real number parts and two imaginary number parts, and a multiplier part has 15 multipliers and 15 shift

registers. Accordingly, 60 multipliers and 60 shift registers are needed in total, and 60 operations are performed at every clock, and thus it is disadvantageous in that the implementation area is increased. Such a
 5 disadvantage can be overcome by implementing the symbol timing offset synchronizer using only adders and shift registers after reducing partial products by converting filter coefficients into the CSD form. In order to use this method, a transposed direct form filter structure is used in
 10 a first stage. For example, a direct form filter structure is used in the structure of the symbol timing offset synchronizer shown in FIG. 3, and this is converted into a transposed direct form filter structure as shown in FIG. 4.

The structure of the symbol timing offset synchronizer
 15 shown in FIG. 4 includes four filters. That is, it includes four filters of $r_1(n)$, $r_2(n)$, $i_1(n)$ and $i_2(n)$. Here, filter $r_1(n)$ and filter $i_1(n)$ are the same filter since they have the same coefficients, and filter $r_2(n)$ and filter $i_2(n)$ are also the same filter since they have the same coefficients.
 20 A low-area can be implemented for filter $r_1(n)$ and filter $r_2(n)$ by converting the filter coefficients into Canonic Signed Digit (CSD) form coefficients.

First, design of a low-area filter structure for the $r_1(n)$ filter is described.

25 In order to implement a low-area structure using adders for the filter structure shown in FIG. 4, coefficients of the filter can be converted into the CSD form. In order to convert coefficients of the filter into the CSD form, training symbols are expressed in the 2's complement form,
 30 and then the 2's complement form is converted into the CSD form. It is because if the filter coefficients are implemented in the CSD form, the number of used adders is

decreased. Table 1 shows real numbers of coefficients used in the filter expressed in the 2's complement form of 16 bits.

[Table 1] 2's complement forms of short training symbols (real) ($r_1(n)$ block)

Training symbol (Real)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0.0460	0	0	0	0	0	1	0	1	1	1	1	0	0	0	1	1
-0.1324	1	1	1	0	1	1	1	1	0	0	0	0	1	1	1	0
-0.0135	1	1	1	1	1	1	1	0	0	1	0	0	0	1	1	0
0.1428	0	0	0	1	0	0	1	0	0	1	0	0	0	1	1	1
0.0920	0	0	0	0	1	0	1	1	1	1	0	0	0	1	1	1
0.1428	0	0	0	1	0	0	1	0	0	1	0	0	0	1	1	1
-0.0135	1	1	1	1	1	1	1	1	0	0	0	0	1	1	1	0
-0.1324	1	1	1	0	1	1	1	1	0	0	0	0	1	1	1	0
0.0460	0	0	0	0	0	1	0	1	1	1	1	0	0	0	1	1
0.0023	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1
-0.0785	1	1	1	1	0	1	0	1	1	1	1	1	0	1	0	0
-0.0127	1	1	1	1	1	1	1	0	0	1	1	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-0.0127	1	1	1	1	1	1	1	0	0	1	1	0	0	0	0	0
-0.0785	1	1	1	1	0	1	0	1	1	1	1	1	0	1	0	0
0.0023	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1

Table 1 shows 2's complement form coefficients and the number of needed adders. The number of 1's in Table 1 is proportional to the number of adders. That is, the number of 1's is proportional to the implementation area. That is, if 2's complement form coefficients are used, the number of needed adders increases since there are relatively a large number of 1's, and thus the implementation area is increased.

Accordingly, in order to reduce the number of adders, the 2's complement form is converted into the CSD form. The

real number and the imaginary number of the short training symbols used as filter coefficients are converted into the CSD form. Table 2 shows 2's complement form coefficients of Table 1 in the CSD form of 16 bits.

5 [Table 2] CSD forms of short training symbols (real)
($r_1(n)$ block)

Training symbol (Real)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0.0460	0	0	0	0	1	0	N	0	0	0	N	0	0	1	0	N
-0.1324	0	0	0	N	0	0	0	N	0	0	0	1	0	0	N	0
-0.0135	0	0	0	0	0	0	N	0	0	1	0	0	1	0	N	0
0.1428	0	0	0	1	0	0	1	0	0	1	0	0	1	0	0	N
0.0920	0	0	0	1	0	N	0	0	0	N	0	0	1	0	0	N
0.1428	0	0	0	1	0	0	1	0	0	1	0	0	1	0	0	N
-0.0135	0	0	0	0	0	0	N	0	0	1	0	0	1	0	N	0
-0.1324	0	0	0	N	0	0	0	N	0	0	0	1	0	0	N	0
0.0460	0	0	0	0	1	0	N	0	0	0	N	0	0	1	0	N
0.0023	0	0	0	0	0	0	0	0	0	1	0	1	0	N	0	N
-0.0785	0	0	0	0	N	0	N	0	0	0	0	N	0	1	0	0
-0.0127	0	0	0	0	0	0	N	0	1	0	N	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-0.0127	0	0	0	0	0	0	N	0	1	0	N	0	0	0	0	0
-0.0785	0	0	0	0	N	0	N	0	0	0	0	N	0	1	0	0
0.0023	0	0	0	0	0	0	0	0	0	1	0	1	0	N	0	N

If filter coefficients of CSD form are used in implementing the $r_1(n)$ filter, the number of adders can be decreased to be smaller than that of 2's complement form structure. The CSD form coefficients of Table 2 are defined and expressed as x_{r0} to x_{r15} in order. Subscript r denotes a real number. Accordingly, table 2 can be expressed as shown in a mathematical expression 3.

[Mathematical expression 3]

$$x_{r0} = a \gg 4 - a \gg 6 - a \gg 10 + a \gg 13 - a \gg 15$$

$$x_{r1} = -a \gg 3 - a \gg 7 + a \gg 11 - a \gg 14$$

$$x_{r2} = -a \gg 6 + a \gg 9 + a \gg 12 - a \gg 14$$

$$5 \quad x_{r3} = a \gg 3 + a \gg 6 + a \gg 9 + a \gg 12 - a \gg 15$$

$$x_{r4} = a \gg 3 - a \gg 5 - a \gg 9 + a \gg 12 - a \gg 15$$

$$x_{r5} = x_{r3}$$

$$x_{r6} = x_{r2}$$

$$x_{r7} = x_{r1}$$

$$10 \quad x_{r8} = x_{r0}$$

$$x_{r9} = a \gg 9 + a \gg 11 - a \gg 13 - a \gg 15$$

$$x_{r10} = -a \gg 4 - a \gg 6 - a \gg 11 + a \gg 13$$

$$x_{r11} = -a \gg 6 + a \gg 8 - a \gg 10$$

$$x_{r13} = x_{r11}$$

$$15 \quad x_{r14} = x_{r10}$$

$$x_{r15} = x_{r9}$$

The $r_1(n)$ filter implementing mathematical expression 3 using adders according to an embodiment of the present invention is as shown in FIG. 5. Referring to FIG. 5, the filter receives signals from the preamble and calculates 15 operation values through shift, add and subtract operations.

Next, design of a low-area filter structure for the $r_2(n)$ filter is described.

2's complement forms of the imaginary numbers of the short training symbols are as shown in Table 3. The value of the imaginary number is the same as a value delayed by eight samples.

[Table 3] 2's complement forms of short training symbols (imaginary) ($r_2(n)$ block)

Training symbol (imaginary)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
-----------------------------------	---	---	---	---	---	---	---	---	---	---	----	----	----	----	----	----

0.0460	0	0	0	0	0	1	0	1	1	1	1	0	0	0	1	1
0.0023	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1
-0.0785	1	1	1	1	0	1	0	1	1	1	1	1	0	1	0	0
-0.0127	1	1	1	1	1	1	1	0	0	1	1	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-0.0127	1	1	1	1	1	1	1	0	0	1	1	0	0	0	0	0
-0.0785	1	1	1	1	0	1	0	1	1	1	1	1	0	1	0	0
0.0023	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1
0.0460	0	0	0	0	0	1	0	1	1	1	1	0	0	0	1	1
-0.1324	1	1	1	0	1	1	1	1	0	0	0	0	1	1	1	0
-0.0135	1	1	1	1	1	1	1	0	0	1	0	0	0	1	1	0
0.1428	0	0	0	1	0	0	1	0	0	1	0	0	0	1	1	1
0.0920	0	0	0	0	1	0	1	1	1	1	0	0	0	1	1	1
0.1428	0	0	0	1	0	0	1	0	0	1	0	0	0	1	1	1
-0.0135	1	1	1	1	1	1	1	0	0	1	0	0	0	1	1	0
-0.1324	1	1	1	0	1	1	1	1	0	0	0	0	1	1	1	0

Table 4 expresses 2's complement forms of imaginary numbers of short training symbols shown in Table 3 in the CSD form.

5 [Table 4] CSD forms of short training symbols (image) ($r_2(n)$ block)

Training symbol (imaginary)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0.0460	0	0	0	0	1	0	N	0	0	0	N	0	0	1	0	N
0.0023	0	0	0	0	0	0	0	0	0	1	0	1	0	N	0	N
-0.0785	0	0	0	0	N	0	N	0	0	0	0	N	0	1	0	0
-0.0127	0	0	0	0	0	0	N	0	1	0	N	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-0.0127	0	0	0	0	0	0	N	0	1	0	N	0	0	0	0	0

-0.0785	0	0	0	0	N	0	N	0	0	0	0	N	0	1	0	0
0.0023	0	0	0	0	0	0	0	0	0	1	0	1	0	N	0	N
0.0460	0	0	0	0	1	0	N	0	0	0	N	0	0	1	0	N
-0.1324	0	0	0	1	0	0	1	0	0	1	0	0	1	0	0	N
-0.0135	0	0	0	0	0	0	N	0	0	1	0	0	1	0	N	0
0.1428	0	0	0	1	0	0	1	0	0	1	0	0	1	0	0	N
0.0920	0	0	0	1	0	N	0	0	0	N	0	0	1	0	0	N
0.1428	0	0	0	1	0	0	1	0	0	1	0	0	1	0	0	N
-0.0135	0	0	0	0	0	0	N	0	0	1	0	0	1	0	N	0
-0.1324	0	0	0	1	0	0	1	0	0	1	0	0	1	0	0	N

Table 4 can be expressed in mathematical expression 4 shown below.

[Mathematical expression 4]

$$x_{r0} = a \gg 4 - a \gg 6 - a \gg 10 + a \gg 13 - a \gg 15$$

$$x_{r1} = a \gg 9 + a \gg 11 - a \gg 13 - a \gg 15$$

$$x_{r2} = -a \gg 4 - a \gg 6 - a \gg 11 + a \gg 13$$

$$x_{r3} = -a \gg 6 + a \gg 8 - a \gg 10$$

$$x_{r5} = x_{r3}$$

$$x_{r6} = x_{r2}$$

$$x_{r7} = x_{r1}$$

$$x_{r8} = x_{r0}$$

$$x_{r9} = -a \gg 3 - a \gg 7 + a \gg 11 - a \gg 14$$

$$x_{r10} = -a \gg 6 + a \gg 9 + a \gg 12 - a \gg 14$$

$$x_{r11} = a \gg 3 + a \gg 6 + a \gg 9 + a \gg 12 - a \gg 15$$

$$x_{r12} = a \gg 3 - a \gg 5 - a \gg 9 + a \gg 12 - a \gg 15$$

$$x_{r13} = x_{r11}$$

$$x_{r14} = x_{r10}$$

$$x_{r15} = x_{r9}$$

If filter $r_2(n)$ is implemented using mathematical expression 4 according to an embodiment of the present invention, it can be expressed as shown in FIG. 6.

In an embodiment of the present invention, a low-area

structure is proposed for a symbol timing offset synchronizer block of IEEE 802.11a WLAN of the OFDM communication method. The adder of the symbol timing offset synchronizer is designed as a concept of a filter. The adder is converted
5 into a transposed direct form structure in the first stage, and then filter coefficients are converted into a CSD form filter in the second stage, and thus the structure of a low-area symbol timing offset synchronizer can be obtained.

The above-described methods can also be embodied as
10 computer programs. Codes and code segments constituting the programs may be easily construed by computer programmers skilled in the art to which the invention pertains. Furthermore, the created programs may be stored in computer-readable recording media or data storage media and may be
15 read out and executed by the computers. Examples of the computer-readable recording media include any computer-readable recording media, e.g., intangible media such as carrier waves, as well as tangible media such as CD or DVD.

Although the present invention has been described with
20 reference to several preferred embodiments, the description is illustrative of the invention and is not to be construed as limiting the invention. Various modifications and variations may occur to those skilled in the art, without departing from the scope of the invention as defined by the
25 appended claims.

【CLAIMS】

【Claim 1】

A symbol timing offset synchronizer for simplifying a direct form filter structure into an eight tap transposed direct form structure and converting eight filter coefficients into a canonic signed digit (CSD) form, wherein

a filter coefficient of the transposed direct form filter structure is converted into coefficients of the CSD form after the direct form filter structure is converted into the transposed direct form filter structure, and the filter structure is re-designed based on the CSD form coefficient, wherein

a packet constructed at a transmitting end of a WLAN (IEEE 802.11a) OFDM wireless communication scheme includes a preamble, a header and a payload which is a data actually desired to transmit, and a structure of the preamble used in the IEEE 802.11a has 160 short training symbol samples and 160 long training symbol samples;

the short training symbol is used for signal detection, AGC, diversity selection, timing synchronization and coarse frequency offset estimation, and the long training symbol is used for channel estimation and fine frequency offset estimation; and

short training sequences are configured of ten identical symbols from s_1 to s_{10} , in which each symbol has 16 real number parts and 16 imaginary number parts, and long training sequences are configured of two identical symbols of l_1 and l_2 , in which each symbol has 64 real number parts and 64 imaginary number parts.

【Claim 2】

A method of designing a symbol timing offset synchronizer which simplifies a direct form filter structure into an eight tap transposed direct form structure and converts eight filter coefficients into a canonic signed digit (CSD) form, the method comprising the steps of:

converting the direct form filter structure into the transposed direct form filter structure;

converting a filter coefficient of the transposed direct form filter structure into coefficients of the CSD form; and

re-designing the filter structure based on the CSD form coefficient, wherein

a packet constructed at a transmitting end of a WLAN (IEEE 802.11a) OFDM

wireless communication scheme includes a preamble, a header and a payload which is a data actually desired to transmit, and a structure of the preamble used in the IEEE 802.11a has 160 short training symbol samples and 160 long training symbol samples;

the short training symbol is used for signal detection, AGC, diversity selection, timing synchronization and coarse frequency offset estimation, and the long training symbol is used for channel estimation and fine frequency offset estimation; and

short training sequences are configured of ten identical symbols from s_1 to s_{10} , in which each symbol has 16 real number parts and 16 imaginary number parts, and long training sequences are configured of two identical symbols of l_1 and l_2 , in which each symbol has 64 real number parts and 64 imaginary number parts.