Method For Forming High-K Charge Storage Device

Abstract

Structures and methods of fabricating of a floating gate non-volatile memory device. In a first example embodiment, We form a bottom tunnel layer comprised of a lower oxide tunnel layer and a upper hafnium oxide tunnel layer; a charge storage layer comprised of a tantalum oxide and a top blocking layer preferably comprised of a lower hafnium oxide storage layer and an upper oxide storage layer. We form a gate electrode over the top blocking layer. We pattern the layers to form a gate structure and form source/drain regions to complete the memory device. In a second example embodiment, we form a floating gate non-volatile memory device comprised of: a bottom tunnel layer comprised essentially of silicon oxide; a charge storage layer comprised of a tantalum oxide; a top blocking layer comprised essentially of silicon oxide; and a gate electrode. The embodiments also comprise anneals and nitridation steps.

Figure 3