

A cross-sectional view of a substrate 2. A conductive layer 3 is formed on the top surface of the substrate 2. A dielectric layer 4 is formed on the top surface of the conductive layer 3. The dielectric layer 4 has a central portion 41 that is thicker than the side portions.

A cross-sectional view of a semiconductor device. A central channel region (2) is formed in a substrate. On both sides of the channel, there are gate structures. Each gate structure includes a gate dielectric layer (3) and a gate electrode (4). The gate electrodes (4) are positioned on the top and side surfaces of the gate dielectric layer (3). A central region (43) is indicated by a double-headed arrow, representing the channel length or a specific region within the channel.

FIG. 2B

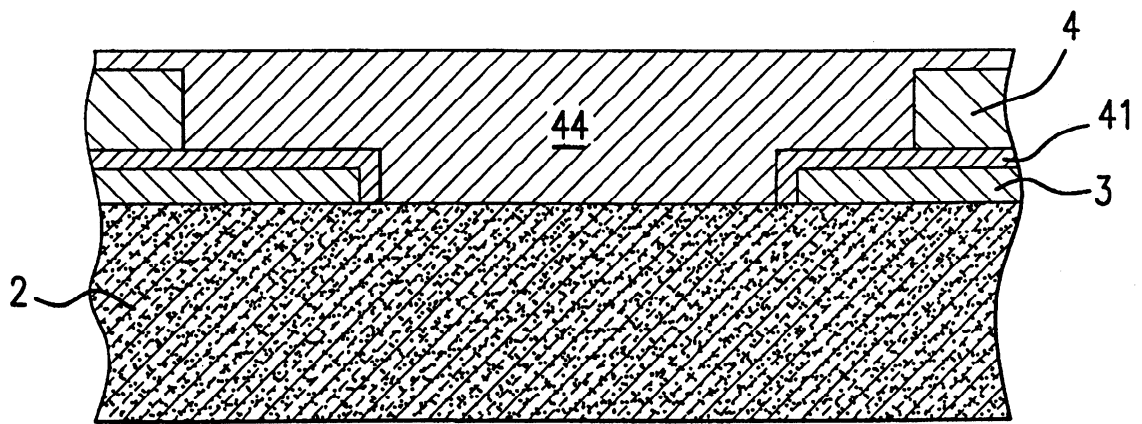


FIG.2C

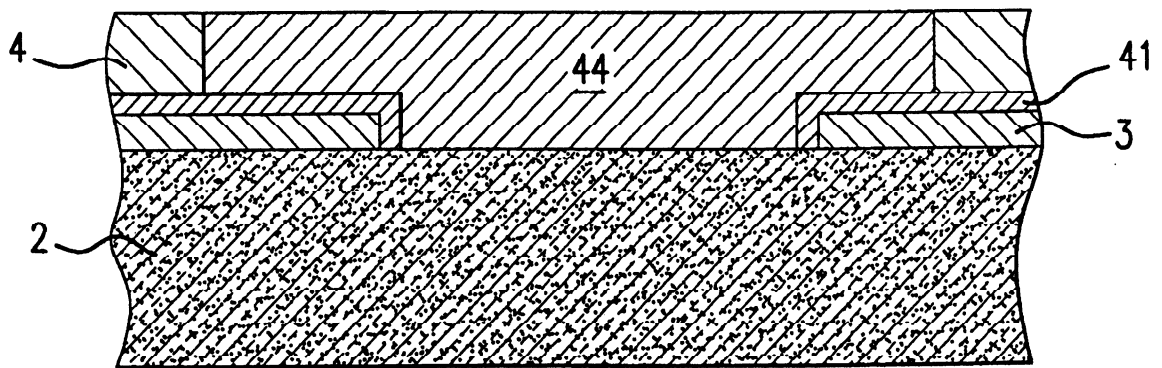


FIG.2D

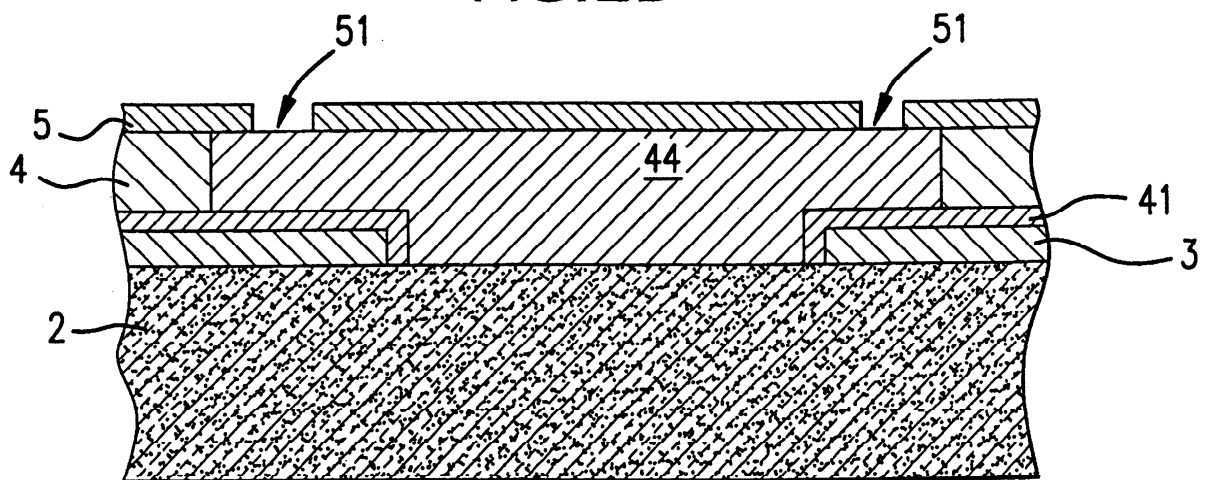


FIG.2E

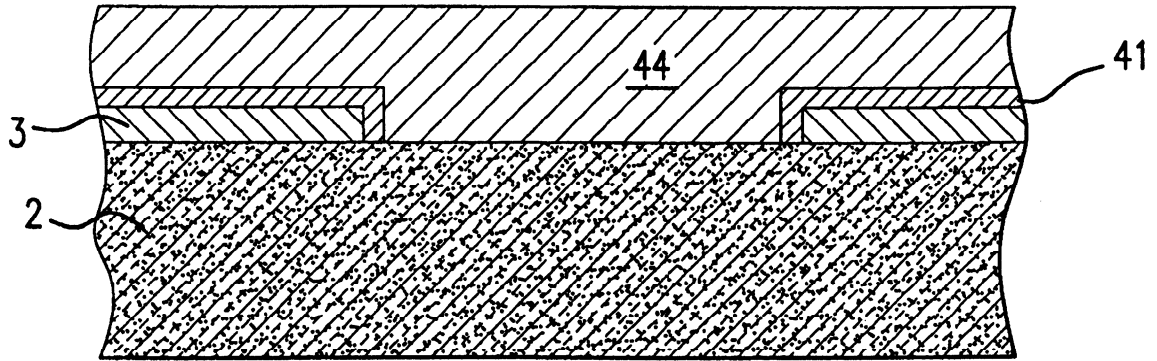


FIG.3A

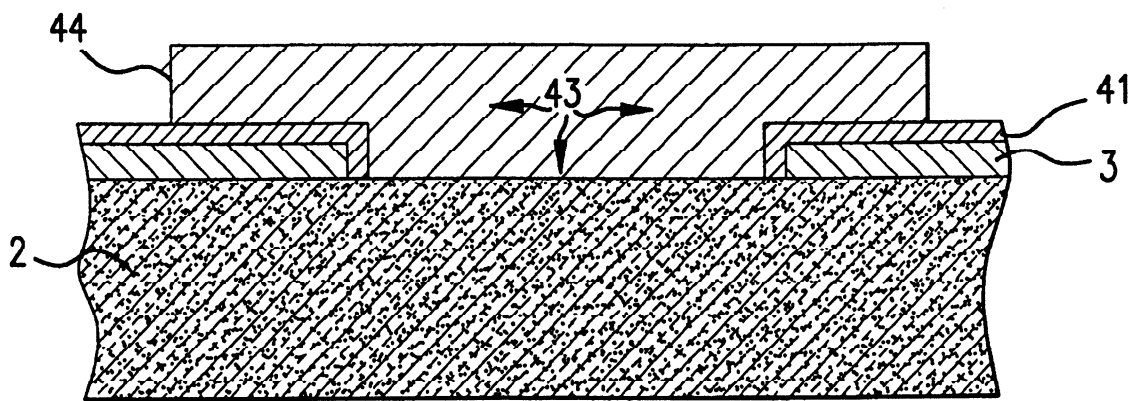


FIG.3B

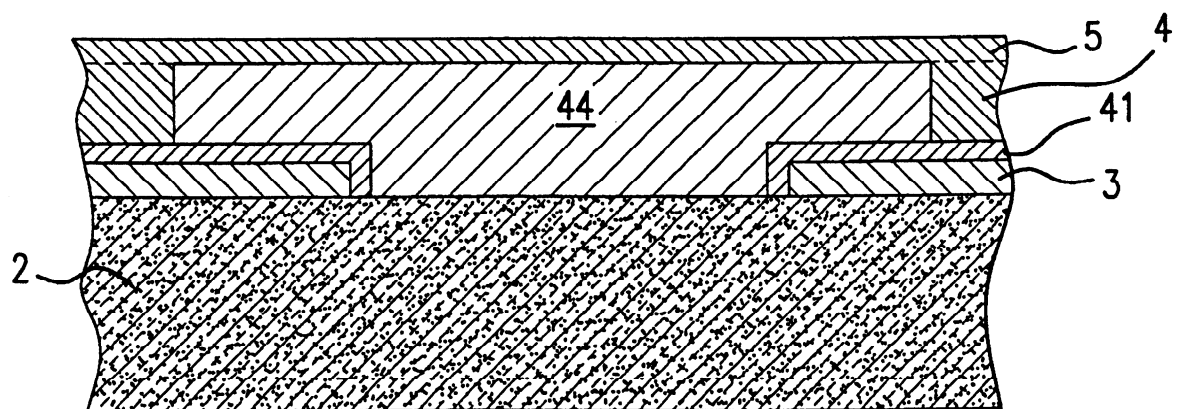


FIG.3C

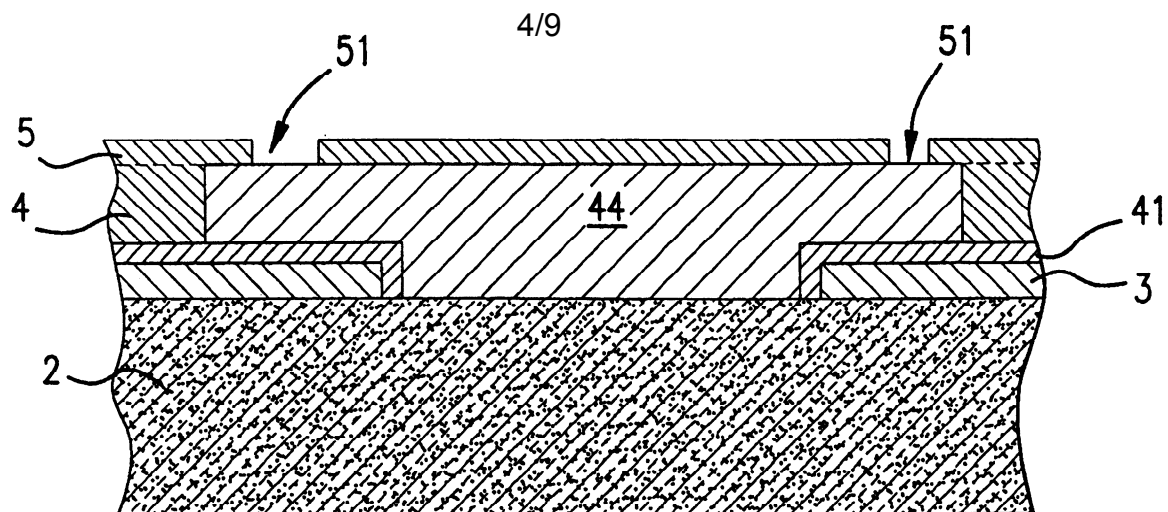


FIG. 3D

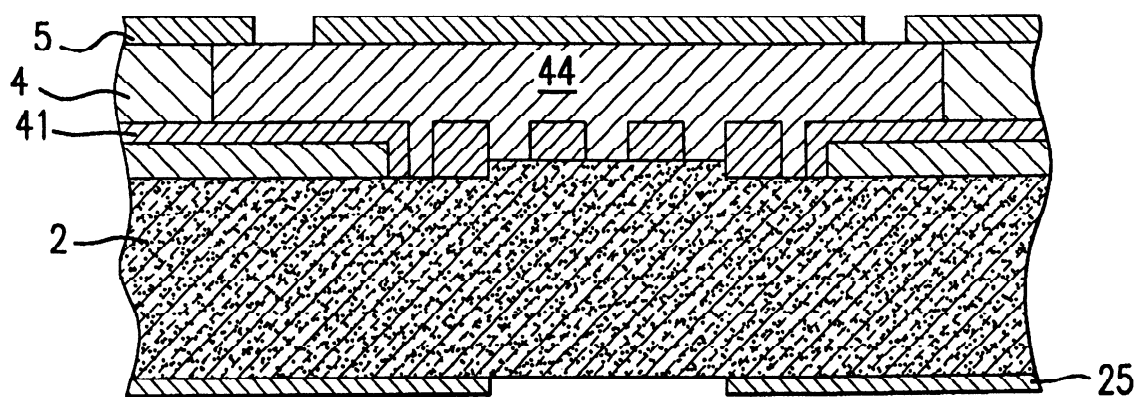


FIG. 4A

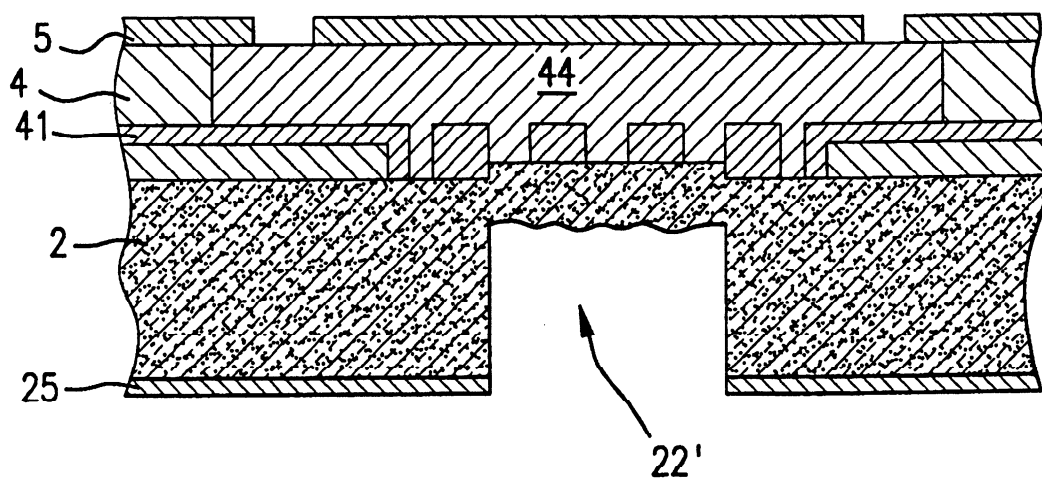


FIG. 4B

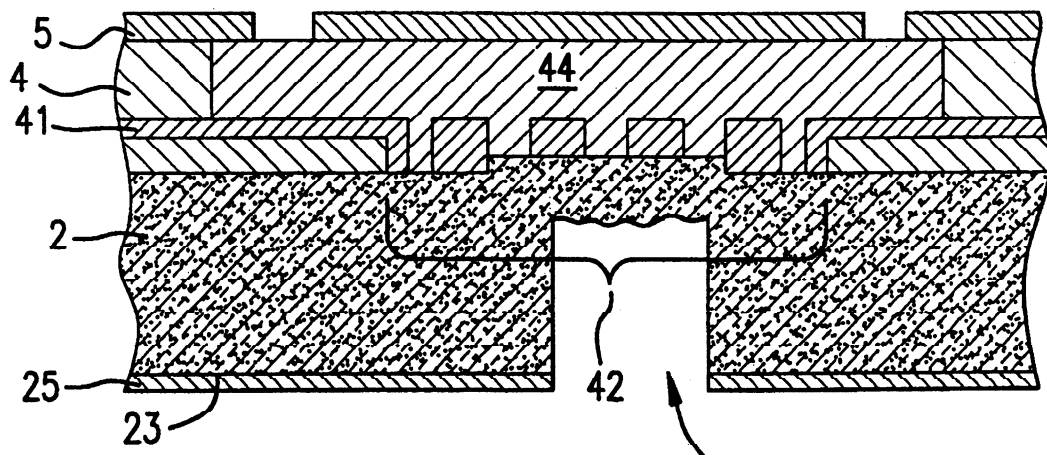


FIG. 4C

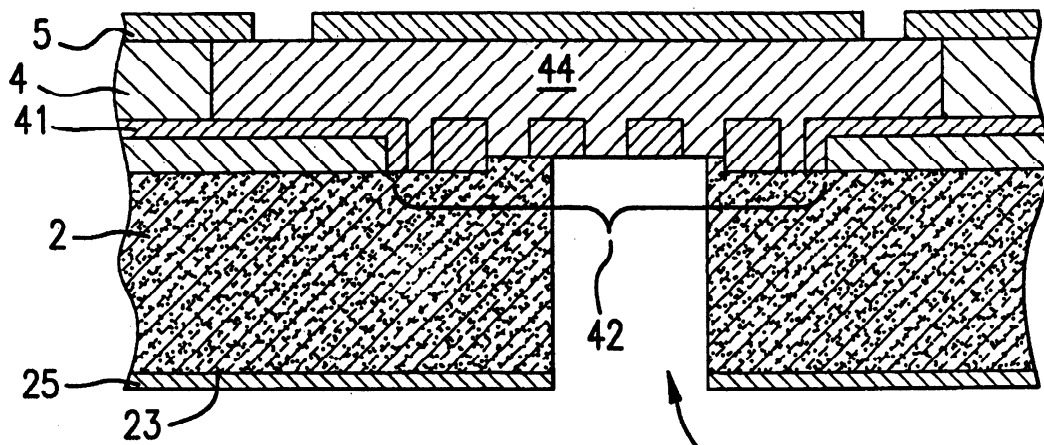


FIG. 4D

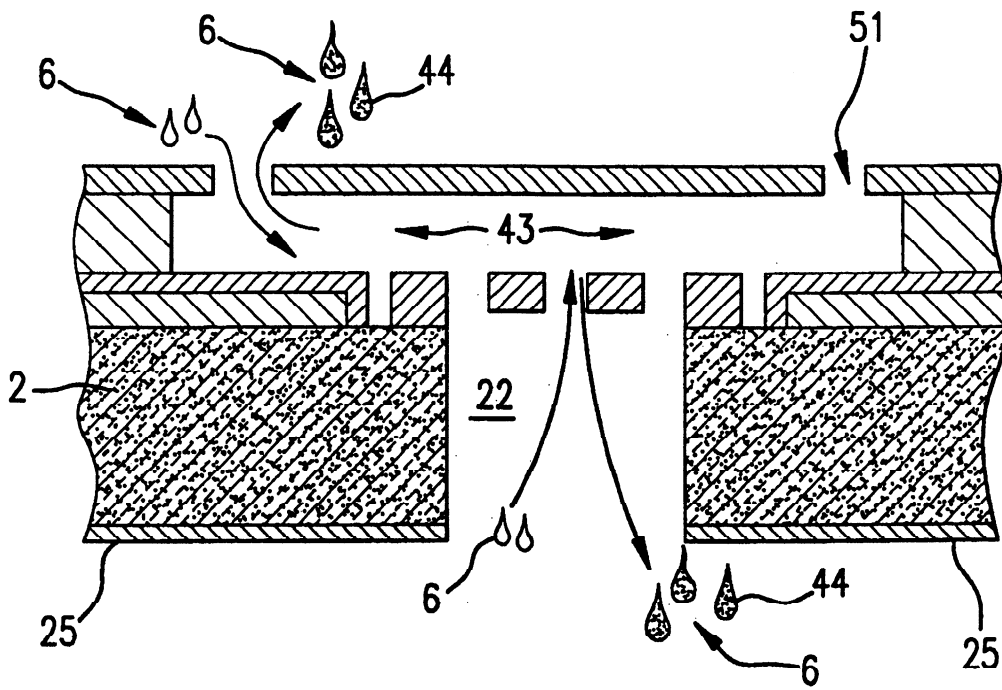


FIG. 5

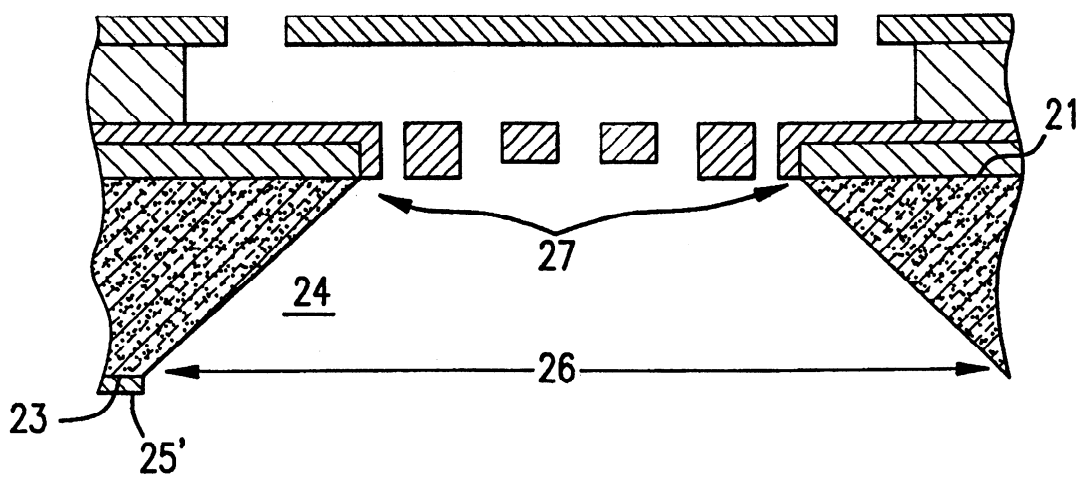


FIG. 6

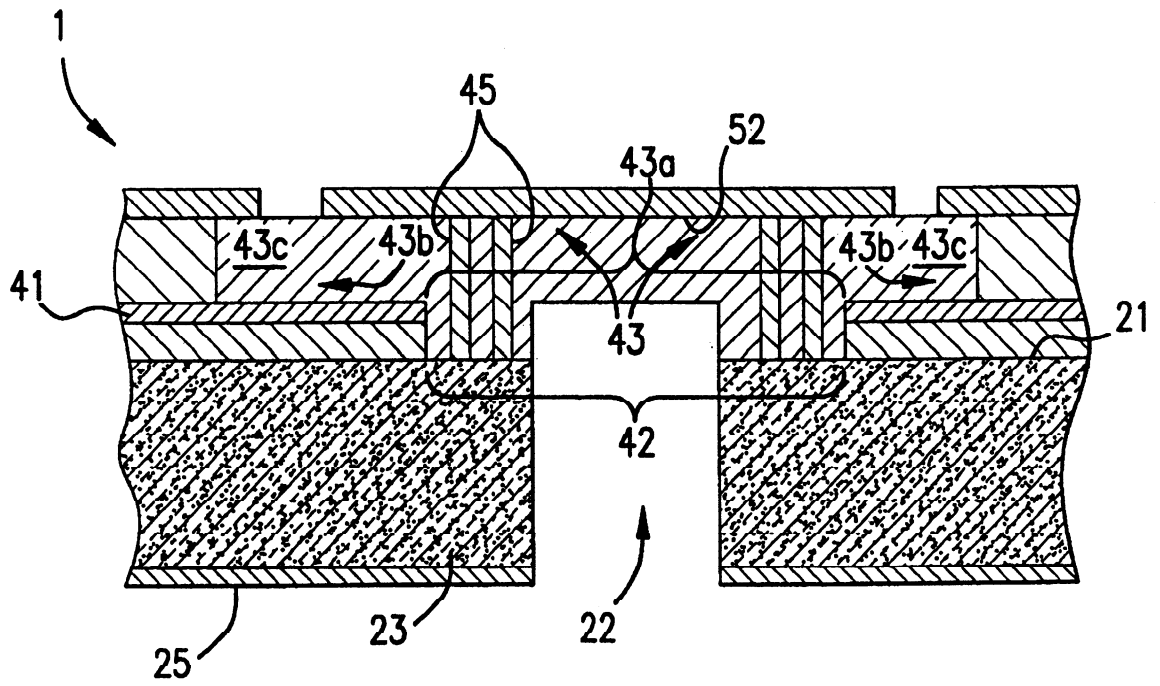


FIG. 7

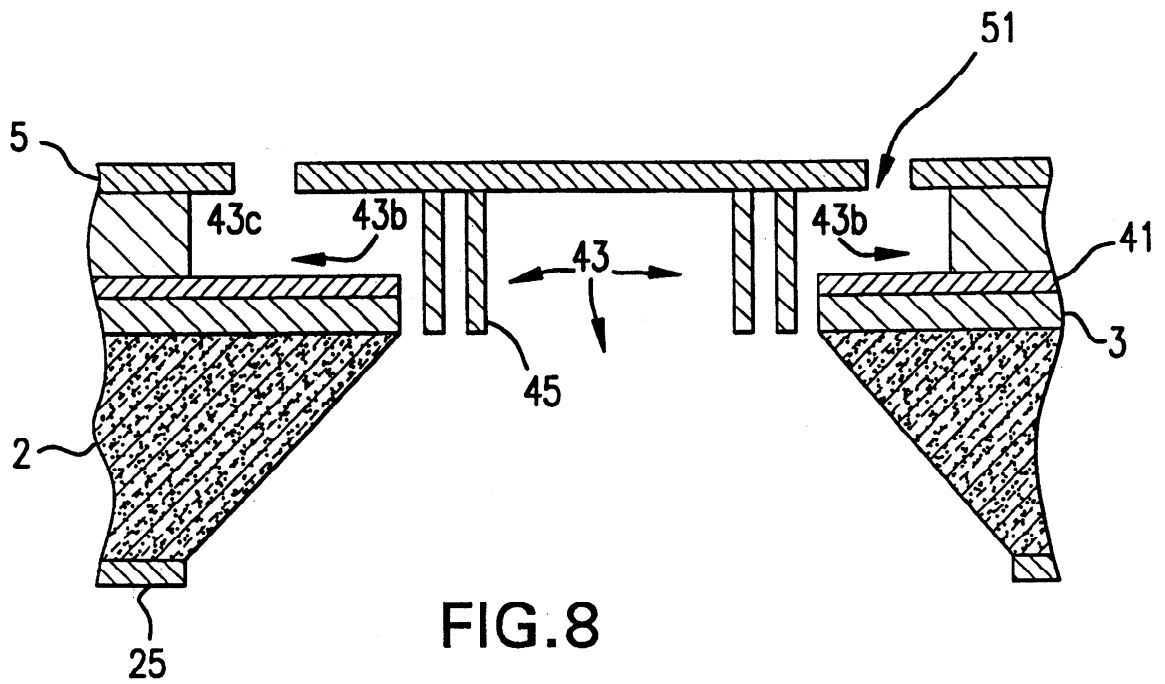


FIG. 8

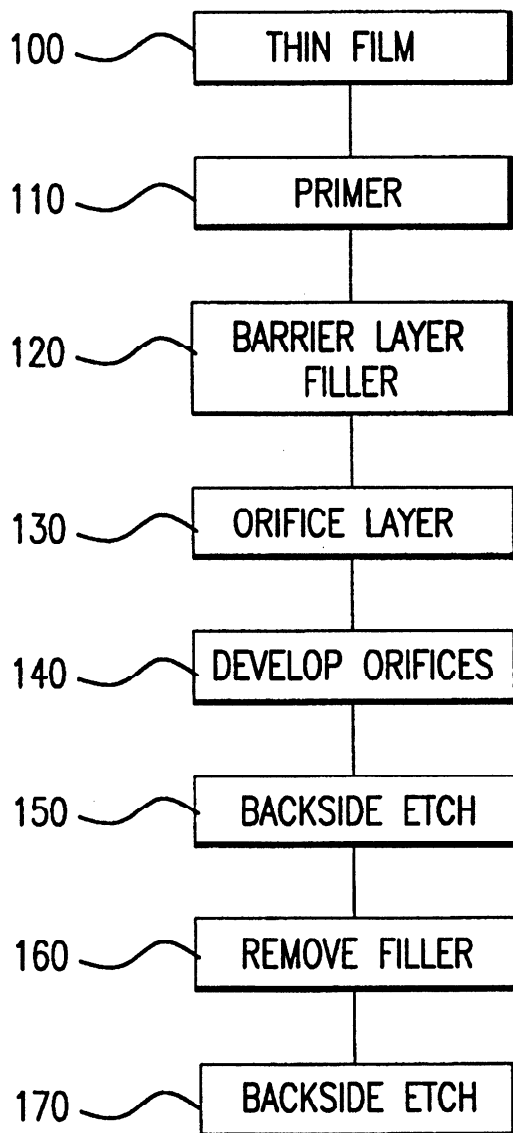


FIG.9

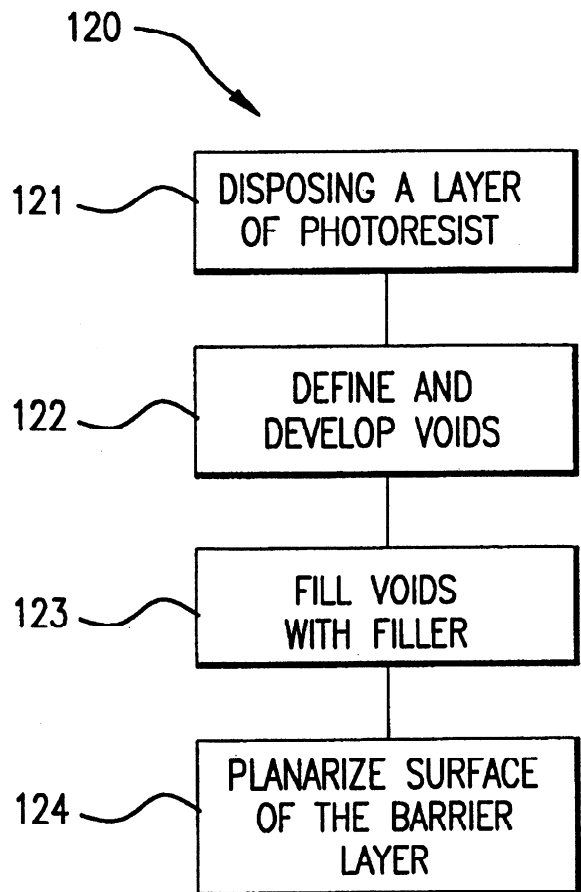


FIG.9A

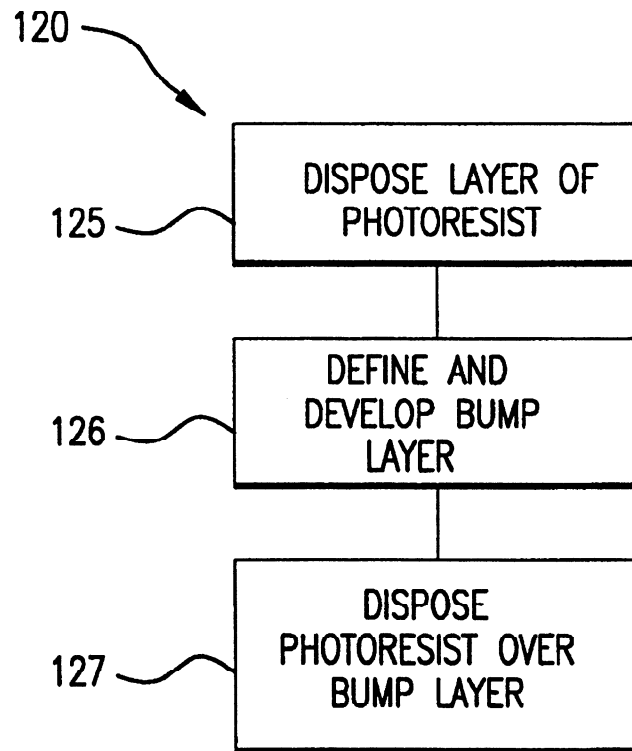


FIG.9B

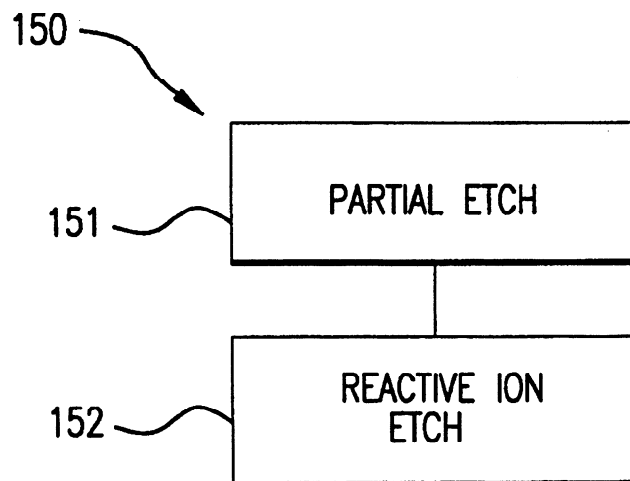


FIG.9C