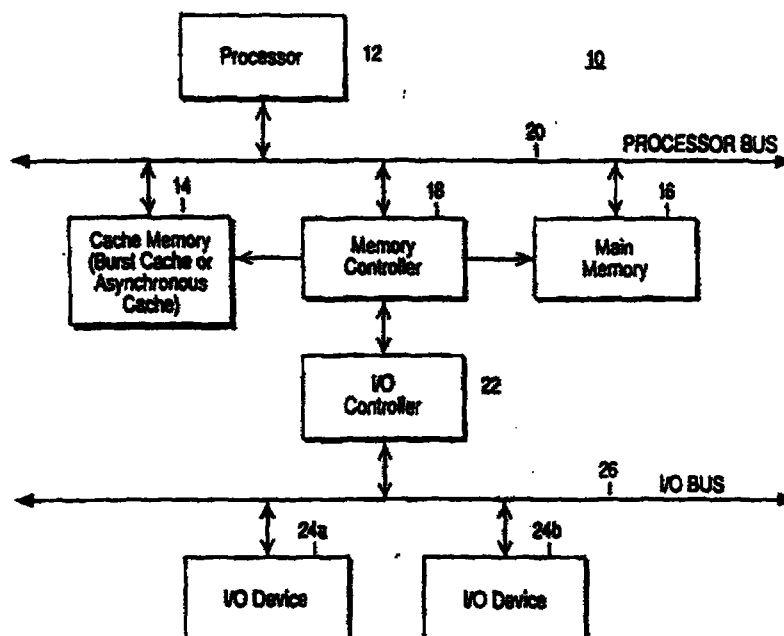




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(54) Title: A CACHE SRAM CONNECTOR ASSEMBLY



(57) Abstract

A cache SRAM connector assembly (26) comprising a connector (28), a number of latches (30A-30B) and a number of high performance switches (32A-32C), is provided to a computer system (10). The connector (28) removably connects either asynchronous or burst cache SRAM to a processor bus (20). The latches (30A-30B) store cache access addresses being driven on a number of address lines of the processor bus (20). The high performance switches (32A-32C) being coupled to both the latches (30A-30B) and the address lines of the processor bus (20) selectively provide the cache SRAM with latched access addresses as required by asynchronous cache SRAM or directly driven access addresses on the processor bus (20) as required by burst cache SRAM.