Phase shifter.

The present invention relates to a phase shifter arrangement having a first and a second input terminal intended for receiving two signals in phase opposition, and having a first and a second output terminal intended for supplying two signals which are shifted in phase relative to the input signals, the arrangement comprising a first series circuit of a resistor and a capacitor connected between the input terminals, in which first series circuit the resistor is connected to the first input terminal and the junction point between the resistor and the capacitor is connected to the first output terminal, and comprising a second series circuit of a resistor and a capacitor connected between the input terminals, in which second series circuit the resistor is connected to the second input terminal and the junction point between the resistor and the capacitor is connected to the second output terminal.

A circuit arrangement of this type is used in a variety of fields in electronics, including SSB radio transceivers, phase modulators having four or multiples of four states, scanning aerials.

A circuit arrangement of this type is known from the Patent US-3,544,886. This document explains that the input impedance of the stages following the phase shifter arrangement should be high and to this end the circuit arrangement in accordance with this document comprises an adapted amplifier which receives the output signal. Furthermore, the circuit arrangement described in said document does not comprise output terminals for transferring the input signals. These signals would nevertheless be available on the points referenced a and b in the Figures of said document, but this would pose the same problem as regards the input impedance of the following stages. Moreover, should the input impedance of the following stages influence each of the two "output signals" in a similar way it would influence the phase and the amplitude of the "input signals" in a different way.

The invention aims at providing a phase-shifter arrangement in which the impedance of the following stages do not affect the relative amplitudes and phases of all the signals appearing at the output, provided that these stages all have the same impedance.

To this end the circuit arrangement in accordance with the invention comprises a first parallel circuit constituted by a resistor and capacitor in parallel, which first parallel circuit is connected between the first input terminal and a third output terminal, and a second parallel circuit constituted by a resistor and capacitor in parallel, which second parallel circuit is connected between the second input terminal and a fourth output terminal.

Thus, the circuit arrangement has output terminals where the relative phases and amplitudes with respect to the outputs of the phase-shifted signals are not changed even if the impedances of the subsequent stages are low, because all phases as well as all amplitudes are then changed by an equal amount.

In order to achieve that the relative phase shifts at the four output terminals are 0°, 180°, φ, and $\varphi+180°$, which are frequently desired values, the four resistors of the arrangement are equal to one another and the four capacitors are equal to one another, at least in nominal value.

Suitably, each resistor is adjusted to compensate for the difference with respect to the nominal value of its associated capacitor, in order to obtain the required RC product.

If the frequency of the signals is variable either the four resistors or the four capacitors are adjustable together by means of a single control. In an advantageous simplified version either the two resistors or the two capacitors of the series circuits are adjustable together by means of a single control, and the elements of the parallel circuits are fixed.

The following description with reference to the annexed drawings, which show non-limitative examples, will clarify how the invention can be realised.

Figure 1 is a circuit diagram of the prior-art circuit arrangement;

Fig. 2 is a circuit diagram of the circuit arrangement in accordance with the invention.

In the specific case in which a phase shifter is used in an SSB receiver with image frequency rejection the shifter is used for generating a signal of the phase φ required for image frequency rejection.

For certain arrangements it is necessary to have four signals having the phases 0°, 90°, 180° and 240°.

The phase shifter shown in Figure 1 comprises a series circuit R_1, C_1 having a variable impedance (by variation of R_1 or C_1) whose ends receive the signals v, -v of opposite phase applied to the input terminals 1, 2. A second circuit R_2, C_2 inverted with respect to the first circuit enables the phase $\varphi + 180°$ to be obtained. Such an arrangement is frequently used for generating a signal of constant amplitude and of variable phase φ.

In the case of a single-sideband-modulation (SSB) receiver with image frequency rejection the amplitude equality of the 0° and 90° signals as well as the phase accuracy are important in order to achieve a high rejection. For example, in the case of a 0.5 dB amplitude difference the rejection is limited to 30 dB. Therefore, the invention is of particular interest for this field of use (SSB transceivers). Such a use requires four phases 0° and 180°, φ and $\varphi + 180°$. The difference signal 0/180° is used as a phase reference for the difference signal $\varphi/\varphi + 180°$. In this case all the signals should have equal amplitudes. Unfortunately, the following stages 5, 6, 7, 8, which take these signals from the terminals 3, 4, 10, 20 have non-zero input admittances Yin = Gin + $j\omega$Cin, which affect the relative amplitudes of the signals. Indeed, the signals on the outputs φ and $\varphi + 180°$ (terminals 3, 4) are related to the signal 0/180° (terminals 10, 20) having an amplitude v by the relation:

$$N_{\varphi} = \pm \frac{G - j\omega C}{(G + Gin) + j\omega(C + Cin)} v$$

Thus, the signal on the outputs φ and $\varphi + 180°$ is attenuated because the modulus of the transfer function is smaller than 1. In order to bring this attenuation back to a reasonable value ($\leq$ -1 dB) it is necessary that G $\geq$ - 10 Gin and C $\geq$ - 10 Cin, which requires the use of a stage having a very high impedance and/or an RC circuit having a low impedance. However, the impedance of the RC circuit should also be high in comparison with the output impedance of the stages 9, 11 which generate the reference

signals v, -v(0, 180°), if the amplitude of the signals should vary little with frequency and/or phase φ. This results in the following compromise:

$$Zout << R + \frac{1}{j\omega C} << Zin$$

where Zout is the output impedance of the stages 9, 11 and

Zin is the input impedance of the stages 5-8.

This compromise is highly restrictive and the phase shifter in accordance with the invention does not require a load stage with a high input impedance in order to ensure that the signals have equal amplitudes.

In the circuit arrangement shown in Fig. 2 a parallel RC circuit R_3, C_3 or R_4, C_4 is added to the preceding circuit, in series in each of the 0° and 180° paths, *i.e.* between the input terminals 1, 2, which are again connected to two series circuits R_1, C_1 and R_2, C_2, and the output terminals 10, 20.

The resistors and capacitors of these parallel circuits R_3C_3 and R_4C_4 have the same values as in the serial phase shift circuits R_1C_1 and R_2C_2. In relation to the differential input signal having an amplitude v the 0/180° output signal (terminals 10, 20) is given by:

$$V_{0°/180°} = \pm \frac{G + j\omega C}{(G + Gin) + j\omega(C + Cin)}$$

and the output signal $\varphi/\varphi+180\varphi$ (terminals 3, 4) is given by:

$$V_{\varphi/\varphi+180°} = \pm \frac{G - j\omega C}{(G + Gin) + j\omega(C + Cin)}$$

The amplitude at the four output terminals 3, 4, 10, 20 is the same regardless of the frequency, the phase shift introduced by the RC circuits, and the input impedance of the load stages 5-8.

This yields an almost perfect compensation for which the use of a high-impedance load stage is no longer indispensable. The load impedance merely has the effect of equally attenuating the four output signals of the system, provided of course that if the impedances are not high they are equal to one another, at least in nominal

value. The rejection ratio attainable in the SSB receiver depends on the permissible tolerances on all the components.

In the specific case that such a circuit arrangement is used for obtaining a fixed phase shift at a fixed frequency it is advantageous to realise in so-called hybrid circuit technology comprising integrated resistors and discrete capacitors on the same substrate. The value of each resistor can then be adjusted (for example, by means of a laser) depending upon the associated capacitor, thereby compensating for a possible error in the nominal value of the latter.

Conversely, when the frequency or rather the desired phase shift varies, it is necessary that either R or C can be varied. The preferred method is to vary either the four resistors or the four capacitors together by means of a single control, in order to ensure that all the RC products remain mutually equal.

In practice, an interesting compromise can be obtained by choosing for R_3, C_3, R_4, C_4 fixed values, substantially corresponding to the value necessary in the middle of the frequency range or the range of variation of φ, and by varying only R_1 and R_2, or C_1 and C_2, by means of a single control.

When used specifically in an SSB receiver for frequencies of the order of 1 to 5 GHz the stages 5 to 8, 9, 11 are realised by means of MESFET transistors on a gallium arsenide substrate. The resistors R1 to R4 are each constituted by a MESFET transistor used as a variable resistor. These transistors all have the same dimension and are together controlled by a variable common gate bias voltage in order to vary their dynamic resistance as desired. For the indicated frequencies the transistors may have, for example, a gate width of approximately 10 μm and the (integrated) capacitors have a value of 0.1 pF. In the output stages 5 and 6 the signal input is the gate of a MESFET transistor.

For use at a lower frequency it is also possible to employ variable capacitors, for example, realised by means of variable-capacitance diodes, all controlled by a single bias voltage, the resistors then being fixed resistors.

CLAIMS:

1. A phase shifter arrangement having a first and a second input terminal intended for receiving two signals in phase opposition, and having a first and a second output terminal intended for supplying two signals which are shifted in phase relative to the input signals, the arrangement comprising a first series circuit of a resistor and a capacitor connected between the input terminals, in which first series circuit the resistor is connected to the first input terminal and the junction point between the resistor and the capacitor is connected to the first output terminal, and comprising a second series circuit of a resistor and a capacitor connected between the input terminals, in which second series circuit the resistor is connected to the second input terminal and the junction point between the resistor and the capacitor is connected to the second output terminal, characterised in that it comprises a first parallel circuit constituted by a resistor and capacitor in parallel, which first parallel circuit is connected between the first input terminal and a third output terminal, and a second parallel circuit constituted by a resistor and capacitor in parallel, which second parallel circuit is connected between the second input terminal and a fourth output terminal.

2. An arrangement as claimed in Claim 1, characterised in that the four resistors are equal to one another and the four capacitors are equal to one another, at least in nominal value.

3. An arrangement as claimed in Claim 2, characterised in that each resistor is adjusted to compensate for the difference with respect to the nominal value of its associated capacitor, in order to obtain the required RC product.

4. An arrangement as claimed in Claim 1 or 2, used in the case that the frequency of the signals is variable, characterised in that either the four resistors or the four capacitors are adjustable together by means of a single control.

5. An arrangement as claimed in Claim 1 or 2, used in the case that the frequency of the signals is variable, characterised in that either the two resistors or the

two capacitors of the series circuits are adjustable together by means of a single control, and the elements of the parallel circuits are fixed.