WHAT IS CLAIMED IS:

1. A semiconductor package, comprising:

a first semiconductor chip on a wiring substrate, the first semiconductor chip electrically connected to the wiring substrate;

an intermediate layer on the first semiconductor chip, the intermediate layer covering an entire surface of the first semiconductor chip;

a second semiconductor chip on the intermediate layer, the second semiconductor chip electrically connected to the wiring substrate;

a mold layer on the wiring substrate, the mold layer covering the first semiconductor chip and the second semiconductor chip, the mold layer including one or more inner surfaces at least partially defining a mold via hole that exposes a portion of a surface of the intermediate layer;

an electromagnetic shielding layer on the one or more inner surfaces of the mold layer, the electromagnetic shielding layer further on one or more outer surfaces of the mold layer; and

a thermal discharge layer on the electromagnetic shielding layer in the mold via hole, such that the thermal discharge layer fills the mold via hole.

2. The semiconductor package of claim 1, wherein

the first semiconductor chip includes a heat source,

the mold via hole and the thermal discharge layer correspond to the heat source, such that the semiconductor package is configured to discharge heat generated in the heat source to an outside of the semiconductor package via at least the mold via hole and the thermal discharge layer.

3. The semiconductor package of claim 1 or claim 2, wherein

the first semiconductor chip includes a logic chip, and

the second semiconductor chip includes a memory chip.

4. The semiconductor package of any one of claims 1 to 3, wherein

the first semiconductor chip is electrically connected to the wiring substrate via a connection bump, and

the second semiconductor chip is electrically connected to the wiring substrate via a bonding wire.

5. The semiconductor package of any one of claims 1 to 4, wherein the second semiconductor chip includes a multilayer chip that includes a plurality of sub-chips, the plurality of sub-chips sequentially stacked on the intermediate layer.

6. The semiconductor package of any one of claims 1 to 5, wherein the intermediate layer is a heat spreader or an interposer chip.

7. The semiconductor package of any one of claims 1 to 6, wherein the mold via hole is at least partially defined by a recess portion recessed from the surface of the intermediate layer into an interior of the intermediate layer.

8. The semiconductor package of any one of claims 1 to 7, wherein the mold via hole includes a mold via pattern having a planar constant area on the intermediate layer.

9. The semiconductor package of any one of claims 1 to 8, wherein the mold via hole includes a plurality of mold via patterns extending in one direction on the intermediate layer and isolated from direct contact with each other.

10. The semiconductor package of any one of claims 1 to 9, wherein the electromagnetic shielding layer extends conformally on a surface defining a bottom of the mold via hole and the one or more inner surfaces defining an inner wall of the mold via hole and on the one or more outer surfaces and opposing side walls of the mold layer.

11. The semiconductor package of any one of claims 1 to 10, wherein

an area of the semiconductor package includes a chip area in which the first semiconductor chip and the second semiconductor chip overlap each other in a vertical direction that extends perpendicular to an upper surface of the wiring substrate and a heat discharge area in which the first semiconductor chip and the second semiconductor chip do not overlap each other in the vertical direction, and

the heat discharge area includes the mold via hole and the thermal discharge layer.

12. A semiconductor package, comprising:

a first semiconductor chip on a wiring substrate, the first semiconductor chip electrically connected to the wiring substrate, the first semiconductor chip including a logic chip;

an intermediate layer on the first semiconductor chip, the intermediate layer covering an entire surface of the first semiconductor chip;

a second semiconductor chip on the intermediate layer, the second semiconductor chip electrically connected to the wiring substrate, the second semiconductor chip including a memory chip;

a third semiconductor chip on the intermediate layer, the third semiconductor chip isolated from direct contact with the second semiconductor chip, the third semiconductor chip electrically connected to the wiring substrate, the third semiconductor chip including a separate memory chip;

a mold layer on the wiring substrate, the mold layer covering the first semiconductor chip, the second semiconductor chip, and the third semiconductor chip, the mold layer including one or more inner surfaces at least partially defining a mold via hole that exposes a portion of a surface of the intermediate layer;

an electromagnetic shielding layer on the one or more inner surfaces of the mold layer, the electromagnetic shielding layer further on one or more outer surfaces of the mold layer; and

a thermal discharge layer on the electromagnetic shielding layer in the mold via hole such that the thermal discharge layer fills the mold via hole.

13. The semiconductor package of claim 12, wherein the mold via hole is on the intermediate layer and is between the second semiconductor chip and the third semiconductor chip.

14. The semiconductor package of claim 12, wherein the mold via hole is on an edge portion of the intermediate layer and is

proximate to the second semiconductor chip in relation to the third semiconductor chip and is isolated from direct contact with the second semiconductor chip, or

proximate to the third semiconductor chip in relation to the second semiconductor chip and is isolated from direct contact with the third semiconductor chip.

15. The semiconductor package of any one of claims 12 to 14, wherein each semiconductor chip of the second semiconductor chip and the third semiconductor chip includes a separate multilayer chip, each separate multilayer chip including a separate plurality of sub-chips that are sequentially stacked on the intermediate layer.

16. The semiconductor package of any one of claims 12 to 15, wherein

the intermediate layer includes a heat spreader,

the first semiconductor chip is electrically connected to the wiring substrate via a connection bump, and

the second semiconductor chip and the third semiconductor chip are each electrically connected to the wiring substrate via a separate bonding wire.

17. The semiconductor package of any one of claims 12 to 14, wherein

the intermediate layer includes an interposer chip,

each semiconductor chip of the second semiconductor chip and the third semiconductor chip includes a separate multilayer chip, each separate multilayer chip including a plurality of sub-chips that are sequentially stacked, and

each semiconductor chip of the second semiconductor chip and the third semiconductor chip is electrically connected to the wiring substrate via the interposer chip.

18. A semiconductor package, comprising:

a first semiconductor chip on a wiring substrate, the first semiconductor chip electrically connected to the wiring substrate, the first semiconductor chip including a logic chip, the logic chip including a heat source;

an intermediate layer on the first semiconductor chip, the intermediate layer covering an entire surface of the first semiconductor chip;

a second semiconductor chip on the intermediate layer, the second semiconductor chip electrically connected to the wiring substrate, the second semiconductor chip including a memory chip;

a third semiconductor chip on the intermediate layer, the third semiconductor chip isolated from direct contact with the second semiconductor chip, the third semiconductor chip electrically connected to the wiring substrate, the third semiconductor chip including a separate memory chip;

a mold layer on the wiring substrate, the mold layer covering the first semiconductor chip, the second semiconductor chip, and the third semiconductor chip, the mold layer including a plurality of inner surfaces at least partially defining a plurality of mold via holes that expose a portion of a surface of the intermediate layer in both a center region between the second semiconductor chip and the third semiconductor chip and in an edge portion of the intermediate layer;

an electromagnetic shielding layer on the plurality of inner surfaces of the mold layer, the electromagnetic shielding layer further on one or more outer surfaces of the mold layer; and

a thermal discharge layer on the electromagnetic shielding layer in each mold via hole of the plurality of mold via holes such that the thermal discharge layer fills the plurality of mold via holes.

19. The semiconductor package of claim 18, wherein

the intermediate layer includes a heat spreader,

the first semiconductor chip is electrically connected to the wiring substrate via a connection bump, and

the second semiconductor chip and the third semiconductor chip are each electrically connected to the wiring substrate via a separate bonding wire.

20. The semiconductor package of claim 18, wherein

the intermediate layer includes an interposer chip,

the first semiconductor chip is electrically connected to the wiring substrate via a connection bump,

each semiconductor chip of the second semiconductor chip and the third semiconductor chip includes a separate multilayer chip, each separate multilayer chip including a separate plurality of sub-chips that are sequentially stacked, and the separate plurality of sub-chips are electrically connected to each other via one or more through vias, and

the second semiconductor chip and the third semiconductor chip are each electrically connected to the wiring substrate, via a separate bonding wire, via the interposer chip.