

WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:
a first interconnection line and a second interconnection line on a substrate; and
a first stack and a second stack between the substrate and the first and second interconnection lines,
wherein each of the first and second stacks comprises:
a plurality of semiconductor patterns vertically stacked on the substrate;
a plurality of conductive lines connected to the plurality of semiconductor patterns, respectively, each of the plurality of conductive lines extending in a first horizontal direction; and
a gate electrode that is adjacent to the plurality of semiconductor patterns and extends in a vertical direction,
wherein the plurality of conductive lines of the first stack comprise a first conductive line, and the plurality of conductive lines of the second stack comprise a second conductive line, and a lower surface of the first conductive line is at a level equal to a level of a lower surface of the second conductive line,
wherein the first interconnection line is electrically connected to at least one of the first and second conductive lines, and
wherein the gate electrode of the first stack comprises a first gate electrode, the gate electrode of the second stack comprises a second gate electrode, and the second interconnection line is electrically connected to at least one of the first and second gate electrodes,
wherein each of the plurality of semiconductor patterns comprises a first impurity region, a second impurity region, and a channel region between the first and second impurity regions,
wherein each of the plurality of semiconductor patterns further comprises an end layer between the first impurity region and a respective one of the plurality of conductive lines, and
wherein the end layer comprises a first semiconductor material whose band gap is smaller than a band gap of a second semiconductor material of the channel region.
2. The device of claim 1, further comprising a third interconnection line on the first and second stacks,
wherein the first interconnection line is electrically connected to the first conductive

line,

wherein the third interconnection line is electrically connected to the second conductive line, and

wherein the second interconnection line is electrically connected to both the first gate electrode and the second gate electrode.

3. The device of claim 2, wherein the second interconnection line extends in a second horizontal direction, and

wherein the first and second gate electrodes are spaced apart from each other in the second horizontal direction and are aligned in the second horizontal direction.

4. The device of claim 1, further comprising a third interconnection line on the first and second stacks,

wherein the first interconnection line is electrically connected to both the first conductive line and second conductive line,

wherein the second interconnection line is electrically connected to the first gate electrode, and

wherein the third interconnection line is electrically connected to the second gate electrode.

5. The device of claim 4, further comprising a common contact contacting both the first conductive line and second conductive line,

wherein the first interconnection line is electrically connected to both the first conductive line and second conductive line through the common contact.

6. The device of any one of claims 1 to 5, wherein each of the plurality of conductive lines is electrically connected to the first impurity region of each of the plurality of semiconductor patterns, and

wherein each of the first and second gate electrodes is adjacent to the channel region of the plurality of semiconductor patterns.

7. The device of any one of claims 1, 2, 4 and 5, wherein the first and second stacks extend parallel to each other in the first horizontal direction, and

wherein each of the plurality of semiconductor patterns of the first and second stacks extends in a second horizontal direction crossing the first horizontal direction.

8. The device of any one of claims 1, 2, 4 and 5, wherein the substrate comprises a first peripheral circuit region and a second peripheral circuit region,

wherein the first interconnection line extends toward the first peripheral circuit region or extends in the first horizontal direction, and the first interconnection line is electrically connected to a first peripheral transistor on the first peripheral circuit region, and

wherein the second interconnection line extends toward the second peripheral circuit region or extends in a second horizontal direction crossing the first horizontal direction, and the second interconnection line is electrically connected to a second peripheral transistor on the second peripheral circuit region.

9. The device of any one of claims 1 to 8, further comprising a contact contacting the at least one of the first and second conductive lines,

wherein the substrate comprises a cell region and a contact region,

wherein each the plurality of conductive lines extends from the cell region to the contact region,

wherein the contact is on the contact region, and

wherein the first interconnection line is electrically connected to the contact.

10. The device of any one of claims 1 to 8, wherein the substrate comprises a cell region and a contact region,

wherein each of the plurality of conductive lines of the first and second stacks comprises:

an interconnection portion horizontally extending from the cell region to the contact region; and

a contact portion that is on the contact region and vertically extends from the interconnection portion, and

wherein the first interconnection line is electrically connected to at least one of the contact portion of the first conductive line and the contact portion of the second conductive line.

11. A semiconductor memory device comprising:
a substrate including a cell region and a contact region;
a plurality of semiconductor patterns vertically stacked on the cell region, wherein each of the plurality of semiconductor patterns comprises a first impurity region, a second impurity region, and a channel region between the first and second impurity regions such that the plurality of semiconductor patterns comprise a plurality of first impurity regions, a plurality of second impurity regions, and a plurality of channel regions;
a plurality of first conductive lines horizontally extending from the cell region onto the contact region, wherein each of the plurality of first conductive lines is connected to a respective one of the plurality of first impurity regions of the plurality of semiconductor patterns;
a plurality of capacitors, wherein each of the plurality of capacitors is connected to a respective one of the plurality of second impurity regions of the plurality of semiconductor patterns; and
a plurality of contacts contacting the plurality of first conductive lines, respectively, on the contact region,
wherein the plurality of contacts comprise a first contact and a second contact that is closer to the cell region than the first contact,
wherein a level of a bottom surface of the second contact is higher than a level of a bottom surface of the first contact,
wherein each of the plurality of semiconductor patterns further comprises an end layer between the first impurity region and a respective one of the plurality of first conductive lines, and
wherein the end layer comprises a first semiconductor material whose band gap is smaller than a band gap of a second semiconductor material of the channel region.

12. The device of claim 11, wherein a first one of the plurality of first conductive lines is in contact with the first contact and has a first length on the contact region,
wherein a second one of the plurality of first conductive lines is in contact with the second contact and has a second length on the contact region, and
wherein the first length is longer than the second length.

13. The device of claim 11 or claim 12, further comprising:

a first interconnection line and a second interconnection line electrically connected to the first and second contacts, respectively; and

a first lower interconnection line and a second lower interconnection line on a peripheral circuit region of the substrate,

wherein the first and second lower interconnection lines are electrically connected to the first and second interconnection lines, respectively,

wherein the first and second lower interconnection lines include a first end and a second end, respectively, and

wherein the second end is closer to the contact region than the first end.

14. The device of claim 11 or claim 12, further comprising:

a second conductive line that is adjacent to the plurality of channel regions of the plurality of semiconductor patterns and extends in a vertical direction;

a first interconnection line electrically connected to the first contact; and

a second interconnection line electrically connected to the second conductive line,

wherein the substrate further comprises first and second peripheral circuit regions, and

wherein the first and second interconnection lines extend onto the first and second peripheral circuit regions, respectively.

15. The device of any one of claims 11 to 14, wherein each of the plurality of semiconductor patterns extends in a first direction, and

wherein the plurality of first conductive lines extend in a second direction crossing the first direction.

16. A semiconductor memory device comprising:

a substrate including a cell region and a contact region;

a first stack and a second stack on the substrate; and

a first interconnection line and a second interconnection line on the first and second stacks,

wherein the first interconnection line extends in a first horizontal direction that is parallel to a top surface of the substrate,

wherein the second interconnection line extends in a second horizontal direction that crosses the first horizontal direction and is parallel to the top surface of the substrate,

wherein each of the first and second stacks comprises:

a plurality of memory cell transistors three-dimensionally arranged on the substrate, the plurality of memory cell transistors comprising a plurality of semiconductor patterns;

a bit line connected to first ones of the plurality of memory cell transistors, the first ones of the plurality of memory cell transistors being spaced apart from each other in the first horizontal direction; and

a word line connected to second ones of the plurality of memory cell transistors, the second ones of the plurality of memory cell transistors being spaced apart from each other in a vertical direction that is perpendicular to the top surface of the substrate, and

wherein the bit line of the first stack comprises a first bit line, the bit line of the second stack comprises a second bit line, and wherein, on the contact region, the first interconnection line is electrically connected to at least one of the first and second bit lines, and

wherein the word line of the first stack comprises a first word line, the word line of the second stack comprises a second word line, and wherein, on the cell region, the second interconnection line is electrically connected to at least one of the first and second word lines,

wherein each of the plurality of semiconductor patterns comprises a first impurity region, a second impurity region, and a channel region between the first and second impurity regions,

wherein each of the plurality of semiconductor patterns further comprises an end layer between the first impurity region and the bit line, and

wherein the end layer comprises a first semiconductor material whose band gap is smaller than a band gap of a second semiconductor material of the channel region.

17. The device of claim 16, wherein the first and second bit lines extend in the first horizontal direction, and

wherein the first and second word lines extend in the vertical direction.

18. The device of claim 16 or claim 17, wherein the first bit line and the second bit line are at the same level.

19. The device of any one of claims 16 to 18, wherein the substrate further includes

a first peripheral circuit region and a second peripheral circuit region,

wherein the first interconnection line extends from the contact region onto the first peripheral circuit region, and

wherein the second interconnection line extends from the cell region onto the second peripheral circuit region.