

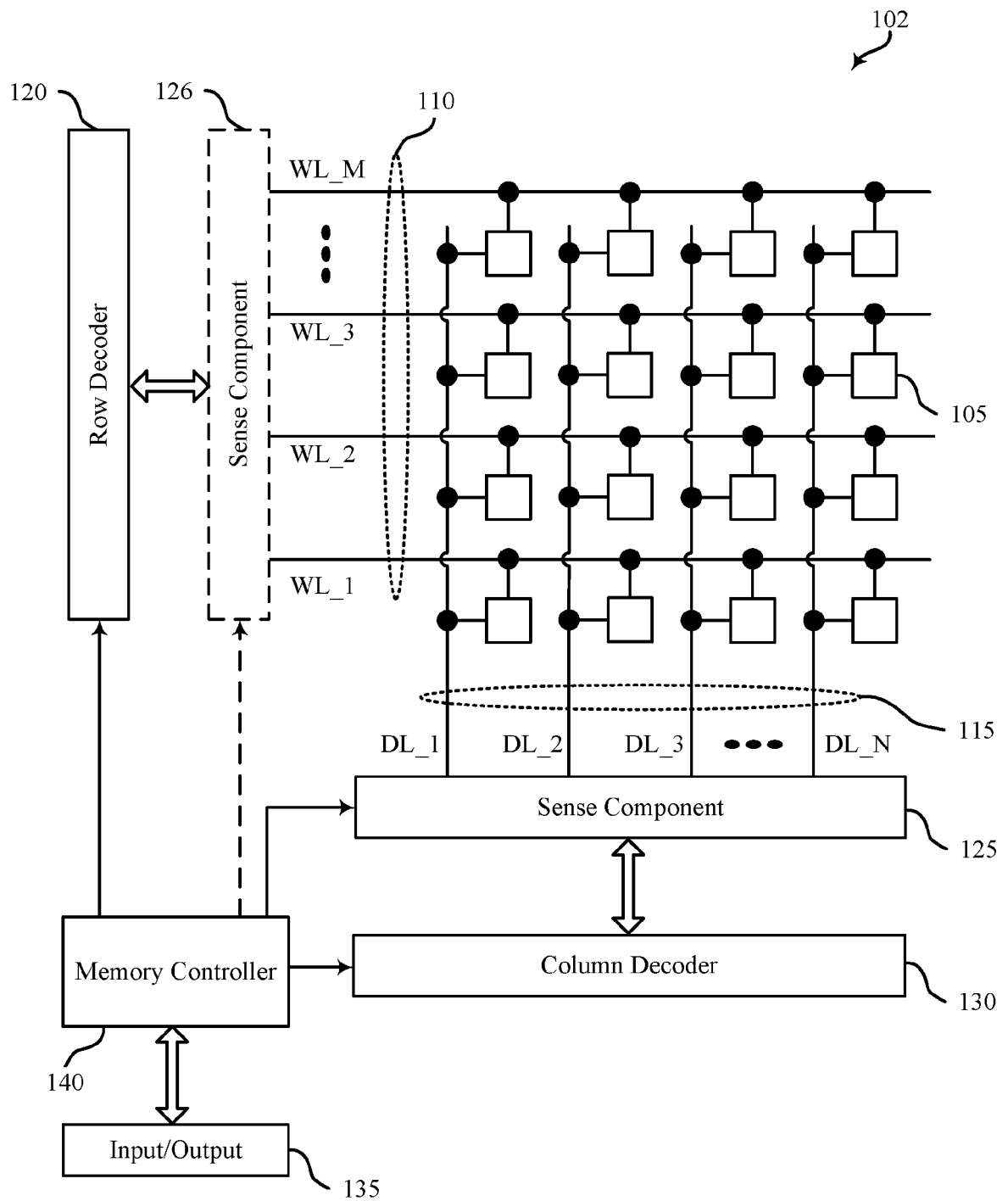


FIG. 1

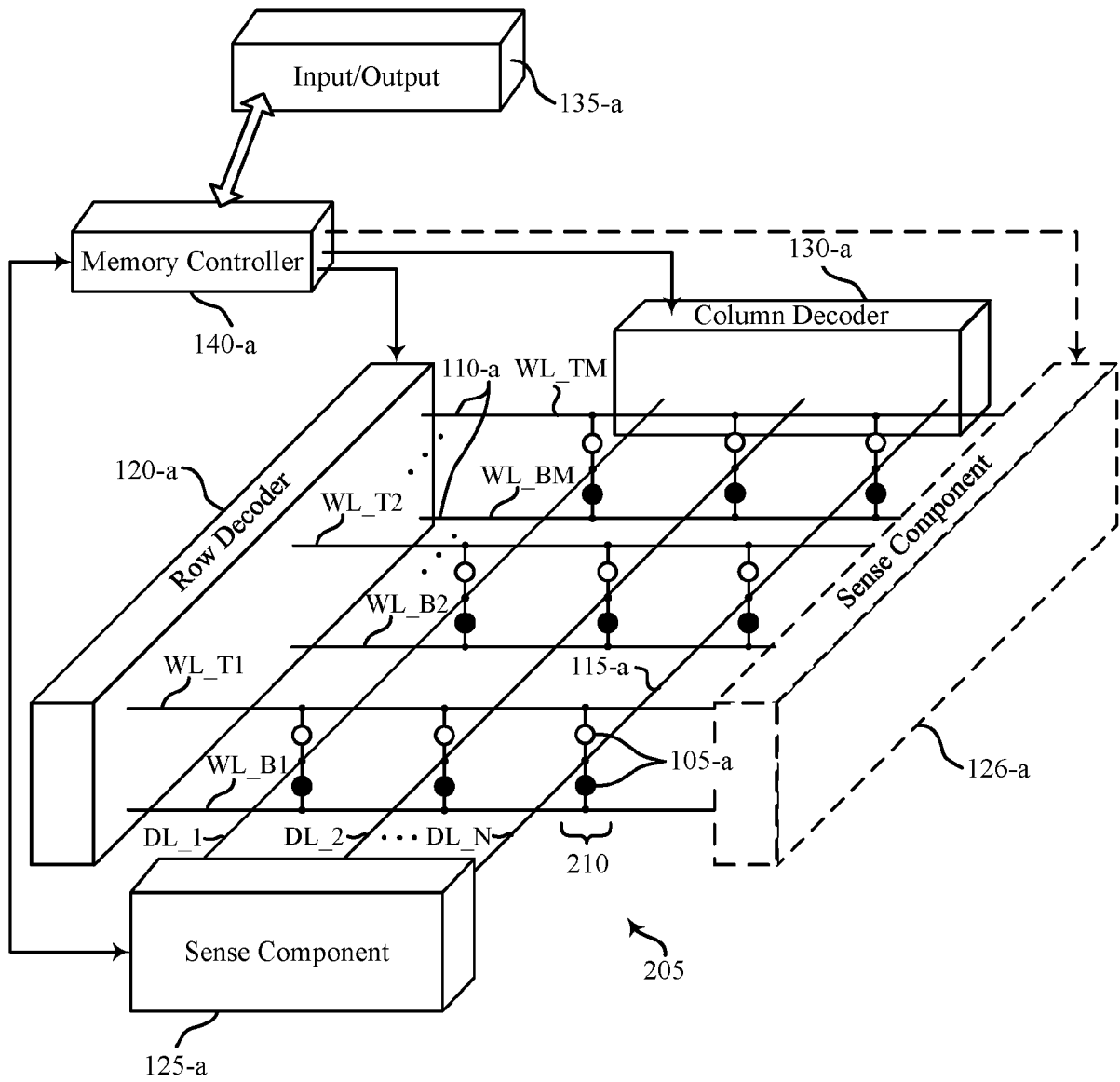


FIG. 2

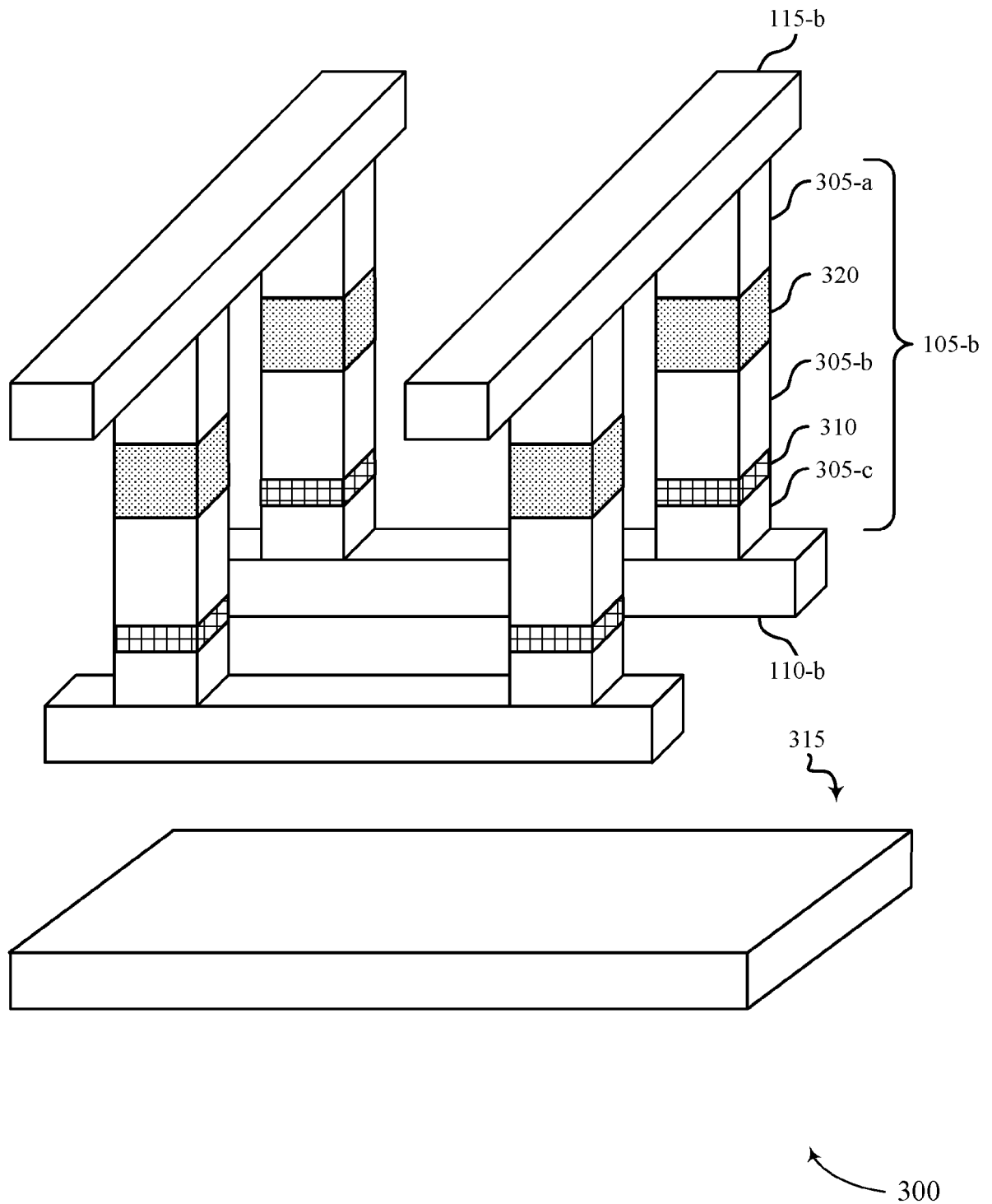
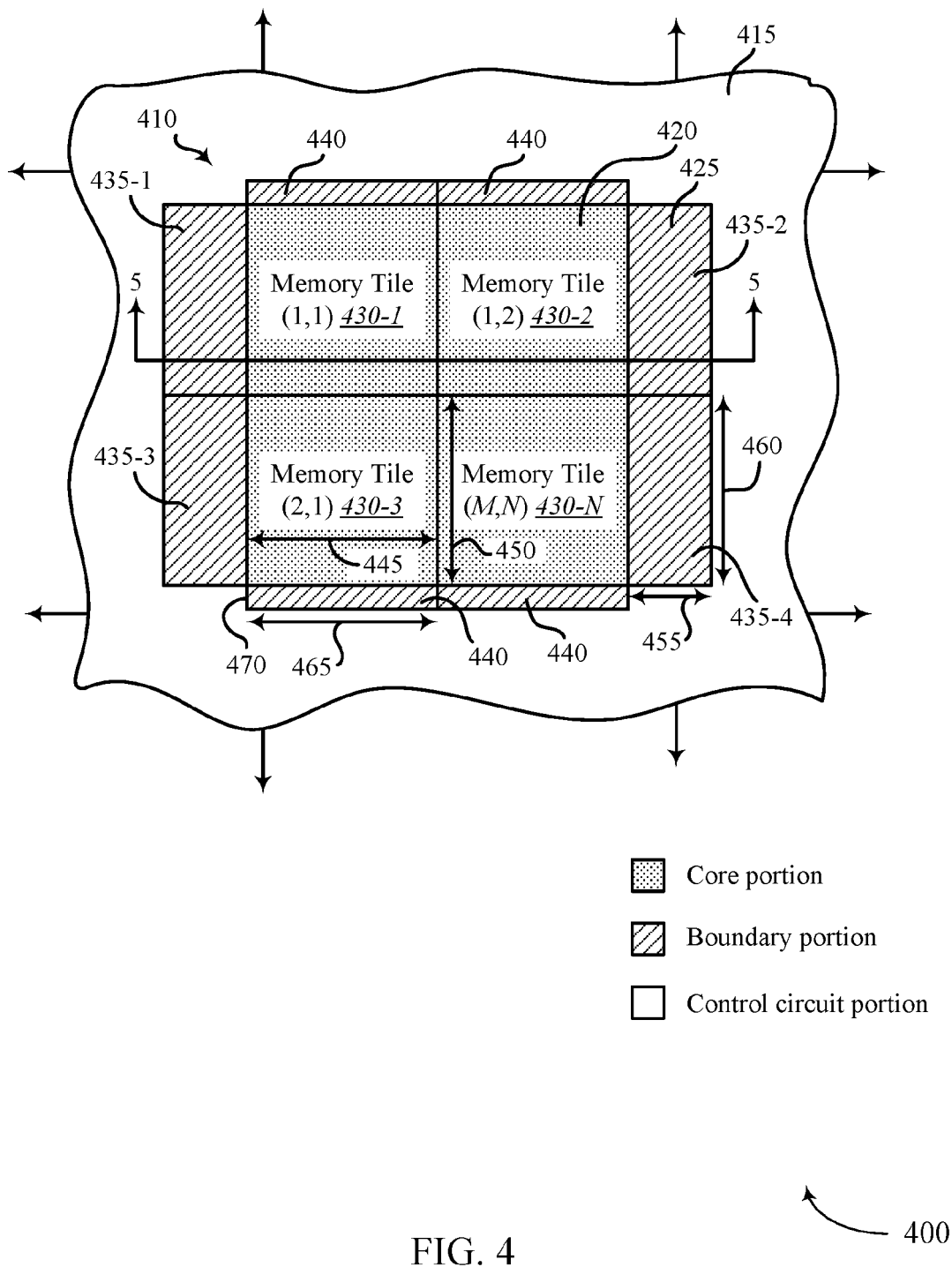
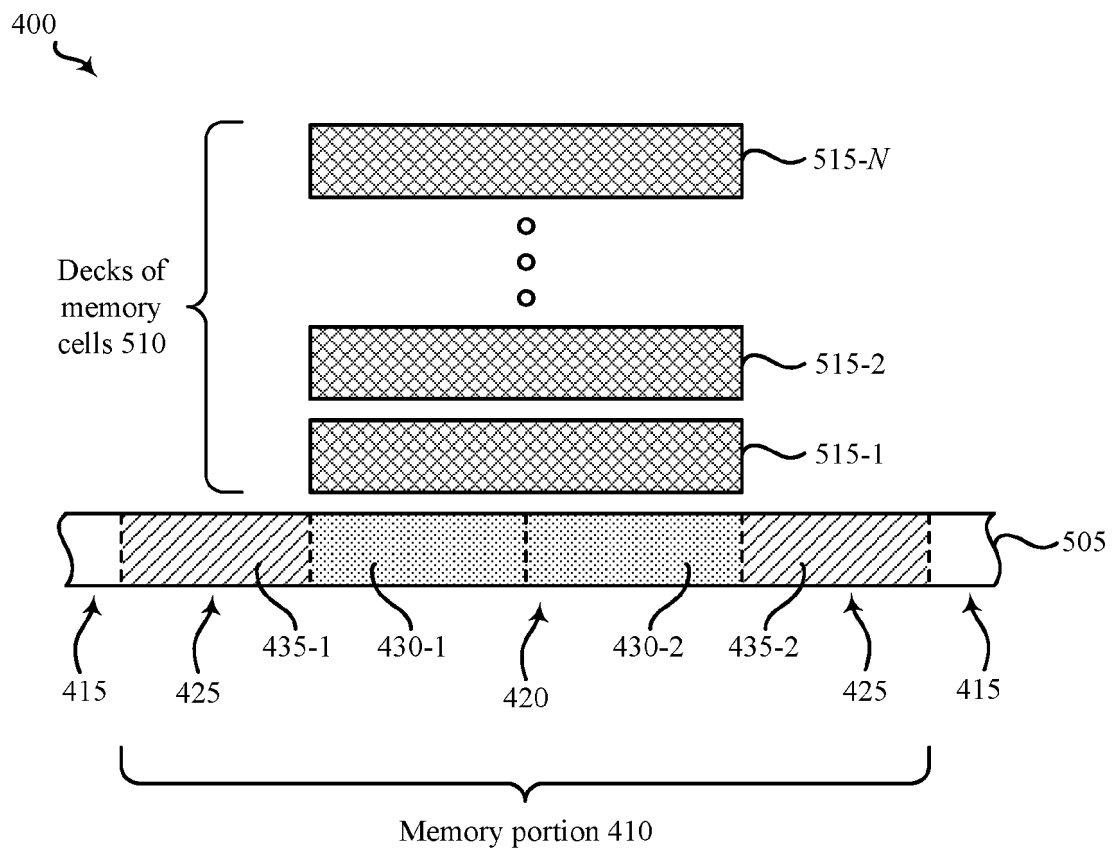


FIG. 3

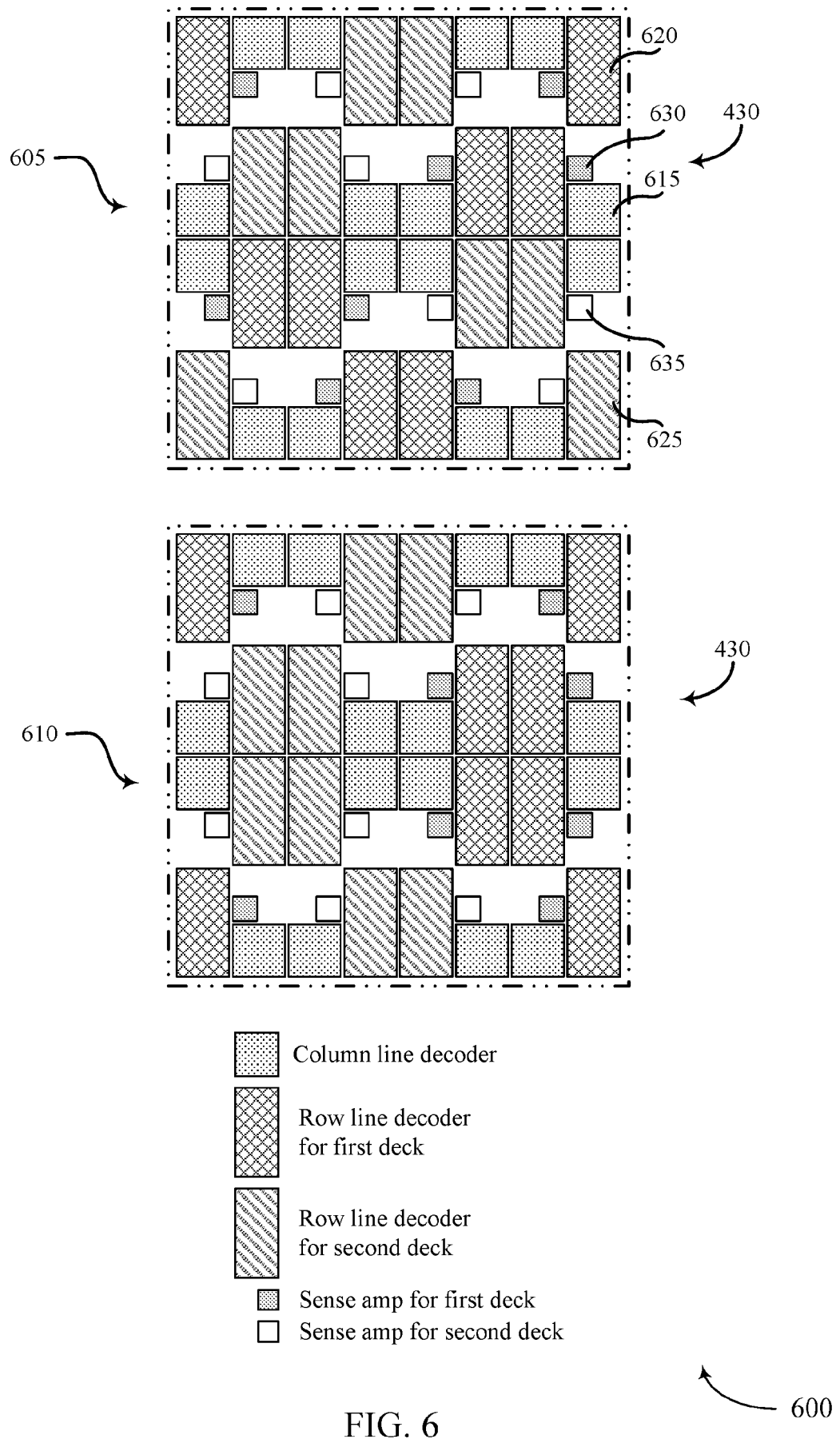




-  Core portion
-  Boundary portion
-  Control circuit portion
-  Array of memory cells

FIG. 5

500



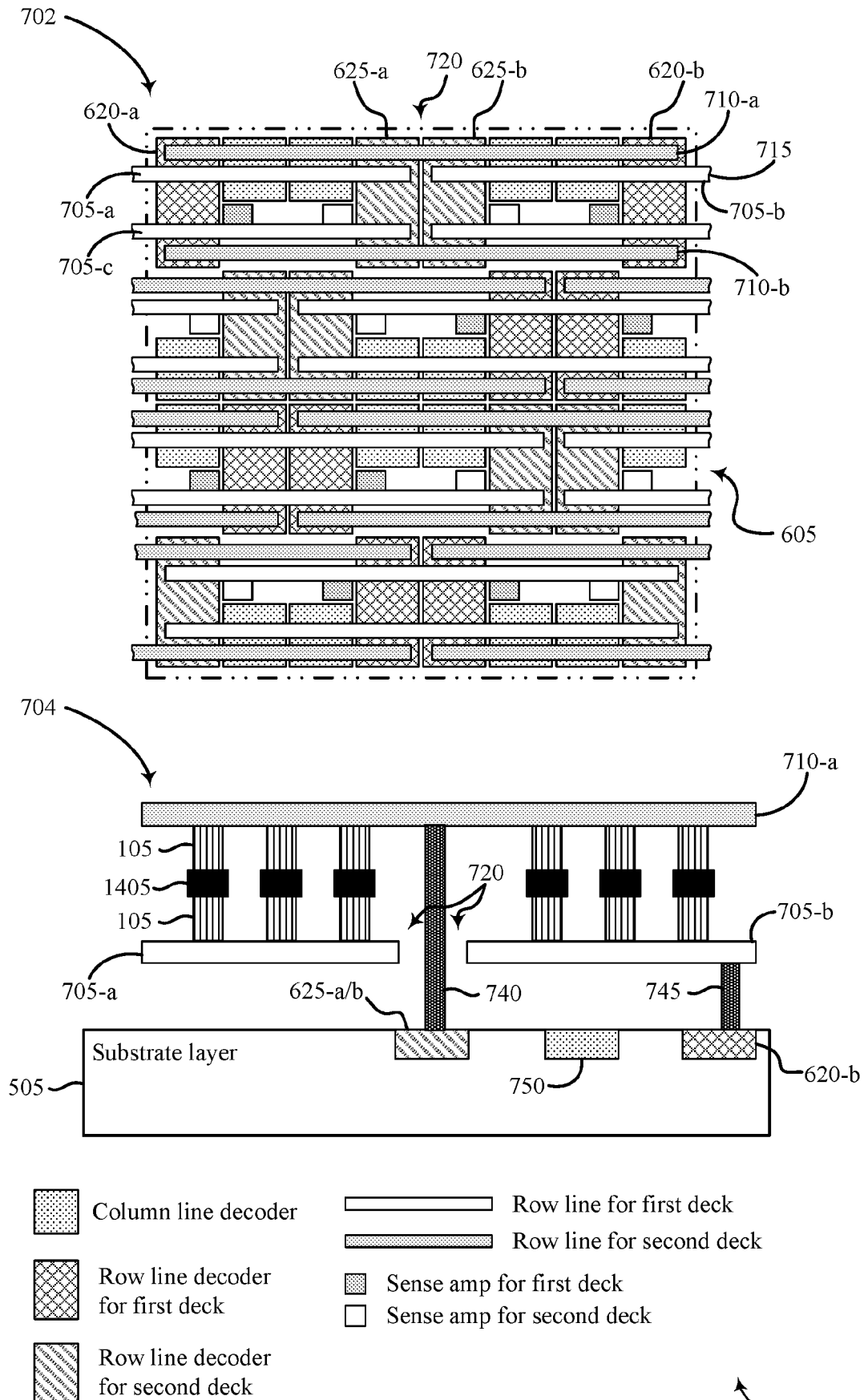


FIG. 7

700

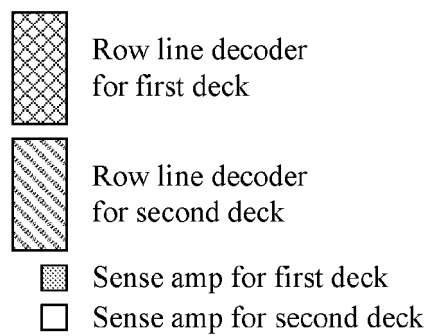
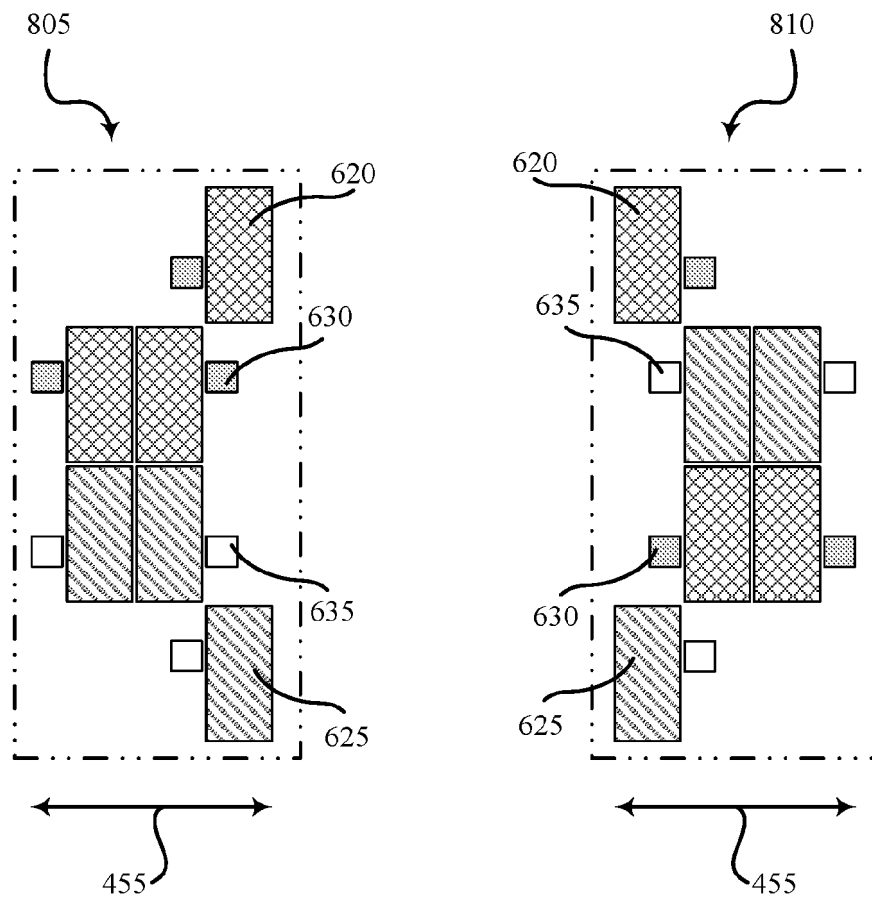
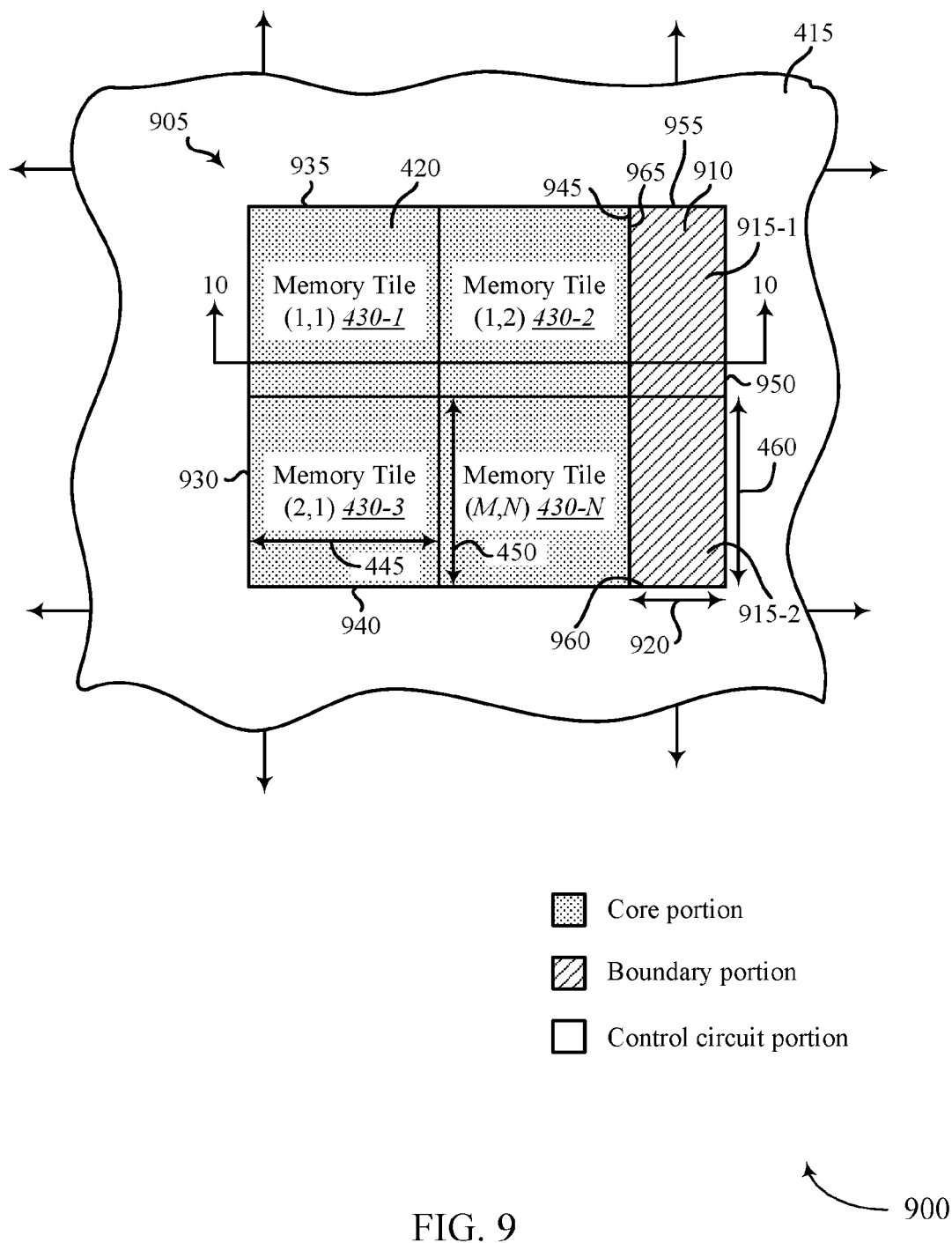


FIG. 8

800



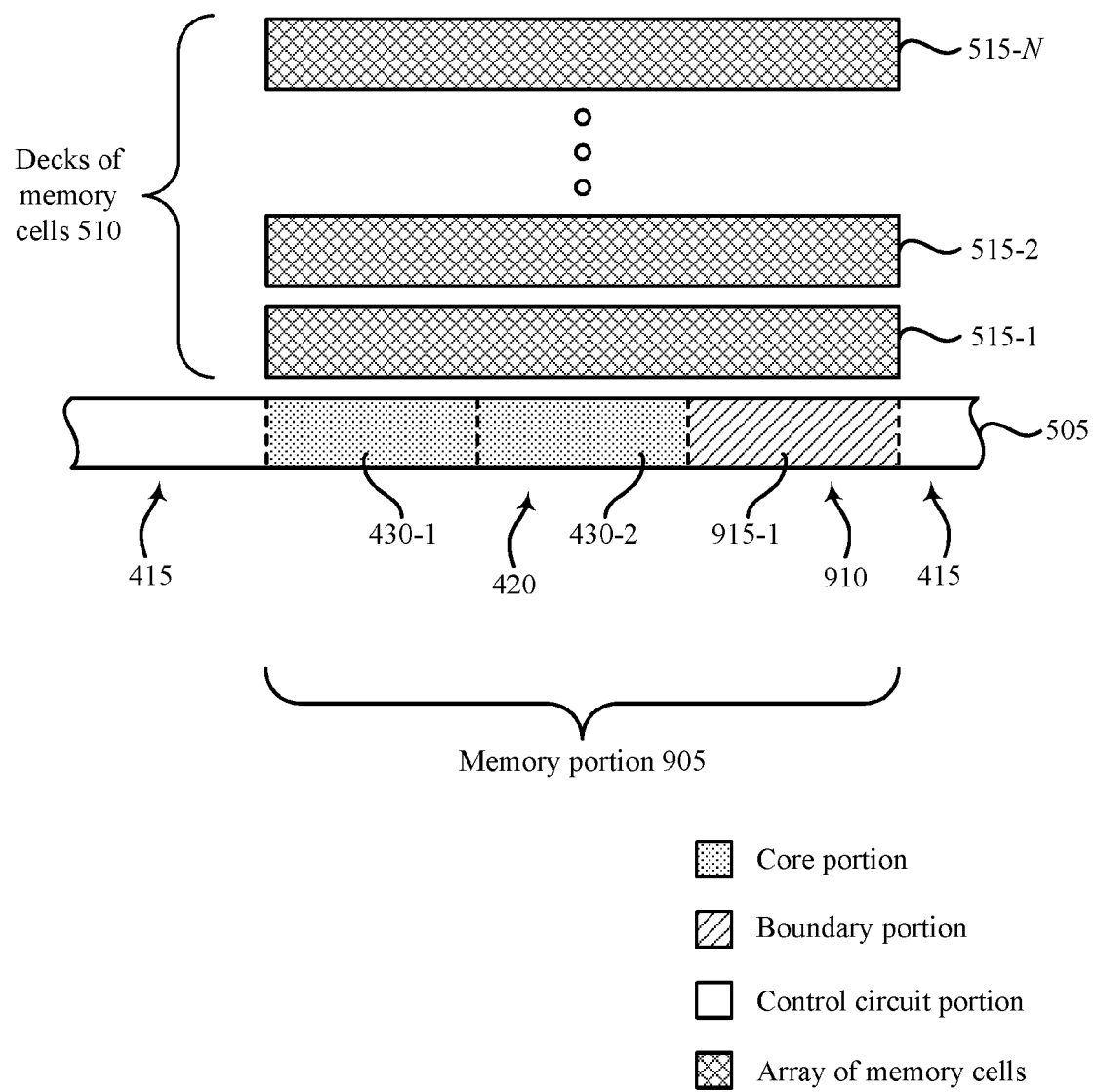


FIG. 10

1000

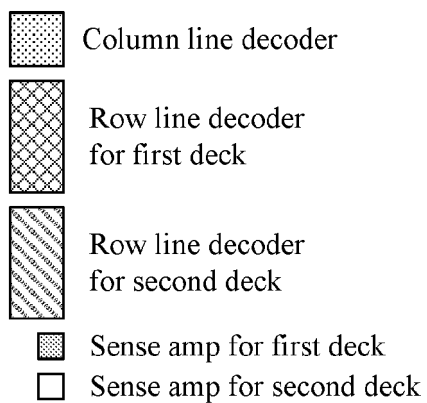
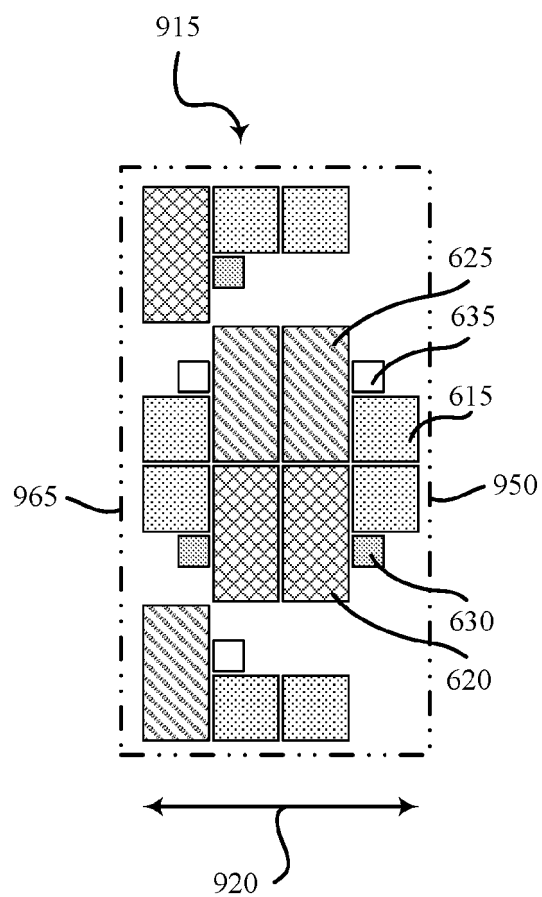
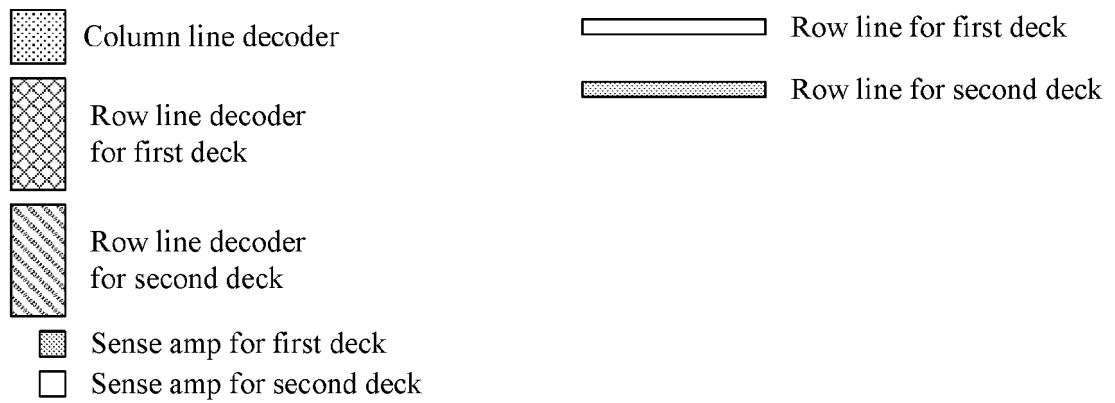
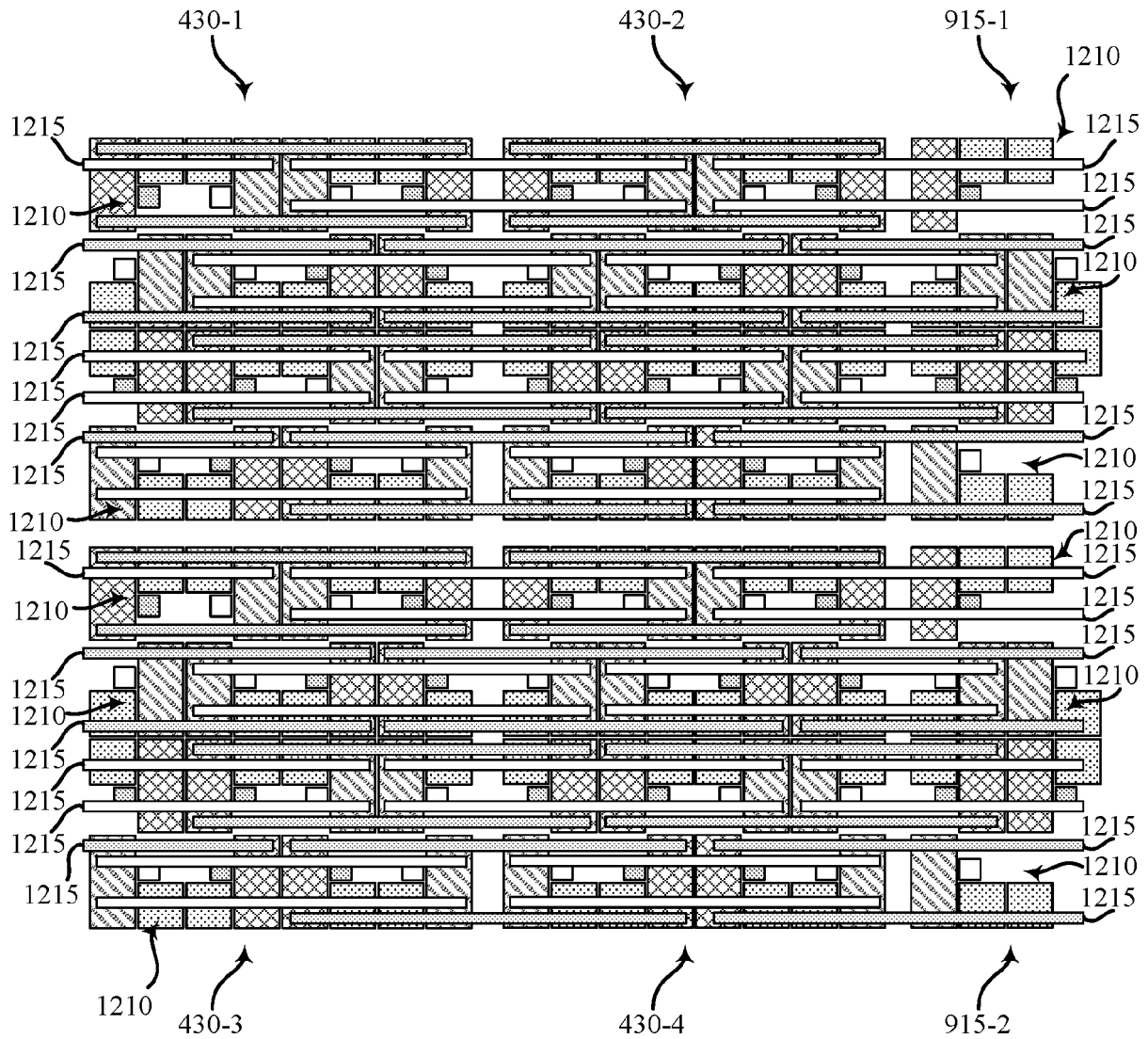


FIG. 11

1100



1200

FIG. 12

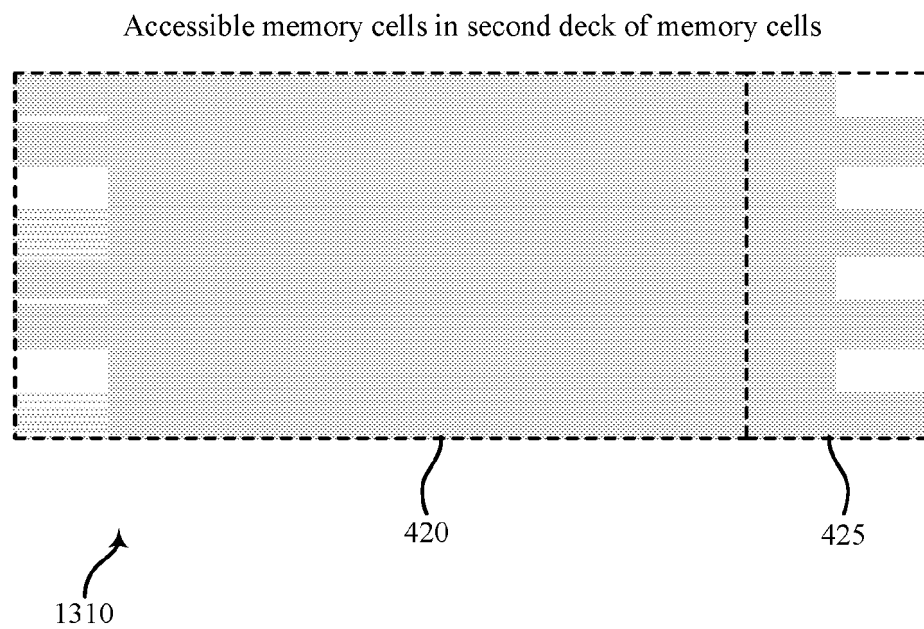
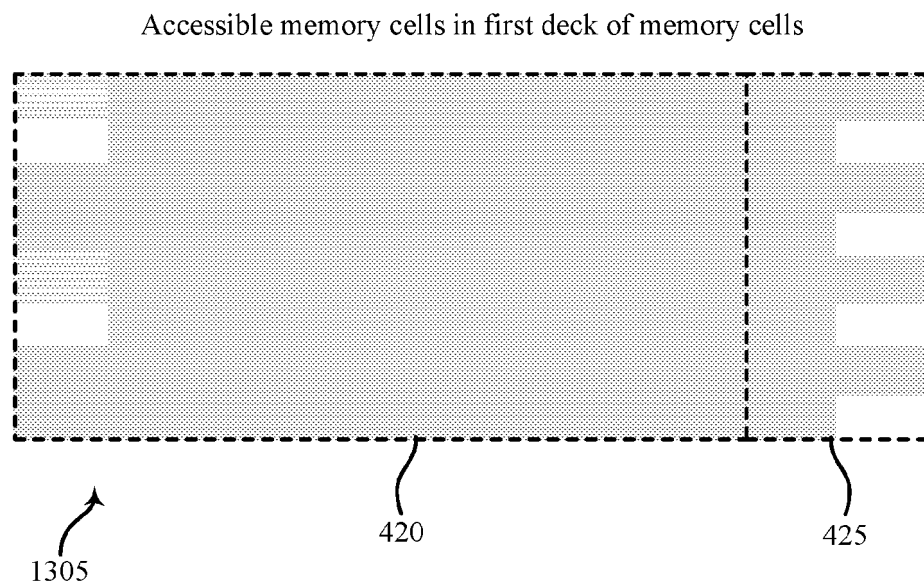
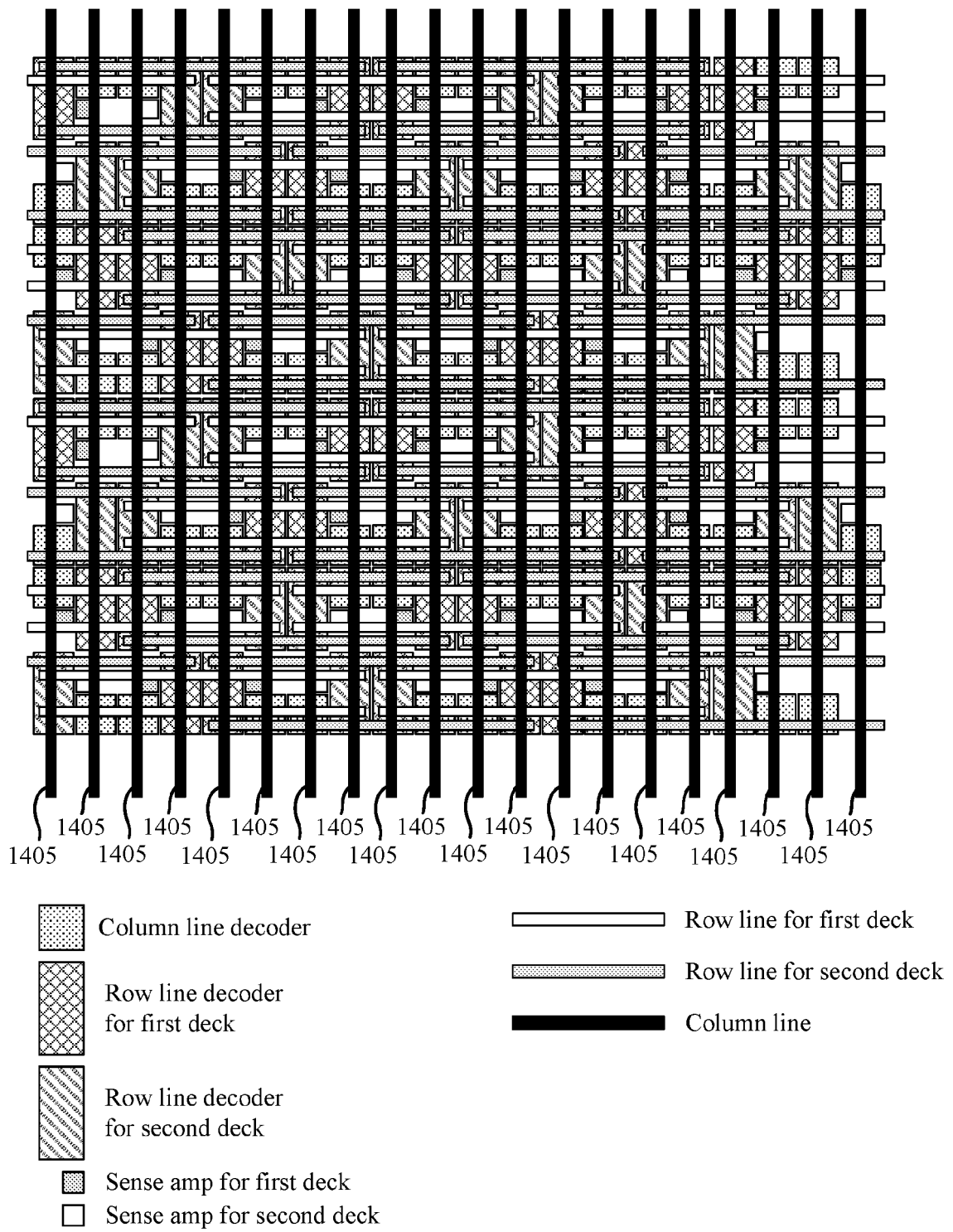


FIG. 13

1300



1400

FIG. 14



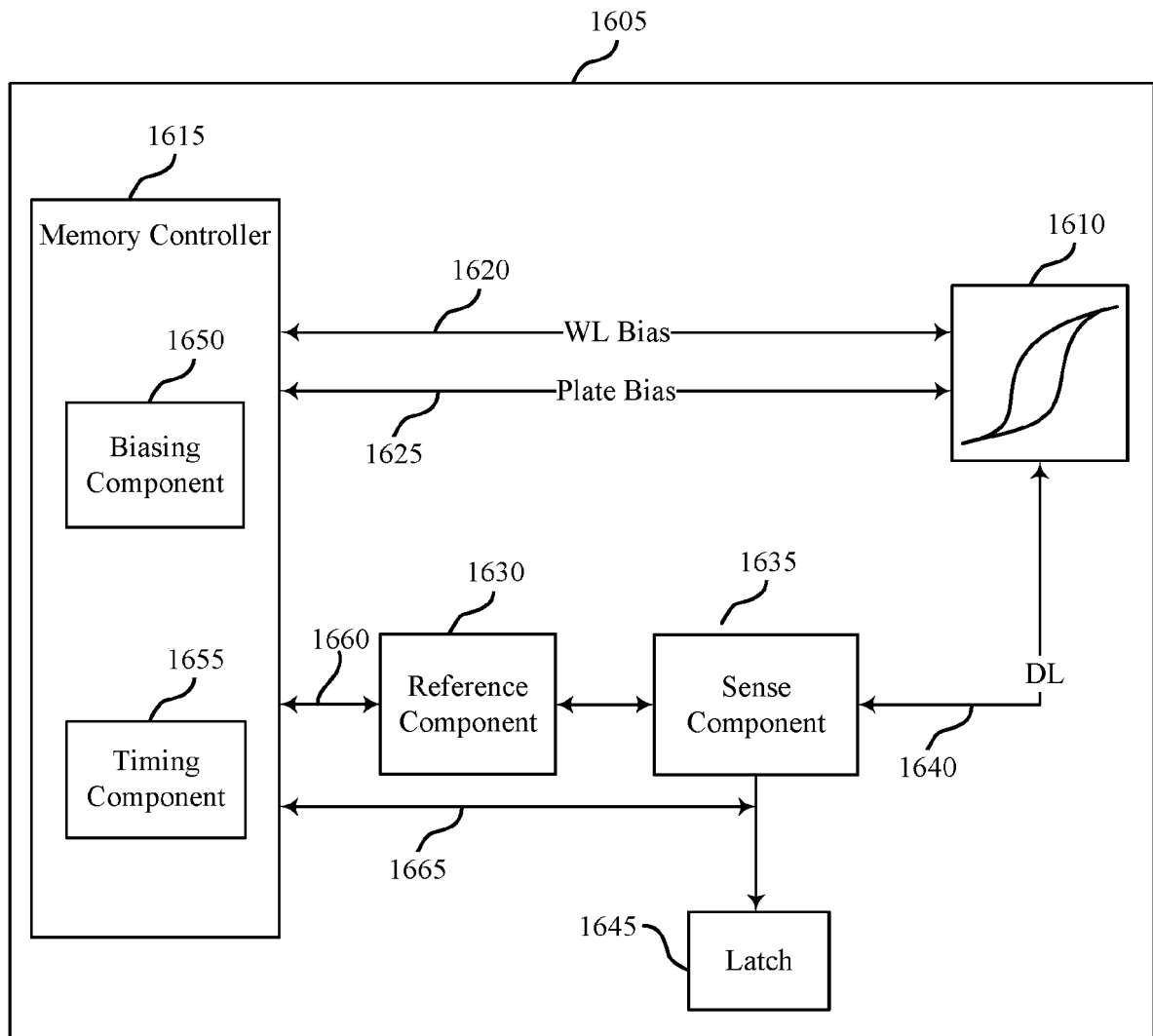


FIG. 16

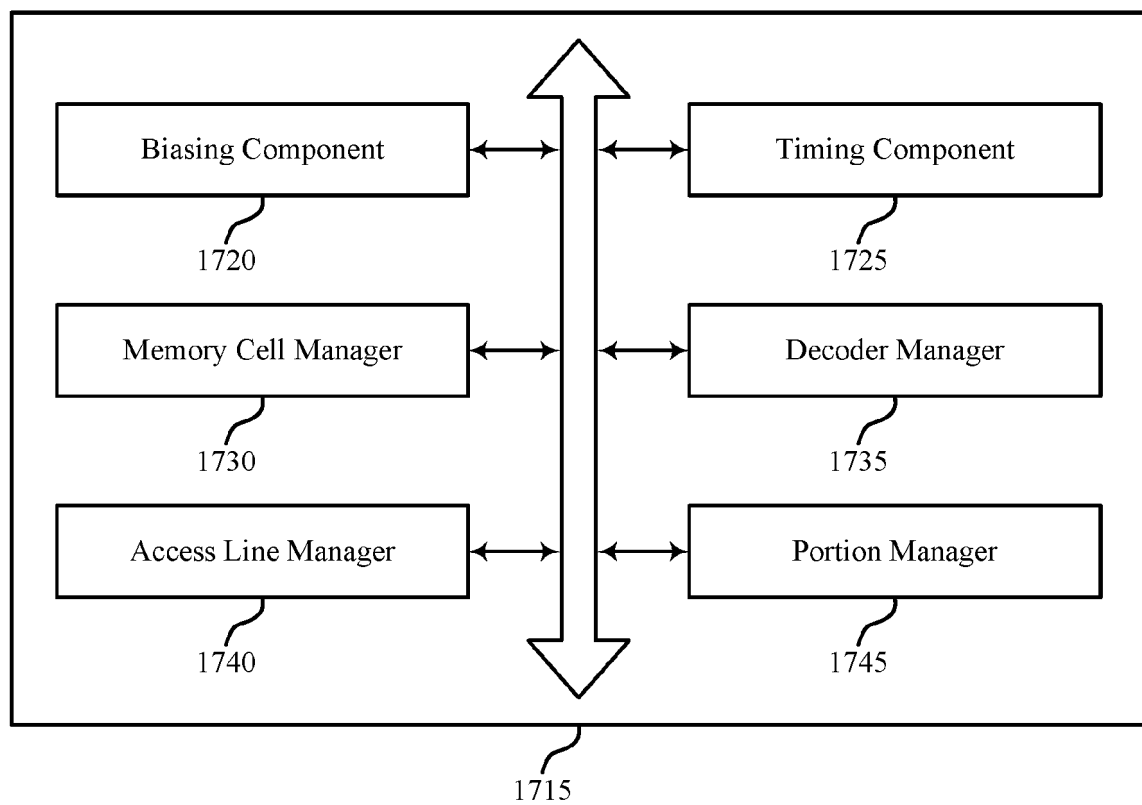


FIG. 17

1700

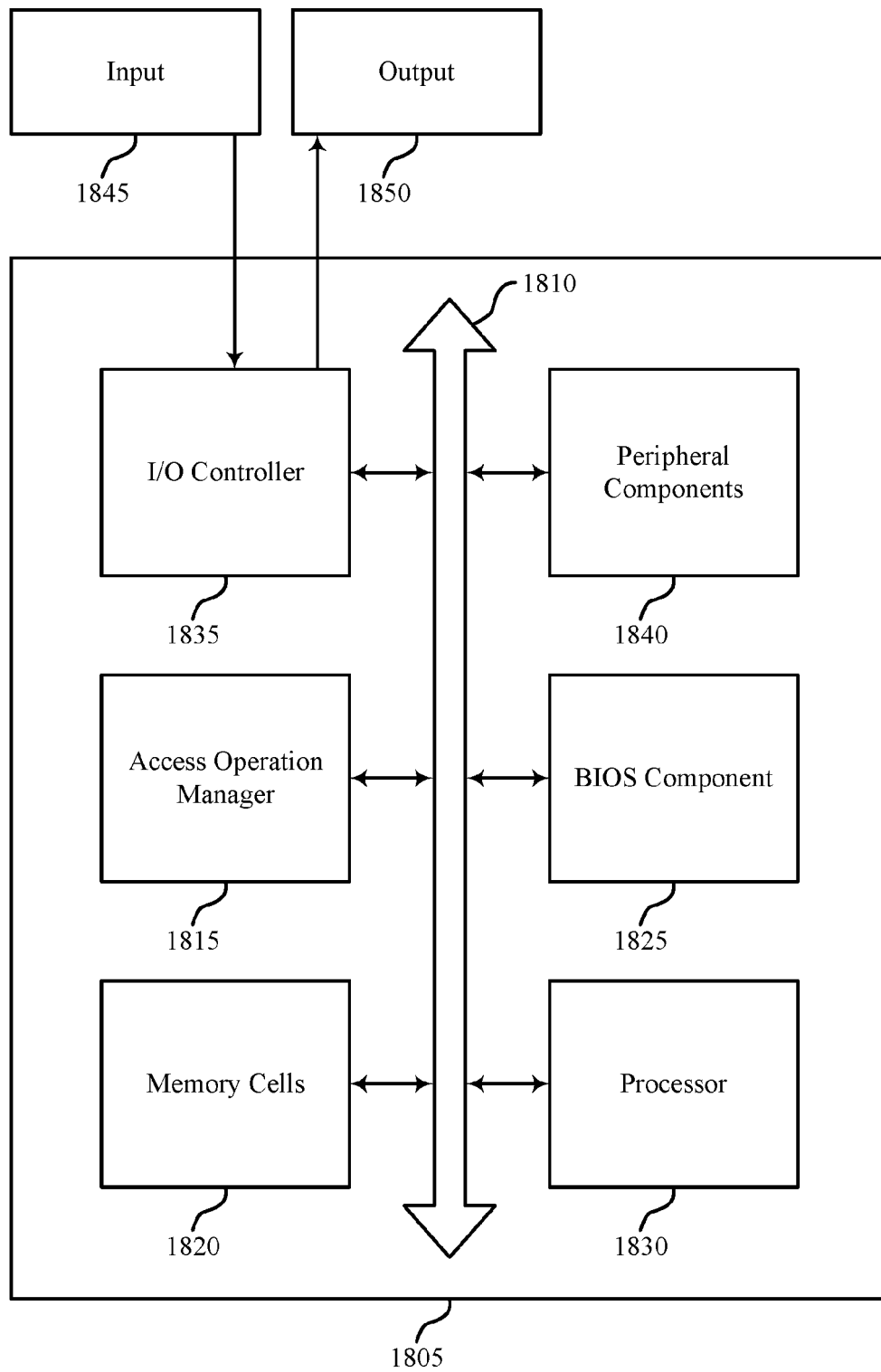


FIG. 18

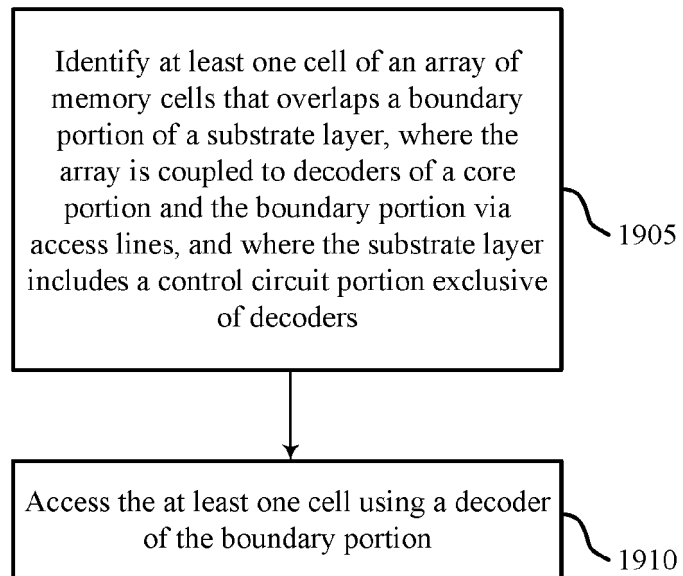


FIG. 19

1900