

Description**Background of the Invention****1. Field of the Invention**

The present invention relates to integrated circuits having a memory array and the capability for testing the memory.

2. Description of the Prior Art

The use of memory arrays integrated with logic circuitry, referred to as "embedded memories" or "application specific memories", results in a memory array that is more difficult to test than a conventional discrete memory integrated circuit (IC). This is due largely to the fact that the access to the memory array itself is limited. That is, the input/output terminals are usually devoted to the logic functions that the IC is intended to perform, and the memory array itself is not directly accessible to the user. Therefore, the testing is usually limited to storing and retrieving data through the intervening logic circuitry, which may not provide a complete test. Furthermore, even if an error is detected, it is frequently not clear whether the logic circuitry or the memory array is at fault. That information is very useful when debugging new designs, and for monitoring processing conditions during production, for example.

One technique for testing the memory array itself is to provide test pads on the integrated circuit that are devoted to the memory array. However, that results in a substantial increase in the integrated circuit area, which is not usually economically feasible. Furthermore, the time required for testing a large memory array is substantial. In addition, the package test may then not be as complete as the wafer test, reducing the ability to detect faults at the package test. Another known technique is to include on the integrated circuit a test generator that generates a known sequence of test bits that are written into the array. The test bits are then read from the array, and compared with the known pattern in a signature recognition circuit. However, the prior art techniques have not yielded as complete a test as is desired, since the signatures used have typically not simulated worst-case conditions very closely.

When the test circuitry is included on the same IC as the memory, the test circuitry should also be tested. However, this is typically very difficult using prior art test techniques. Finally, the customer logic designs of the prior art signature generation and recognition circuitry are not very regular. Hence, they are difficult to partition when computer-aided design (CAD) techniques are used, especially the CAD techniques that group the circuitry into blocks.

THE 15TH ANNUAL INTERNATIONAL SYMPOSIUM ON FAULT-TOLERANT COMPUTING, Ann Arbor, Michigan, 19th - 21st June 1985, p. 118-123, IEEE Computer Society, US, discloses an integrated circuit as set out in the preamble of claim 1. This incorporates a built-in self-test (BIST) technique for random access memories (RAMs). An address generator is used to sequentially select all the cells of the RAM, and also the reverse sequence. Control circuitry allows for selecting the type of the test sequence.

Summary of the Invention

According to the invention there is provided an integrated circuit as set out in claim 1.

A memory address generator may be used to provide the proper test bits to each location. An expected data generator and comparator circuitry may be used to compare the information read from a given memory location with the information written into that location. Alternately, signature analysis circuitry may be used for this purpose. Data compression circuitry may be included to reduce the number of test flags used to signal the results of each test.

Brief Description of the Drawing

FIG. 1 shows a memory array and various circuits for testing according to the present technique.

FIG. 2 is a typical layout of memory cells that shows the logical addresses and the physical locations.

FIG. 3 shows schematically static memory cells that each comprise two inverters.

FIG. 4 shows the physical voltage states for the cells of FIG. 3 in the layout of FIG. 2.

Detailed Description

The following detailed description relates to an integrated circuit having a memory array and a self-testing capability for the memory. Other circuitry may be included on the IC, making the memory a so-called "application specific" memory, alternately referred to as an "embedded memory". If desired, the self-test capability of the present invention may be included with a discrete (i.e. stand-alone) memory chip. The present technique will be illustrated in terms of a static memory wherein a multiple-bit word is accessed. The present technique initially writes a checkerboard pattern (alternating "1's" and "0's") into physical memory locations in the memory array. In the case of a static memory having a cross-coupled cell, this means that the alternating pattern be written so that the voltage state of adjacent inverters define the alternating pattern. The test sequence provides for reading the information from a given address location (which may comprises multiple bits), and comparing the information with the known test information for that location. The test is then performed on the next memory address, and so forth, until all of the memory address locations in the memory array have been tested. The tests may then be repeated in the reverse direction (i.e., starting at the last memory address location) if desired. Note that the present sequential read-and-compare technique is in contrast to prior art techniques that read out an entire memory array (or large portion thereof) into circuitry that compares the information with the expected test values.

In the present technique, the detection of faults is provided by the following test conditions: Condition 1: Each cell undergoes a 0 to 1 transition a 1 to 0 transition and is read after each of these transitions. Condition 2: For every pair of adjacent (in the physical layout) cells i and j, the test writes cell i with 1 and cell j with 0 cell i with 0 and cell j with 1 and reads after each of these writes. This writing sequence produces the so-called "checkerboard" pattern referred to herein. Condition 3: Each memory cell is read twice, after writing logic 1 and 0. Condition 4: Some memory words are written and read with data having different logic values (i.e. 01 and 10 pair) on every pair of adjacent input data lines. This conditions tests the comparator that is described below.

Still other conditions may be imposed. For example, after writing into a cell, a hold time delay may be included before reading the cell. This tests for open conductors that make static memories behave as dynamic memories, and for capacitor hold time in the case of dynamic memories.

Referring to FIG. 1, a typical random access memory layout is illustrated, wherein the memory array is divided into a number of segments. Each segment includes a multiplicity of adjacent columns. A single column is selected from each segment during a given read or write access operation. Therefore, the illustrative design provides for 4 bit access, with the present technique being useful with designs simultaneously accessing any number of multiple bits, or even only a single bit as noted below. The information accessed at a given memory address is referred to as a "word" herein, so that a 4 bit word is illustrated herein. To select a given word, address input circuitry provides address bits (A3...A5) to a row decoder to select a unique one of the rows, and also address bits (A1...A2) to a column decoder, which selects a unique one of the columns from each segment. The intersection of the selected row and columns determines the position of the word in the physical layout. One possible data bit mapping scheme from the word address to the physical word location, is illustrated in FIG. 2. The address (ADD) is indicated, with each address comprising four bits (D1...D4). For example, address ADD 5 is physically located in row W2, columns 4, 8, 12 and 16. The following discussion will refer to the mapping of FIG. 2, with others being possible.

The present invention provides that in the case of memory cells having cross-coupled inverters, the checkerboard test pattern that is initially written into the memory array is defined by the inverter locations, rather than by the cells alone. For example, referring to FIG. 3, two 6 transistor "full CMOS" static memory cells are shown, with 4 transistor static cells (including two load resistors) being comparable for purposes of the present invention. The cells are located in adjacent columns (3 and 4) and along a common row (1). Each cell comprises two cross-coupled inverters, with transistors 302-303 and 304-305 forming inverters INV1 and INV2, respectively. The inverters are cross-coupled, thereby producing bi-stable voltage states so that when node 307 is high, then node 308 is low, and vice-versa. Node 307 is accessed by the "true" bit line D1 through access transistor 301, whereas node 308 is accessed by the "complement" bit line D1 (BAR) through access transistor 306. Note that inverter INV2 is physically adjacent to inverter INV3 in the adjacent memory cell. Hence, in writing a checkerboard pattern into the array according to the present inventive technique, node 308 is placed in the opposite voltage state as node 309. This is accomplished by either writing a "1" into both of the two adjacent cells shown, or by writing a "0" into both cells, considering that the stored memory state of a given cell is defined by the node accessed by the "true" bit line. Dynamic memory cell arrays may also be tested by the present technique, including dynamic cells using cross-coupled transistors that produce nodes at opposite voltage states, which are known in the art.

If the pattern of "true" and "complement" bit lines continues as shown along an entire row, then an entire row of cells will be logically written with all "1's" or alternately all "0's" to obtain the desired physical checkerboard pattern of voltage states along the row (horizontal axis as viewed in FIG. 3). However, in some memory designs, the "true" and "complement" bit lines are mirror images between adjacent cells, as taken along the axis of symmetry A-A shown. Therefore, in such designs, the cells in a given row are written with alternating logical "1's" and "0's" to obtain the checkerboard voltage pattern in the physical inverter locations along the row. Still other arrangements of the bit lines are possible, with corresponding changes in the logical information written into the cells to obtain the physical checkerboard pattern. Note also that to obtain the checkerboard, the stored voltage states are also alternated in the vertical axis, as viewed in FIG. 3. That is, the cells in row 2 (below row 1 as viewed) have the opposite voltage state as those in row 1. Hence, if all logic "1's" are stored in row 1, then all logic "0's" are stored in row 2, and so forth for the remaining rows. The stored voltage states for the arrangement of FIG. 2 and memory cells of FIG. 3 are shown in FIG. 4, wherein the state of each inverter is indicated. The inverter that is accessed by the true bit line is referred to as the "master" (M), and the inverter accessed by the complement bit line as the "slave" (S), for each memory cell.

After initializing the array in the checkerboard pattern, the array is written with the inverse pattern (the "inverse checkerboard"), wherein the 1's and 0's are interchanged, in a subsequent pass through the array. This provides for testing the transition between the 0 and 1 states for each cell. A subsequent pass in the reverse direction then writes the initial checkerboard pattern into the cell, to check for transitions that may be affected by neighboring cells on the opposite side as those that could affect the test in the forward direction.

A presently preferred sequence of read and write operations that achieves the above conditions is as follows, wherein a pair of operations (e.g., write-read) implies that the operations are performed on a given word address before moving to the the next address. That is, the address counter increments by 1 digit in the forward direction, and decrements by 1 digit in the reverse direction. Hence, each read or write accesses 4 bits in the illustrative case. As indicated, the tests are performed in several passes through the entire memory array, starting from either the first memory address (forward direction), or from the last memory address (reverse direction). The "first" memory address is conventionally considered to be the 0...0 address, and the "last" memory address is conventionally considered to be the 1...1 address, but these designations may be reversed insofar as the present invention is concerned. Note also that the initial checkerboard pattern may begin with either a 1 or a zero.

TABLE

SELF-TEST SEQUENCE		
OPERATION	PATTERN	ADDRESS DIRECTION
Write-Read	Checkerboard	Forward
Read-Write	Inverse Checkerboard	Forward
Read-Read	"	Forward
Read-Write	Checkerboard	Reverse
Read-Read	"	Reverse

Still other operations may be added in either the forward or reverse direction as desired. One significant feature of this sequence is the "double read", wherein two read operations are performed sequentially (without an intervening write operation) on a given memory word. This double read provides a test to determine whether the read operation itself affects the information stored in the word. Additional reads may be provided if desired (producing, e.g., a triple read).

A significant feature of operating on one memory address at a time is that the information read out of that location may be readily compared with the information written into that location. Furthermore, by performing the operations on sequential memory locations, both the word address and the test information written into the word may be readily generated by an address counter. Referring again to FIG. 1, the address register serves as an address counter when in the self-test mode. A read/write register (C1) and a control register (C2...C4), under the control of a system clock determines whether a read or write test operation is being performed. And address bits A1...A5 are incremented (or decremented) so as to produce the desired address sequence through the memory array during a test. Furthermore, control register bits C2, C3 and C4 are used to determine which of the five memory test operations in the above Table are

being conducted. The Data In Generator produces the actual test data read into each word (4 bits per word in the illustrative case), whereas the Expected Data Generator provides an identical test word for comparison in the comparator. The Expected Data Generator function may be combined with the Data In Generator. However, they are desirably separate to provide a self-check of the Data In Generator. The Comparator provides a comparison on each bit of the test word read out of the memory array during a read operation. If the bits are identical with those from the Expected Data Generator, then a "pass" signal is sent from the comparator; otherwise, a "fail" signal is sent. The output of the comparator is sent to a Data Compression circuit in the preferred embodiment, so that if any one of the test words fail in the entire array, then a "flag" is set to the "fail" state, and supplied to an external terminal of the integrated circuit. In this manner, the self-test may be conducted even after the integrated circuit is packaged and operating in a system, if desired. An additional test may be provided by the test circuitry that allows full testing of the comparator and all data columns adjacent to each other. This test moves a logic 0 through a field of logic 1's in a data word that is both written and read for each bit position of the zero in the word. This is followed by a comparable test that moves a logic 1 through a field of logic zeros in a data word.

As an alternative to the test comparator shown herein, signature analysis techniques may be used. In that case, each read of a word under test places the information in a test register, after performing a logical "OR" with the previous contents of the register. Each bit of the test register is then compared to an expected value that may be stored in a read only memory (ROM), which may be either on the same chip as the test circuitry, or on an external chip. Thus, by combining several words before examining the test register, the test data is "compressed" in this case also, so that relatively fewer bits need to be examined than the total read out of the word under test.

Claims

1. An integrated circuit comprising an array of memory cells, and address decoding circuitry for accessing a word of information in said array for each word address supplied thereto,
said integrated circuit further comprising self-test circuitry comprising address counter means for providing sequential word addresses to said decoding circuitry, means for writing test information into each word so as to produce a pattern of logic 1 and 0 test voltage states in said array, means for reading each word after writing test information into the word, and means for compressing the test information read from the words in said array, characterized in each cell has two nodes at opposite voltage levels and that said test information is written into physically adjacent memory locations such that adjacent nodes of adjacent memory cells are at opposite voltage levels and form a checkerboard pattern of alternating 1 and 0 states.
2. The integrated circuit of claim 1 further comprising means for writing the inverse of said checkerboard pattern of alternating 1's and 0's into adjacent memory locations of said array.
3. The integrated circuit of claim 1 further comprising means for reading the test information from a given word at least twice without an intervening write operation into the given word.
4. The integrated circuit of claim 1 wherein said address counter means provides for at least one forward test sequence of addresses beginning at the first memory word address and ending at the last memory address, and at least one reverse test sequence of addresses beginning at the last memory word address and ending at the first memory word address.
5. The integrated circuit of claim 1 wherein said self-test circuitry provides for test operations in a given word address direction comprising the following: write-read, forward; read-write, forward; read-read, forward; read-write, reverse; and read-read, reverse.
6. The integrated circuit of claim 1 wherein said means for writing test information into the words is controlled by said address counter means.
7. The integrated circuit of claim 1 wherein each word comprises a multiplicity of memory cells.
8. The integrated circuit of claim 1 wherein each memory cell is a static memory cell comprising a pair of cross-coupled inverters.

Compression circuit in the preferred embodiment, so that if any one of the test words fail in the entire array, then a "flag" is set to the "fail" state, and supplied to an external terminal of the integrated circuit. In this manner, the self-test may be conducted even after the integrated circuit is packaged and operating in a system, if desired. An additional test may be provided by the test circuitry that allows full testing of the comparator and all data columns adjacent to each other. This test moves a logic 0 through a field of logic 1's in a data word that is both written and read for each bit position of the zero in the word. This is followed by a comparable test that moves a logic 1 through a field of logic zeros in a data word.

As an alternative to the test comparator shown herein, signature analysis techniques may be used. In that case, each read of a word under test places the information in a test register, after performing a logical "OR" with the previous contents of the register. Each bit of the test register is then compared to an expected value that may be stored in a read only memory (ROM), which may be either on the same chip as the test circuitry, or on an external chip. Thus, by combining several words before examining the test register, the test data is "compressed" in this case also, so that relatively fewer bits need to be examined than the total read out of the word under test.

Claims

1. An integrated circuit comprising an array of memory cells, and address decoding circuitry for accessing a word of information in said array for each word address supplied thereto,
said integrated circuit further comprising self-test circuitry comprising address counter means for providing sequential word addresses to said decoding circuitry, means for writing test information into each word so as to produce a pattern of logic 1 and 0 test voltage states in said array, means for reading each word after writing test information into the word, and means for compressing the test information read from the words in said array, characterized in each cell has two nodes at opposite voltage levels and that said test information is written into physically adjacent memory locations such that adjacent nodes of adjacent memory cells are at opposite voltage levels and form a checkerboard pattern of alternating 1 and 0 states.
2. The integrated circuit of claim 1 further comprising means for writing the inverse of said checkerboard pattern of alternating 1's and 0's into adjacent memory locations of said array.
3. The integrated circuit of claim 1 further comprising means for reading the test information from a given word at least twice without an intervening write operation into the given word.
4. The integrated circuit of claim 1 wherein said address counter means provides for at least one forward test sequence of addresses beginning at the first memory word address and ending at the last memory address, and at least one reverse test sequence of addresses beginning at the last memory word address and ending at the first memory word address.
5. The integrated circuit of claim 1 wherein said self-test circuitry provides for test operations in a given word address direction comprising the following: write-read, forward; read-write, forward; read-read, forward; read-write, reverse; and read-read, reverse.
6. The integrated circuit of claim 1 wherein said means for writing test information into the words is controlled by said address counter means.
7. The integrated circuit of claim 1 wherein each word comprises a multiplicity of memory cells.
8. The integrated circuit of claim 1 wherein each memory cell is a static memory cell comprising a pair of cross-coupled inverters.



bei der jedes Wort eine Vielzahl von Speicherzellen umfaßt.

8. Integrierte Schaltung nach Anspruch 1, bei der jede Speicherzelle eine statische Speicherzelle mit einem Paar von kreuzgekoppelten Invertern ist.
9. Integrierte Schaltung nach Anspruch 1, bei der jede Speicherzelle eine dynamische Speicherzelle mit einem Paar von kreuzgekoppelten Transistoren ist.



10. Intégrée Schaltung nach Anspruch 1,
mit einem Generator für erwartete Daten und einem Komparator, der die aus jedem Wort gelesenen
Prüfdaten mit den von dem Generator erzeugten Daten vergleicht.

5 11. Intégrée Schaltung nach Anspruch 1,
mit einer Kennwert-Analyseschaltung zur Feststellung, ob die aus jedem Wort gelesenen Prüfdaten
richtig sind.

Revendications

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1. Un circuit intégré comprenant un réseau de cellules de mémoire; et un circuit de décodage d'adresse
pour accéder à un mot d'information dans ce réseau pour chaque adresse de mot qui lui est appliquée,
ce circuit intégré comprenant en outre un circuit d'auto-test qui comprend des moyens compteurs
d'adresse destinés à fournir des adresses de mot séquentielles au circuit de décodage, des moyens
15 pour écrire de l'information de test dans chaque mot, afin de produire dans le réseau une configuration
d'états logiques de tension de test 1 et 0, des moyens pour lire chaque mot après l'écriture
d'information de test dans le mot, et des moyens pour comprimer l'information de test qui est lue dans
les mots dans le réseau, caractérisé en ce que

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chaque cellule comprend deux noeuds à des niveaux de tension opposés;
et en ce que l'information de test est écrite dans des positions de mémoire physiquement
adjacentes, de façon que des noeuds adjacents de cellules de mémoire adjacentes soient à des
niveaux de tension opposés et forment une configuration en damier d'états 1 et 0 alternés.

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2. Le circuit intégré de la revendication 1, comprenant en outre des moyens pour écrire l'inverse de la
configuration en damier de 1 et de 0 alternés dans des positions de mémoire adjacentes du réseau.

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3. Le circuit intégré de la revendication 1, comprenant en outre des moyens pour lire au moins deux fois
l'information de test provenant d'un mot donné, sans une opération d'écriture intermédiaire dans le mot
donné.

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4. Le circuit intégré de la revendication 1, dans lequel les moyens compteurs d'adresse produisent au
moins une séquence d'adresses de test de direction avant, commençant à la première adresse de mot
de mémoire et se terminant à la dernière adresse de mémoire, et au moins une séquence d'adresses
de test de direction arrière, commençant à la dernière adresse de mot de mémoire et se terminant à la
première adresse de mot de mémoire.

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5. Le circuit intégré de la revendication 1, dans lequel le circuit d'auto-test effectue des opérations de test
dans une direction d'adresse de mot donnée, comprenant les opérations suivantes : écriture-lecture en
avant; lecture-écriture en avant; lecture-lecture en avant; lecture-écriture en arrière; et lecture-lecture en
arrière.

6. Le circuit intégré de la revendication 1, dans lequel les moyens qui sont destinés à écrire de
l'information de test dans les mots sont commandés par les moyens compteurs d'adresse.

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7. Le circuit intégré de la revendication 1, dans lequel chaque mot comprend une multiplicité de cellules
de mémoire.

8. Le circuit intégré de la revendication 1, dans lequel chaque cellule de mémoire est une cellule de
mémoire statique qui comprend une paire d'inverseurs en couplage croisé.

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9. Le circuit intégré de la revendication 1, dans lequel chaque cellule de mémoire est une cellule de
mémoire dynamique qui comprend une paire de transistors en couplage croisé.

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10. Le circuit intégré de la revendication 1, comprenant un générateur de données prévues et un
comparateur pour comparer les données de test qui sont lues dans chaque mot avec les données que
génère le générateur de données prévues.



11. Le circuit intégré de la revendication 1, comprenant un circuit d'analyse de signature pour déterminer si les données de test qui sont lues dans chaque mot sont correctes.

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