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IPOS'S

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SYSTEM WITH MESHED POWER AND SIGNAL BUSES ON CELL ARRAY

Cross Reference

This application claims the benefit of U.S. Provisional Application No. 60/005,502, filed Nov. 9, 1995.

Field of the Invention

The invention relates generally to semiconductor circuit design and, more particularly, to a method and apparatus for interconnecting power and signal buses in an integrated circuit.

Background of the Invention

As semiconductor technology develops, the number of transistors included in a single integrated circuit, or "chip," is becoming larger and the design rule parameters therefore are becoming smaller. These two developments contribute to increased metal layer resistance and to difficulties associated with this increased resistance. Such difficulties include ground bounce, cross talk noise, and circuit delays. All of these difficulties slow down chip operation and may even corrupt data stored on the chip. Eliminating the impact of increased metal layer resistance is an important design challenge in most semiconductor designs, including designs for dynamic random access memory (DRAM) devices.

One solution to this problem has been the development of a meshed power bus system for the chip, as described in Yamada, *A 64-Mb DRAM with Meshed Power Line*, 26 IEEE Journal of Solid-State Circuits 11 (1991). A meshed power bus system is readily implemented in integrated circuits like DRAMs because of their large arrays of memory cells and the presence of distributed sense amplifier drivers. The meshed system supplies

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adequate power to the distributed sense amplifier drivers because the system has many power buses running in both horizontal and vertical directions across the arrays.

The Yamada meshed system may be implemented using a conventional complimentary metal oxide semiconductor (CMOS) technology, including first, second and third metal layers, each electrically isolated from each other, wherein the first metal layer represents the lowest metal layer, the third metal layer represents the upper-most metal layer, and the second metal layer lies between the first and third layers. The Yamada meshed system is constructed in the second and third metal layer and includes a positive supply voltage (VDD) mesh and a negative supply voltage (VSS) mesh, for the VDD power buses and the VSS power buses, respectively. Conventional designs have these meshes running over the memory array and connecting at the sense amplifiers. Connections are made using through-holes, located in the area of the sense amplifier circuits. However, the presence of VDD and VSS power buses in the sense amplifiers is unnecessary, since these circuits do not require either VDD or VSS power buses, except for well bias.

As a result, the sense amplifiers, due to their relatively small size and numerous associated signal and power buses, are adversely affected by the Yamada meshed system. The Yamada meshed system overcrowds the sense amplifiers with additional power and signal buses. In addition, the metal line width required for overlapping through-holes is larger than the minimum metal line width and therefore increases the width of the metal layers even further. As a result, the metal layer over the sense amplifiers becomes determinative of the size of the sense amplifier circuits. Accordingly, their size reduction must be realized by tightening the metal width, inevitably resulting in increased resistance and slower operation.

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In addition to the Yamada meshed system, other proposals have been made for conventional DRAM design. Recently, a hierarchical word line scheme was proposed in K. Noda et Al., *a Boosted Dual Word-line Decoding Scheme for 256 Mbit DRAM's*, 1992 Symp. on VLSI Circuits Dig. of Tech. Papers, pp. 112-113 (1992). The Noda scheme includes main word lines, constructed in the second metal line layer, and subword lines constructed in a poly silicon layer. The Noda scheme describes two main word lines (one true, one bar) for every eight subword lines, and is thereby able to relax the main word line pitch to four times that of the subword line. However, this pitch would not support an improved meshed power and signal bus system.

Consequently, there is a need for a meshed power and signal bus system on an array-type integrated circuit that does not limit mesh through-hole connections to the area of the sense amplifiers, but provides for such connections at other locations on the array, thereby allowing for a relaxed metal width over the sense amplifiers and a reduction of the overall area of the chip with lower power bus resistance.

Furthermore, there is a need for a hierarchical word line scheme that supports an improved meshed power and signal bus system, that has a main word line pitch greater than four times that of the subword line pitch.

Summary of the Invention

The present invention, accordingly, is a method and apparatus for providing a meshed power bus and signal bus system on an array-type integrated circuit that does not limit mesh through-hole connections to the area of the sense amplifiers, but provides for these connections at other locations on the array, thereby allowing for a relaxed metal width over the sense amplifiers, faster sense amplifier operation, and chip size reduction. The through-holes for the mesh system are located in the cell array instead

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of, or in addition to, being located in the area of the sense amplifier circuits. This utilizes the available space for through-holes in the array, and allows for more efficient use of power and signal buses in the sense amplifiers.

The invention includes an array of DRAM memory cells, arranged as a plurality of subarrays and selected by main address decoders. Each subarray is surrounded by a plurality of sense amplifiers circuits, subdecoder circuits, and VDD, VSS and signal buses connecting to and running across the subarray. The VDD buses run in both vertical and horizontal directions across the subarray, with all the vertical buses lying in the third metal layer and all the horizontal buses lying in the second metal layer, thereby creating a VDD mesh. The buses in each layer are connected to each other using through-holes located in the memory cell subarray as well as on the sense amplifier area. Likewise, a VSS mesh and/or a signal mesh is created using through-holes located on the memory cell subarray. Once connected, the buses extend to the appropriate circuits, such as sense amplifier drive circuits, and the metal layer and through-hole requirement over the sense amplifiers is significantly reduced.

The invention also includes a hierarchical word line scheme. To facilitate the combination of the above-mentioned meshed system and the hierarchical word line scheme, the Noda hierarchical word line scheme should also be improved to provide a greater pitch of main word lines to subword lines. In the improved hierarchical word line system, an intersection area, created between the sense amplifier and the subdecoder, includes subdecoder drivers as well as sense amplifier drivers. This combination provides high speed word line selection and high speed sense amplifier operation at the same time.

Once the sense amplifier size is no longer determined by the metal usage, as provided by the above-mentioned meshed system, an improved layout technique for the sense amplifier circuits may be necessary to match

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the fine memory cell size. This improved layout technique includes an alternating T-shaped gate region for a bit line equalization circuit and an H-shaped moat region with a metal-to-polysilicon-to-metal change structure for a latch circuit.

A technical advantage achieved with the invention is the ability to fully utilize the low resistance design of a meshed power system without having to increase the size of the peripheral circuits, for example, sense amplifiers, that are limited in size by their metal layers.

A further technical advantage achieved with the invention is that both signal and power buses may freely run in both horizontal and vertical directions.

A further technical advantage achieved with the invention is that the design for through-holes located in the array area or on a step difference compensation area do not have to be made to the minimum design widths like the through-holes located in the peripheral area, and therefore the yield is improved.

A further technical advantage achieved with the invention is that the improved hierarchical word line structures are smaller and faster than conventional hierarchical word line structures.

Brief Description of the Drawings

Fig. 1 is a block diagram of a 256 Mbit DRAM embodying features of the present invention.

Fig. 2 is a block diagram of two subarrays and surrounding sense amplifiers and subdecoders of the DRAM of Fig. 1.

Fig. 3 is a block diagram of one subarray, two sense amplifiers, and a subdecoder, as shown in Fig. 2, and a meshed power and signal system running across the subarray.

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Fig. 4 is a schematic diagram of a meshed power and signal system over the subarray of Fig. 3.

Fig. 5a is a cross sectional view of a memory cell of the subarray of Fig. 3 with a through-hole connecting two metal layers used in the meshed power system of Fig. 4.

Fig. 5b is a detailed schematic of a memory cell of the subarray of Fig. 3.

Figs. 6a-6c are layout diagrams of expanded sections of the meshed system of Fig. 4.

Figs. 7a-b are schematic diagrams of circuits included in the intersection area, sense amplifier, subdecoder and memory array of Fig. 3.

Fig. 8 is a diagram of the subdecoder circuits of Figs 7.

Fig. 9a is a schematic diagram of a prior art subdecoder circuit showing the Noda hierarchical word line implementation.

Fig. 9b is a schematic diagram of one subdecoder circuit showing a hierarchical word line implementation.

Fig. 9c is a schematic diagram of a preferred subdecoder circuit showing a hierarchical word line implementation of the present invention.

Fig. 10a is a schematic diagram of the two sense amplifier circuits of Fig. 7a.

Fig. 10b is a layout diagram of the sense amplifier circuits of Fig. 10a.

Fig. 11a is a layout diagram of a circuit used in an equalizer section of a conventional sense amplifier.

Fig. 11b is a layout diagram of a circuit used in the equalizer section of the sense amplifier circuit of Fig. 7a, utilizing an alternate T-shaped gate region of the present invention.

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Fig. 12a is a layout diagram of a circuit used in the latch section of the sense amplifier circuit of Fig. 7a, utilizing the H-shaped moat region of Fig. 10b.

Fig. 12b is a simplified diagram of the H-shaped moat region of Fig. 12a.

Fig. 13a is a metal layout diagram of a section of a conventional sense amplifier.

Figs. 13b-c are metal layout diagrams of an improved section of the sense amplifier of Fig. 7a, implementing a noise decreasing method of the present invention.

Fig. 14a is a first cross sectional view of a sense amplifier using a triple well structure.

Fig. 14b is a second cross sectional view of the sense amplifier of Fig. 2, using a triple well structure.

Fig. 14c is a cross sectional view of the subdecoder of Fig. 2 using a triple well structure.

Fig. 15a is a block diagram showing four fuses used for the sense amplifiers of Fig. 2 and two additional sense amplifiers.

Fig. 15b is a schematic diagram showing four fuses used for the sense amplifiers of Fig. 2 and two additional sense amplifiers.

Detailed Description of the Invention

In Fig. 1 the reference numeral 10 refers to a memory device embodying features of the present invention. The device 10 is fabricated using a conventional CMOS technology, including first, second and third metal layers and a polysilicon layer. The device 10 also utilizes metal oxide semiconductor field effect transistors (MOSFETs), but other types of transistors may also be used, such as bipolar, and metal insulator semiconductors. Furthermore, while in a preferred embodiment of the

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invention, the device 10 is a 256 Mbit dynamic random access memory (DRAM), it should be understood that the present invention is not limited to use with a 256Mbit DRAM, but may be used in conjunction with other devices having arrays, including a programmable array logic, a 1Gbit DRAM and other memory devices.

The device 10 includes a set of array blocks of memory cells, such as an array block 12, a group of pads 14a - 14f, and a group of main address decoders 16a - 16*l*, wherein decoders 16b, 16e, 16h and 16k are row decoders and decoders 16a, 16c, 16d, 16f, 16g, 16i, 16j and 16*l* are column decoders. The array block 12 is selected by signals from the address pads 14a - 14d. It should be understood that while more address and signal pads exist, they may be represented by address pads 14a - 14d, which are decoded by main address decoders 16a - 16*l*. The main address decoders 16a - 16*l* represent a plurality of row and column decoders. The row decoders generate signals including main-word signals MWB and subdecoder control signals DXB, and the column decoders generate signals such as column select signals YS. These signals are controlled by different address signals from the address pads 14a - 14d, as discussed in greater detail below.

Array block 12, which is representative of the 16 Mbit array blocks, is further divided into 256 subarrays, two of which are shown in Fig. 2, and are respectively designated by reference numerals 18a and 18b. Each subarray consists of 128K of memory cells (arranged as 512 rows by 256 columns).

Power is supplied to the device 10 through power pads 14e and 14f. The pad 14e is the positive supply voltage (V_{DD}) power pad and is connected to an external power supply (not shown). The pad 14f is the negative supply voltage (V_{SS}) power pad and is connected to an external ground (also not shown).

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Referring to Fig. 2, the memory cells of the subarray 18a are selected by signals from two groups of address subdecoders 20a and 20b. Likewise, the memory cells of the subarray 18b are selected by signals from two groups of address subdecoders 20c and 20d. The memory cells of subarray 18a are read by two groups of sense amplifiers 22a and 22b. Likewise, the memory cells of subarray 18b are read by two groups of sense amplifiers 22b and 22c. The sense amplifiers 22a-22c intersect with the subdecoders 20a-20d, at intersection areas 24a-24f. In this way, intersection areas 24a-24f are created by the extension of sense amplifier areas 22a-22c and subdecoder areas 20a-20d.

Referring to Fig. 3, the pads 14e and 14f act as electrical ports to supply power to the entire device 10 through main VDD and VSS power buses 28 and 26, respectively. The main VDD and VSS power buses 28 and 26 supply power to the device 10 through a plurality of buses, located in different metal layers. The metal layers are layered onto a silicon substrate, in the order of: a first metal layer (M1), a second metal layer (M2), and a third metal layer (M3). Each of the metal layers M1, M2, M3 is electrically isolated from each other, but may be electrically interconnected at intersection points using through-holes. Each metal layer M1, M2, M3 also has associated therewith a thickness such that the thickness for M3 is greater than the thickness for M2, which is greater than the thickness for M1.

A first VDD bus 30, comprising a conductor constructed in the third metal layer M3, extends in a vertical path across the subarray 18a. A first VSS bus 32, also a conductor constructed in M3, extends in a vertical path across the memory subarray 18a, parallel with the bus 30. Similarly, a first signal bus 34 and a first column select YS bus 35, conductors constructed in M3, run vertically across the subarray 18a parallel with power buses 30 and

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32. A first subdecoder DXB bus 36, also a conductor constructed in M3, runs vertically across address subdecoder 20a, outside of the subarray 18a.

A second VDD bus 37a, a second VSS bus 37b and a second signal bus 37c, conductors constructed in M3, run vertically across the subdecoder 20a and the intersection areas 24a and 24b. The second VDD bus 37a and the second VSS bus 37b have a width that is less than a width of the first VDD bus 30 and the first VSS bus 32, respectively.

A third VDD bus 38 and a third VSS bus 40, along with a third signal bus 42 and a second DXB bus 44, are also conductors similar to those described above, except that they are constructed in the second metal layer M2, and extend in parallel, horizontal paths across the memory subarray 18a. The third VDD bus 38 electrically connects with the second VDD bus 37a within the subdecoder 20a at their intersection point 45 over the peripheral circuit area 20a and the first VDD bus 30 at their intersection point 46 within the memory subarray 18a. Likewise, the third VSS bus 40 electrically connects with the second VSS bus 37b at their intersection point 47 within the subdecoder 20a and the first VSS bus 32 at their intersection point 48 within the memory subarray 18a. Furthermore, the third signal bus 42 electrically connects with the second signal bus 37c at their intersection point 49 within the subdecoder 20a and the first signal bus 34 at their intersection point 50 within the memory subarray 18a. Finally, the second DXB bus 44 electrically connects with the first DXB bus 36 at their intersection point 52 in the subdecoder circuit 20a. Each of the intersection points is achieved using through-holes, as discussed in greater detail with reference to Figs. 5a-6c.

Associated with each bus is a line width, it being understood that a bus with a larger surface area (width and thickness) provides a lower resistance current path. The first VDD and VSS bus 30, 32 have a line width of 1.8 microns. The second VDD and VSS bus 37a, 37b have a line

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width of 0.7 microns. The third VDD and VSS bus 38, 40 have a line width of 1.8 microns. Likewise, the through-holes have associated therewith a diameter, it being understood that a through-hole with a larger surface area (diameter) provides a lower resistance current path. The through-holes located above the memory subarray 18a have a diameter of 0.6 microns, while the through-holes located above the subdecoder circuit 20a have a diameter of 0.8 microns.

VDD and VSS power is supplied through the external pads 14e and 14f the main power buses 28 and 26, respectively, as previously described in Fig. 3. The first VDD bus 30 is electrically connected to the main VDD power bus 28 thereby supplying VDD power to the first VDD bus, the second VDD bus 37a, and the third VDD bus 38. The first VSS bus 32 is electrically connected to the main VSS power bus 26 thereby supplying VSS power to the first VSS bus, the second VSS bus 37b, and the third VSS bus 40. In this manner, a VDD mesh 54 is created by the VDD buses 30, 37a and 38 and a VSS mesh 56 is created by the VSS buses 32, 37b and 40. As a result, each of the foregoing meshes have power buses running both vertically and horizontally across the subarray 18a, the subdecoder 20a and the intersection areas 24a-24b. Furthermore, the VDD and VSS meshes 54 and 56 significantly reduce the total power bus resistance from the power pads 14e and 14f to the subdecoder 20a, the intersection areas 24a-24b and other circuits, even when the widths of the VDD and VSS buses 37a and 37b are narrow.

A first peripheral circuit (not shown) drives electrical signals to the first signal bus 34 and the column decoder 16a (Fig. 1) drives electrical signals to the YS bus 35, which is used in sense amplifiers 22a and 22b. Likewise, main address decoder 16b (Fig. 1) drives electrical signals to the second DXB bus 44, in a conventional manner. The first signal bus 34 electrically connects with the second signal bus 37c and the third signal bus

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42 thereby creating a signal mesh 58 across the subarray 18a and the subdecoder 20a. Likewise, the first DXB bus 36 electrically connects with the second DXB bus 44 thereby creating a subdecoder mesh 60 across the subdecoder 20a. In this manner, the signal and subdecoder meshes 58 and 60 are able to connect the sense amplifiers 22a-22b, the subdecoder 20a, and the intersection areas 24a-24b in many different combinations. Although not shown, there are many additional buses constructed in M2 and extending horizontally across the sense amplifier circuit areas 22a and 22b. Some of these buses are connected to other signal buses, such as the YS bus 35.

Referring to Fig. 4, the VDD, VSS, signal and subdecoder meshes 54, 56, 58 and 60 actually represent many vertical and horizontal lines for each mesh, thereby providing more buses for the surrounding circuits, and decreasing the resistance of each mesh. For example, the subarray 18a has multiple VDD buses 38a-38d running in M2 and multiple VDD buses 30a-30d running in M3, all tied to the main VDD bus 28 (Fig. 3), thereby decreasing the overall resistance of the VDD mesh 54. Likewise, the subarray 18a has multiple VSS buses 40a-40d running in M2 and multiple VSS buses 32a-32d running in M3, all tied to the main VSS bus 26 (Fig. 3), thereby decreasing the overall resistance of the VSS mesh 56.

In addition to the VDD, VSS, signal and subdecoder meshes 54, 56, 58 and 60, other buses run across the subarray 18a. These other buses include multiple column factor (CF) buses 61a-61d running vertically in M3, for inputs to the column decoders 16a, 16c, 16d, 16f, 16g, 16i, 16j and 16*l* (Fig. 2), and multiple subdecoder buses (DXB1, DXB3, DXB5, DXB7) 44a-44d running horizontally in M2, for connection to the subdecoder circuits 20a and 20b (Fig. 2) and to the first DXB bus 36. Furthermore, as shown in Fig. 4, power buses 30a-30d, 32a-32d, 38a-38d, 40a-40d are located near an outer edge of the subarray 18a than the signal buses 61a-61d, 44a-44d. As

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a result, resistance of the power buses is reduced, while the resistance for the signal buses, all grouped toward the interior edge of the subarray 18a, are relatively consistent with each other, thereby making signal propagation through the signal buses relatively consistent.

Referring to Fig. 5a, the electrical connections between the buses shown in Fig. 4 are made at intersection points located above memory cells. An intersection point 48a denotes where the VSS bus 32b crosses the VSS bus 40b. An electrical connection is made between the VSS bus 32b and the VSS bus 40b using a through-hole 62, located above a memory cell circuit 64.

Referring to Figs. 5a-5b, the memory cell circuit 64 of the subarray 18a comprises a conventional, one capacitor and one transistor type DRAM cell. For example, a capacitor 65 is formed between a plate 67 and a storage node 68. Likewise, a transistor 69 is formed with the source and drain connected to the storage node 68 and a bit line (BL1) bus 70, respectively, and the gate connected to a first subword line (SW) bus 72a, having a width 74. To avoid any coupling noise caused by the power and signal buses, the cell structure of the preferred embodiment is a capacitor on bit line (COB) structure. This structure facilitates the sensitive nature of the BL1 bus 70 and enables operation without any detrimental effect by noise from the power and signal meshes 54, 56 and 58 located over the cell, due to the shielding affect of the plate 64.

Although the intersection point 48a appears to be located directly over the memory cell circuit 64, this is not required, and is only for the benefit of explanation. Furthermore, the through-hole 62 and VSS buses 32b and 40b are not necessary for memory cell 64 and not all of the power and signal buses will be connected to other buses.

Referring to Figs. 4 and 6a, a first section 76 gives an expanded view of the subarray 18a, showing more signal lines located between the buses shown in Fig. 4. Section 76 has several signal and power buses of various

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widths running both vertically and horizontally across it. These buses include YS buses 35a-35d, having a width 80, the CF bus 61a, having a width 82, and the VSS bus 32b, having a width 84, running vertically in M3. Likewise, MWB buses 86a-86d, having a width 88, the DXB1 bus 44a, having a width 90 and the VSS bus 40b, having a width 92, run horizontally in M2. The signal buses YS 35a-35d, CF 61a, MWB 86 and DXB1 44a run directly to their corresponding circuits, and therefore do not require a through-hole on the subarray 18a to change directions. Only the VSS buses 32b and 40b have a through-hole 62 to electrically connect them. With this arrangement, the width of each bus, 80, 82, 84, 88, 90 and 92, is optimized for speed and power resistance effect. For example the widths 84 and 92 of the VSS buses 32b and 40b, the width 82 of the CF bus 61a, and the width 90 of the DXB1 bus 44a are wider than the widths 80 and 88 for high speed and low power resistance, and to accommodate the through-hole 62. Meanwhile, the width 80 of the YS buses 35 and the width 88 of the MWB buses 86, are made narrower than the widths 82, 84, 90, 92 to conserve metal space.

Likewise, referring to Figs. 6b and 6c, sections 94 and 96 are shown, having two and no through-holes, respectively. As a result, two YS buses and one CF bus (or two YS buses and one power bus) are created with every four sense amplifier circuits, while still meeting acceptable M3 width and space requirements. Likewise, two MWB buses and one DXB bus (or two MWB buses and one power bus) are placed with every sixteen sub-word-line SW buses, while still meeting acceptable M2 width and space requirements. In addition, the widths of all the power and signal buses may be optimized to accommodate the multiple buses used by each mesh for reducing effective resistance and for achieving high speed, keeping the essential advantage of high yield by having the relaxed metal pitch of hierarchical word-line configuration.

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Referring again to Fig. 3, in addition to the power and signal meshes 54, 56, and 58 being constructed over the subarray 18a, they are partially constructed over the subdecoder 20a, along with the subdecoder mesh 60. Other circuits are modified to accommodate the metal space needed by the power and signal meshes 54, 56, 58 and 60,. The modified circuits are included in the sense amplifiers, the subdecoders and the intersection areas, as described below.

Figs. 7a and 7b illustrate the subarray 18a comprising 32 representative memory cells including the memory cell 64 of Figs. 5a-b. Furthermore, the subarray 18a is shown in relation to the intersection area 24a, the subdecoder 20a, and the sense amplifier 22a of Fig. 2.

In the preferred embodiment, the sense amplifier 22a includes 128 sense amplifier circuits, such as sense amplifier circuits 98a and 98b. Both of the sense amplifier circuits 98a-98b are connected to a sense amplifier driver 100a, which is located in the intersection area 24a. The sense amplifier circuit 98a is connected to a column of memory cells 102a, through the BL1 bus 70 (Fig. 5a) and a bit line (BL1B) bus 104a, which are both constructed in M1, and run vertically across the array 18a. Likewise, the sense amplifier circuit 98b is connected to a column of memory cells 102b, through a bit line (BL2) bus 104b and a bit line (BL2B) bus 104c, which are also constructed in M1, and run vertically across the array 18a. Sense amplifier circuits 98a-98b are discussed in greater detail with reference to Figs. 10a-10b, below.

In addition to the sense amplifier driver 100a, the intersection area 24a includes a plurality of circuits (excluding sense amplifier driver 100a and subdecoder drivers 110a-110d) which are referenced generally by the numeral 100b. These circuits 100a-100b are designed to employ the advantages of the low resistance of the VDD, VSS and signal meshes 54, 56 and 58, as supplied by the buses 37a-37c.

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The subdecoder 20a includes 256 subdecoder circuits, represented generally be subdecoder circuit 106a-106d. The subdecoder circuit 106a illustrates a hierarchical word line structure utilized in each of the remaining subdecoder circuits. The subdecoder circuit 106a is connected to the DXB7 bus 44d and the MWB bus 86a, which is routed to the four subdecoder circuits 106a-106d through a connector bus 108, constructed in M1. The subdecoder circuit 106a is also connected to a first subdecoder driver 110a, located in the intersection area 24a, along with the sense amplifier driver 100. Likewise subdecoder circuits 106b-106d are connected to subdecoder drivers 110b-110d, located in the intersection areas. The subdecoder 20a is discussed with more detail below.

Referring to Fig. 8, two subdecoder drivers 110a-110d are located in intersection area 24a, while the other two subdecoder drivers 110b-110c are located in the intersection area 24b. The subdecoder driver 110a comprises an inverter, which converts the DXB7 bus 44d, to an inverted subdecoder (DX7) bus 114d. Likewise, the subdecoder drivers 110b-d convert the DXB1 44a, DXB3 44b and DXB5 44c to inverted subdecoder buses DX1 114a, DX3 114b and DX5 114c. In the preferred embodiment, each of the subdecoder drivers 110a-110d drive 64 subdecoder circuits, thereby driving all 256 of the subdecoder 20a. Being located in the intersection areas 24a-24b, the subdecoder drivers 110a-110d are made of significant size, and are supplied an internally generated boosted voltage (VPP) so that the buses DX1 114a, DX3 114b, DX5 114c and DX7 114d can be driven to VPP.

The subdecoder circuits 106a et seq. employ a hierarchical word line structure. As discussed earlier, the subdecoder circuits formed in the subdecoder area 20a and 20b are used to select certain memory cells in the subarray 18a. This is accomplished by utilizing a plurality of subword lines, such as the line 72a, constructed in the polysilicon (FG) layer (Fig. 5a). The MWB bus 86a drives four subdecoder circuits 106a-106d of subdecoder are

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20a, which each drive a SW bus 72a-72d, extending into the subarray 18a. Likewise, the MWB bus 86a drives four additional subdecoder circuits 106e-106h of subdecoder area 20b, which each drive a SW bus 72e-72h, extending into the subarray 18a.

Referring to Figs. 9a-9b, a conventional subdecoder circuit 116 and an alternative subdecoder circuit 118 implement a hierarchical word line structure. The structures are hierarchical due to the placement of main word line buses, constructed in M2, over a subword line buses, constructed in FG. However, the subdecoder circuits 116, 118 do not facilitate the meshed system of the present invention.

Referring to Fig. 9a, the conventional subdecoder circuit 116, as used in the Noda hierarchical word line structure scheme, consists of three n-type metal oxide semiconductor (NMOS) transistors and produces an SW output. However, the subdecoder circuit 116 requires a non-inverted word line (MW) bus, which must also run across the array (not shown) along with a MWB bus. This effectively doubles the number of main word lines running in M2 across the array. As a result, two main word lines are used to drive eight subword lines, thereby creating a pitch of 4 subword lines to every main word line. This pitch, however, does not allow the extra metal space needed for the meshed system of the present invention.

Referring to Fig. 9b, the subdecoder circuit 118 consists of two NMOS transistors and two p-type metal oxide semiconductor (PMOS) transistors. The subdecoder driver does not require a non-inverted word line bus (MW) as in Fig. 9a. As a result, one main word line is used to drive eight subword lines, thereby creating a pitch of 8 subword lines to every main word line. But, since the subdecoder circuit consists of four transistors, it thereby consumes a lot of space, and to speed the circuit up, some of the transistors must be made very large.

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Referring to Fig. 9c, the subdecoder circuit 106a of the preferred embodiment comprises the advantages of the above two subdecoder drivers. The subdecoder circuit 106a uses the MWB bus 86a, the DXB7 bus 44d, and the DX7 bus 114d to produce the subword line SW bus 72a, thereby allowing the subdecoder circuit 106a to be constructed with only three transistors 120a-120c. Since the DX7 bus 114d runs only in the subdecoder 20a, and does not have to run horizontally across the array, the main word line pitch across the subarray 18a remains at eight subword lines for every main word line. As a result, there is sufficient metal space for the power, signal and subdecoder meshes 54, 56, 58 and 60, and the DXB bus 44 (Fig. 3) of the present invention.

In operation, the signals on the MWB bus 86a and DXB7 bus 44d, designated as MWB and DXB7, are negative logic signals, i.e. they are high in the standby mode, low in an enable mode. When the signals MWB and DXB7 are both low, an output signal on the subword line SW bus 72a is driven to a selective high level. When only one of the signals MWB or DXB7 is high, the output signal on the subword line SW bus 72a is driven to a non-selective low level. In the standby or precharge mode, i.e., when all of the MWB and DXB signals are high, all subword lines SW are set to low.

An advantage of the subdecoder circuit 106a is that a subthreshold current in the row decoders and DXB drivers is primarily determined by NMOS transistors 120a, 120b. As a result, a low standby current is achieved during standby or precharge mode. This is because a gate with for the NMOS tranisistors 120a, 120b can be narrower than that of PMOS transistors, and NMOS transistor cutoff-transition characteristics are sharper than that of PMOS transistors.

Other advantages of the subdecoder circuit 106a are that the subdecoder circuit 106a provides extra metal space for the power, signal and

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subdecoder meshes 54, 56, 58 and 60, and the subdecoder circuit 106a improves in speed performance. The speed of the subdecoder circuit 106a is directly proportional to the ability of the DX7 bus 114d to transition from low to high. Since the DX7 bus 114a is driven by the subdecoder driver 110a, and since the subdecoder driver is located in the non-crowded intersection area 24a, it can be made of sufficient size. Furthermore, the DX7 bus 114a is constructed in M3, which has the lowest resistance of the three metal layers. Thus, the DX7 bus 114a produces a sharp rising wave form, thereby achieving high speed activation of the SW bus 72a. In the preferred embodiment, a gate width (not shown) of the NMOS transistor 120b of is narrower than that of a gate width (also not shown) of the NMOS transistor 120a, thereby improving speed and layout area optimization. For example, in the preferred embodiment, the gate widths of transistors 120a and 102b are 2.2 microns and 1 micron, respectively. The narrow gate width of transistor 120b contributes to smaller load capacitance and faster fall times for signals on the DXB bus 44d. As a result, the DX bus 114d achieves faster rise times. In addition, the gate width of 120a is set to the sufficient value for falling speed of the subword line SW.

Referring to Fig. 10a, the sense amplifier circuit 98a comprises a latch section 122a and an equalizer section 124a. The latch section 122a comprises two NMOS transistors 126a-126b, connected between the bit line buses 70 and 104a and a first latch bus 128. The latch section 122a also comprises two PMOS transistors 130a-130b connected between the bit line buses 70 and 104a and a second latch bus 132. All four transistors 126a, 126b, 130a, 130b are cross-coupled in a conventional latching manner for storing signals from the bit line buses 70 and 104a.

The equalizer section 124a includes three NMOS transistors 134a-134c for equalizing the BL1 bus 70 and the BL1B bus 104a during the

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standby or pre-charge modes. The three transistors 134a-134c are controlled by an equalization bus 136.

In a similar manner, the sense amplifier circuit 98b comprises a latch section 122b and an equalizer section 124b connected to the bit line buses 104b-104c. The latch section 122b and the equalizer section 124b are also connected to the two latch buses 128, 132 and the equalization bus 136, respectively.

Referring to Fig. 10b, a further reduction in the size of the sense amplifier 22a is achieved by other layout improvements. The equalizer sections 124a and 124b are constructed in shapes of alternating "T's" as discussed in greater detail below with reference to Fig. 11a. The latch sections 122a and 122b are constructed utilizing "H" shaped moat regions, as discussed in greater detail below with reference to Fig. 12a-b.

Referring to Figs. 11a-11b, to reduce the size constraints of the equalizer section 124a caused by the transistors 134a-134c, a T-shaped gate region 138a (Fig. 11a) is utilized. The equalizer signal bus 136 creates a gate for each of the transistors 134a-134c. In a similar manner, the equalizer section 124b utilizes an inverted T-shaped gate region 138b. As a result, the gate regions 138a, 138b can be compacted together, while still maintaining a required moat isolation distance 137 between the gate regions 138a, 138b. In so doing, a width 140 of the two gate regions is smaller than a conventional width 142 of two square gate regions 144a and 144b, as shown in Fig. 11b, and a small sense amplfier circuit 22a corresponds to the small memory cell circuit 64 (Fig. 5a).

Referring to Fig. 12a, the sense amplifier 22a also comprises an H-shaped moat 146. The BL1 bus 70, constructed in M1, must cross the BL1B bus 104a, also constructed in M1, at the H-shaped moat 146 without electrically intersecting. Furthermore, the BL1 bus 70 must drive a transistor gate 148a and the BL1B bus 104a must drive a transistor gate

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148b. At a crossing point 150, the BL1B bus 104a is connected to the transistor gate 148b, constructed in FG, which runs under the metal layers. The gate 148b not only serves to allow the BL1B bus 104a to cross the BL1 bus 70, but it is the gate for the transistor 130b. After crossing the BL1 bus 70, the gate 148b is reconnected to a connecting bus 152, also constructed in M1, thereby electrically connecting the BL1B bus 104a to the connecting bus 152. Similarly, the BL2 bus 104b and the BL2B 104c bus also cross in the H-shaped moat 146.

Referring to Fig. 12b, these connections create an M1 to FG to M1 change and construct the two PMOS transistors 130a-130b. Not only does this change provide a size reduction, it does so without using an additional metal layer.

Furthermore, the H-shaped moat 146 solves another problem associated with the meshed system, that is, noise on the bit line buses 70 and 104a-104c. Noise at the sense amplifiers 22a-22c is often caused by signal buses constructed in M3 overlapping the bit line buses 70 and 104a-c constructed in M1. Since the bit line buses 70 and 104a do a crossing pattern, any noise or capacitive coupling induced from signal buses constructed in M3, such as the CF bus or the YS bus, will be the same for both the BL1 bus 70 and the BL1B bus 104a, thereby effectively canceling the effect of noise. Likewise, any noise will be the same for the BL2 bus 104b and the BL2B bus 104c.

Referring to Fig. 13a, addition noise protection from signal buses constructed in M3 overlapping the bit line buses 70 and 104a-c constructed in M1 can be reduced through M2 shielding. For example, in conventional prior art designs having first and second buses 154a-154b constructed in M1 and running in a vertical direction, and having a third bus 154c constructed in M3 which also running in a vertical direction, noise is aggravated. Noise is induced from the third bus 154c to the first and second buses 154a and

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154b, since they overlap and run in the same direction, allowing the noise to be strengthened by the large area of overlap. This conventional design can be a problem, especially when the buses 154a, 154b are particularly sensitive to noise, such as the bit line buses 70 and 104a of the present invention. Furthermore, in the conventional design, a group of other buses 156a-156d constructed in M2 and running in a horizontal direction have little to no shielding effect, as shown.

Referring to Figs. 13b-13c, the preferred embodiment reduces the noise between buses running in the same direction by improving the shielding effect of the M2 buses. In the preferred embodiment, the BL1 bus 70 and the BL1B bus 104a are constructed in M1 and run in the vertical direction. Furthermore, the CF bus 61a is constructed in M3 and runs in the vertical direction, just above the two bit line buses 70 and 104a. Located between the CF bus 61a and the bit line buses 70 and 104a are four buses 158a-158d constructed in M2 and running in the horizontal directions.

Referring to Fig. 13b, one technique for reducing noise is used in a situation where the M2 buses 158a and 158d are noisy, active lines, such as parts of the sense amplifiers, and the M2 buses 158b-c are inactive, quiet buses, such as a power supply bus, a first technique is used. Instead of having some of the M2 buses 158a-158d only extending across one of the bit line buses 70 and 104a, as shown in Fig. 13a, the M2 buses 158b-158c now extend over both bit line buses. In this manner, the M2 buses 158a-158d provide more of a shielding affect from any noise from the CF bus 61a.

Referring to Fig. 13c, in a situation where two of the M2 buses 158a and 158d are inactive, quiet buses, such as a power supply bus, and the other two of the M2 buses 158b,158c are active, noisy buses, a second technique is used. In this case, the bit line buses 70 and 104a are better shielded from the noise of the CF bus 61a by the quiet M2 buses 158a,

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158d. Therefore, the quiet M2 buses 158a, 158d are drawn as large as possible, thereby maximizing their shielding affect.

Referring to Fig. 14a, the well structure of the sense amplifier can also be size determinative, especially in a situation like the preferred invention where power and signal meshes are utilized. In a first design, a triple well structure 160 comprising a p well (PW) 162a, a deep well (DW) 164a and a p-substrate (P-Sub) 166 is used for noise protection from a sense amplifier circuit 170 to a subarray 168a. Likewise, the triple well structure 160 comprises a p well (PW) 162b, a deep n-type well (DW) 164b and the P-Sub 166 for noise protection from a sense amplifier circuit 170 to a subarray 168b. Although the wells 162a, 162b, 164a, 164b and substrate 166 may have various bias arrangements, one such arrangement provides:

Well	Bias Name	Bias Voltage
PW over DW	VBBA 167a	-1V
NW over DW	VPP 167b	4.0V
DW	VPP 167b	4.0V
P-Sub	VBB 167c	0V
PW (not over DW)	VBB 167c	0V
NW (not over DW)	VDD 167d	3.3V

Table 1

It is noted that well biasing is well known in the art, and any descriptions of bias voltage are merely illustrative, and should not be limited to such in any manner.

The subarrays 168a and 168b are isolated from the noisy effects of the sense amplifiers 170 by two isolation n wells (NWs) 172a and 172b, respectively. The NWs 172a, 172b create separation transistors for sharing one sense amplifier between memory cell arrays located on either side. A

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negative bias voltage that is suitable for device isolation is supplied to the P-wells 162s and 162b, where the above described separation transistors and the memory cell transistors are both located. The NWs 172a, 172b are biased to VPP 167b for electrical isolation. Furthermore, the NW's 172a, 172b are located above the DWs 164a, 164b, respectively, and thereby bias the Dws to VPP. The sense amplifier circuit 170 has an additional NW 174, which is biased to VDD 167d to provide faster operation of a p-type transistor 176. The advantage for DWs 164a, 164b being biased to VPP is that the subdecoders are CMOS circuits operating at the VPP voltage level (Figs. 7a, 7b, 14c). On the other hand, because PMOS transistors of the sense amplifier circuit 170 operate at or below the VDD voltage level, the VDD voltage level is suitable as a bias voltage for the NW 174, instead of the VPP voltage level. The sense amplifier 170 also has two PWs 178a, 178b, biased to VBB 167c through the P-sub 166. The PW 178a supports a transistor 180a and the PW 178b supports transistors 180b, 180c.

Referring to Fig. 14b, the preferred embodiment is able to shrink the well structure of the sense amplifier 24b, as compared to Fig. 14a. The preferred embodiment utilizes a triple well structure 182 comprising a PW 184a, a DW 186a, and a P-Sub 188, for subarray 18a, and a PW 184b, a DW 186b, and the P-Sub 188, for subarray 18b. The subarrays 18a-18b are thereby protected from the sense amplifier circuit 22b. The triple well structure 182 also uses well-biasing similar to the illustrative biases described in Table 1. It is noted, however, that well biasing is well known in the art, and any descriptions of bias voltage are merely illustrative, and should not be limited to such in any manner.

The subarrays 18a-18b are isolated from the noisy effects of the sense amplifiers 24b by two isolation NWs 190a, 190b, respectively. The isolation NWs 190a, 190b are biased to VPP 167b for isolation. Furthermore, the isolation NWs 190a, 190b are located above the DWs 186a-186b,

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respectively, and thereby bias the DWs. The preferred embodiment differs from the conventional system of Fig. 14a in that the isolation NW 190a also supports the transistor 130d, which corresponds with the transistor 176 of Fig. 14a. As a result, the transistor 130d will operate slower than the transistor 176 of Fig. 14a. However, the speed of the transistor 130d is not critical to the overall timing of the sense amplifier circuit 90a. Therefore, although the PMOS transistor 130d is using a VPP biased well, there is no overall speed degradation.

There is a size advantage, however, to the isolation NW 190a over the conventional technique described in Fig. 14a. Instead of having the NW 172a for the sole purpose of isolation, and the second NW 174 for the transistor 176 (Fig. 14a), the two are combined in the NW 190a of the preferred embodiment, thereby shrinking the space of the sense amplifier 24b. Furthermore, a single PW 192 can be used to support the transistors 134a-134c.

Referring to Fig. 14c, a triple well structure 193 is implemented for the subdecoder 20a. The P-Sub 188 and the DW 186a extend throughout the subarray 18a (Fig. 14b), across the subdecoder 20a, and into a subarray 196. The PW 184a is separated from a PW 198 by an NW 200, which is biased to VPP 167b for isolation. By biasing the NW 200 at VPP 167b, the SW bus 72a can operate at VPP.

Referring to Figs. 15a and 15b, the sense amplifier 22a includes four fuses 202a-202d used for a column redundancy scheme. The two fuses 202b and 202d are used to disable sense amplifier circuits 98a-98b, and the two fuses 202a and 202c are used to disable sense amplifier circuits 204a-204b. Column redundancy is well known to those skilled in the art; however, conventional designs result in a dramatic area penalty in the sense amplifier design due to the fuse placement. Accordingly, in the preferred embodiment, the fuses 202a-202d are lined in parallel with the bit line

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buses 70 and 104a, even for the fuses corresponding to sense amplifiers located in a different area. In this way, the vertical running CF bus 61a and the YS buses 35c-35d need to be offset for only one group of fuses, thereby providing the maximum space for the power and signal meshes 54, 56, 58 and 60.

Although the illustrative embodiment of the present invention has been shown and described, a latitude of modification, change and substitution is intended in the foregoing disclosure, and in certain instances, some features of the invention will be employed without a corresponding use of other features. For example, the horizontal and vertical directions were included to make the preferred embodiment simpler to describe, but are not intended to limit the present invention. Accordingly, it is appropriate that the appended claims be construed broadly and in a manner consistent with the scope of the invention.

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WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:

a semiconductor substrate having a main surface;

a memory array portion in said main surface, in which a plurality of memory cells are arranged in row direction and in column direction;

bit lines each extending in said column direction and each of said bit lines connected to said memory cells;

word lines each extending in said row direction and each of said word lines connected to said memory cells;

a first peripheral circuit portion having a plurality of MOSFETs and said first peripheral circuit arranged adjacent to said memory array portion;

an external terminal formed on said main surface of said semiconductor substrate, and a predetermined voltage is supplied to said external terminal from outside of said semiconductor memory device;

a plurality of first voltage supply lines each extending in said column direction and formed over said bit lines and word lines;

a plurality of second voltage supply lines each extending in said row direction and formed over said bit lines and word lines, and said second voltage supply lines formed by a conductive layer which is different from that of said first voltage lines,

wherein said first and second voltage supply lines are connected each other at the intersection of said first and second voltage supply lines,

wherein one of said first and second voltage supply lines is connected to said external terminal, and

wherein said predetermined voltage is supplied to said MOSFETs in said first peripheral circuit portion from said external terminal via said first and second voltage supply lines.

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2. A semiconductor memory device according to claim 1, wherein said first voltage supply lines are comprised of a first conductive layer and said second voltage supply lines are comprised of a second conductive layer, and said first conductive layer is over said second conductive layer and said first conductive layer has a predetermined thickness which is thicker than that of said second conductive layer.

3. A semiconductor memory device according to claim 1, further comprising:

a second peripheral circuit portion having a plurality of MOSFETs, said second peripheral circuit portion being adjacent to said memory array region in said row direction and being adjacent to said first peripheral circuit portion in said column direction; and

a third voltage supply line formed in said first peripheral circuit portion and extending in parallel with said bit lines and into said second peripheral circuit portion,

wherein said second voltage supply lines extend into said second peripheral circuit portion and connected to said third voltage supply line at the intersections between said second voltage supply lines and third voltage supply line.

4. A semiconductor memory device according to claim 3, wherein said third voltage supply line is comprised of said first conductive layer and said third voltage supply line is connected to said MOSFETs in said first peripheral circuit portion.

5. A semiconductor memory device according to claim 4, wherein said first voltage supply lines each has a predetermined width which is larger than that of said third voltage supply line.

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6. A semiconductor memory device according to claim 5, further comprising:

an insulating layer formed between said first conductive layer and said second conductive layer, said insulating layer has a first through hole through which said first and second voltage supply lines are connected and a second through hole through which said second and third voltage supply lines are connected, wherein said first through hole has a predetermined diameter which is larger than that of said second through hole.

7. A semiconductor memory device according to claim 6, wherein said memory cell is comprised of a MOSFET and a capacitor element connected in series, and said capacitor element is formed over said MOSFET.

8. A semiconductor memory device according to claim 4, further comprising:

a sense amplifier circuit portion being adjacent to said memory array portion in said column direction and being adjacent to said first peripheral circuit portion in said row direction, wherein said MOSFETs in said first peripheral circuit portion constitute sense amplifier driver circuit.

9. A semiconductor memory device according to claim 8, wherein a plurality of signal wirings extending in row direction in said sense amplifier circuit portion, said signal wirings are comprised of said second conductive layer.

10. A semiconductor memory device according to claim 4, wherein sub-decoder circuit is formed in said second peripheral circuit portion, and

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said sub-decoder circuit has two input terminals and an output terminal, a main word line and sub-decoder control line are connected to said input terminals and said word line is connected to said output terminal.

11. A semiconductor memory device according to claim 10, wherein said main word line and said sub-decoder control signal are comprised of said second conductive layer.

12. A semiconductor memory device according to claim 11, wherein said second voltage supply line has a predetermined width which is larger than that of said main word line.

13. A semiconductor memory device according to claim 11, further comprising:

a fourth voltage supply line formed in said memory array portion and comprised of said second conductive layer, and said subdecoder control line extending in said row direction arranged in the center of said memory array portion and said fourth voltage supply line extending in said row direction, and said second and fourth voltage supply lines are arranged at the both sides of said sub-decoder control line.

14. A semiconductor memory device according to claim 13, wherein said fourth voltage supply line is connected to said first voltage supply line at the intersection of said fourth and first voltage supply lines.

15. A semiconductor memory device according to claim 1, further comprising:

row select lines formed in said memory array portion and comprised of said first conductive layer;

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row decoder circuit selecting a predetermined row select line into row select lines, wherein said first voltage supply line has a predetermined width which is larger than that of said row select line.

16. A semiconductor memory device according to claim 15, further comprising:

signal lines which is different from said row select line, extending in said column direction in said memory array portion, said signal lines comprised of said first conductive layer.

17. A semiconductor memory device according to claim 16, further comprising:

a fifth voltage supply line comprised of said first conductive layer and being extending in said column direction.

18. A semiconductor memory device according to claim 17, wherein said signal lines extend at the center of said memory array portion in said column direction, and said first and fifth voltage supply lines are arranged at the both sides of said signal lines.

19. A semiconductor memory device, comprising:

a semiconductor substrate;

a sub-array portion including a plurality of memory cells each being arranged at the intersection of bit line extending in a column direction and word line extending in a row direction;

a first peripheral circuit portion being adjacent to said sub-array in said row direction;

a second peripheral circuit portion being adjacent to said sub-array in said row direction;

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a third peripheral circuit portion at the intersection of said first and second peripheral circuit portions;

a plurality of first voltage supply lines each extending in said column direction and formed over said bit lines and word lines;

a plurality of second voltage supply lines each extending in said row direction and formed over said bit lines and word lines, and said second voltage supply lines formed by a conductive layer which is different from that of said first voltage lines, and said second voltage lines formed over said sub-array portion and said second peripheral circuit portion;

a third voltage supply line comprised of said first conductive layer and extending over said second and third peripheral circuit portion,

wherein said first and second voltage supply lines are connected each other at the intersection of said first and second voltage supply lines over said sub-array portion,

wherein said second and third voltage supply lines are connected each other at the intersection of said second and third voltage supply lines over said second peripheral circuit portion, and

wherein said first and second voltage supply lines each has predetermined width which is larger than that of said third voltage supply line.

20. A semiconductor memory device according to claim 19, wherein a plurality of MOSFETs are arranged in said third peripheral circuit portion, and said MOSFETs are connected to said third voltage supply line.

21. A semiconductor memory device according to claim 20, further comprising:

a plurality of signal wiring lines extending in said row direction and comprised of said second conductive layer.

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22. A semiconductor memory device according to claim 21, further comprising:

an insulating film formed between said first and second conductive layers, said insulating layer has a first through hole through which said first and second voltage supply lines are connected and a second through hole through which said second and third voltage supply lines are connected, wherein said first through hole has a predetermined diameter which is larger than that of said second through hole.

23. A semiconductor memory device according to claim 6, wherein said memory cell is comprised of a MOSFET and a capacitor element connected in series, and said capacitor element is formed over said MOSFET.

24. A semiconductor memory device according to claim 21, wherein said first conductive layer is over said second conductive layer and said first conductive layer has a predetermined thickness which is thicker than that of said second conductive layer.

25. A semiconductor memory device according to claim 19, wherein sub-decoder circuit is formed n said second peripheral circuit portion, and said sub-decoder circuit has two input terminals and an output terminal, a main word line and sub-decoder control line are connected to said input terminals and said word line is connected to said output terminal.

26. A semiconductor memory device according to claim 25, wherein said main word line and said sub-decoder control signal are comprised of

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said second conductive layer, and said second voltage supply line has a predetermined width which is larger than that of said main word line.

27. A semiconductor memory device according to claim 26, wherein said sub-decoder control line extending in said row direction arranged in the center of said sub-array portion and said second voltage supply lines are arranged at the both sides of said of said sub-decoder control line.

28. A semiconductor memory device including a plurality of memory cells formed on a semiconductor substrate, complementary first and second bit lines to which said memory cells are connected, a first and second MOSFET connected in series between said first and second bit lines and third MOSFET connected between said first and second bit lines, comprising:

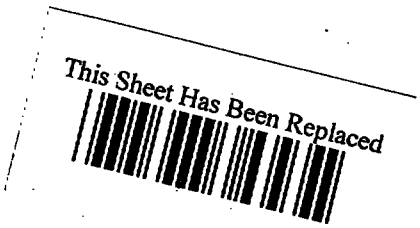
an active region formed on the main surface of said semiconductor substrate, in order to form said first, second and third MOSFETs;

a first, a second and a third semiconductor region formed in said active region;

an insulating film formed between said first, second and third semiconductor region and said first and second bit lines, said insulating film having a first through hole for connecting said first semiconductor region to said first bit line, a second through hole for connecting said second semiconductor region to said second bit line and a third through hole formed over said third semiconductor region; and

a gate electrode arranged between said first and second semiconductor regions, between second and third semiconductor regions and between said third and first semiconductor regions,

wherein said first, second and third through holes constitute a triangle, and the triangle corresponding complementary bit lines and the



triangle corresponding adjacent complementary bit lines are mirror symmetrical relationship.

29. A semiconductor memory device according to claim 28, wherein said active region has T-shape configuration.

30. A semiconductor memory device according to claim 29, wherein said gate electrode has T-shape configuration.

31. A semiconductor memory device according to claim 30, wherein a predetermined fixed voltage is supplied to said third semiconductor region.

32. A semiconductor memory device, comprising:

a first MOSFET and a second MOSFET which constitute a sense amplifier circuit, said first and second MOSFETs each having a first semiconductor region and a second semiconductor region as source and drain;

a first memory array portion and a second memory array portion at both sides of said first and second MOSFETs;

complementary a first and a second bit lines extending in said first memory array portion, and complementary a third and a fourth bit lines extending in said second memory array portion,

wherein said first, second, third and fourth bit lines are comprised of a conductive layer,

wherein said first bit line is connected to said first semiconductor region, and is connected to said third bit line via said gate electrode of said second MOSFET,

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wherein said second bit line is connected to said gate electrode of said first MOSFET and said first semiconductor region of said second MOSFET, and said second bit line is integral with said fourth bit line.

33. A semiconductor memory device comprising:

a memory array having a main word line, first and second subword lines corresponding to said main word line, a plurality of data lines and a plurality of memory cells;

a first subdecoder having an output terminal coupled to said first subword line and a first input terminal coupled to said main word line;

a second subdecoder having an output terminal coupled to said second subword line and a first input terminal coupled to said main word line;

a first driver, coupled to a second input terminal of said first subdecoder, outputting selection level voltage to be supplied to said first subword line; and

a second driver, coupled to a second input terminal of said second subdecoder, outputting selection level voltage to be supplied to said second subword line,

wherein said memory array is formed in a first area,

wherein said first and second subdecoders are formed in a second area which is adjacent to said first area, and

wherein said first and second drivers are formed in a third area which is adjacent to said second area.

34. A semiconductor memory device according to claim 33, further comprising:

a plurality of sense amplifiers coupled to said plurality of data lines,

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wherein said plurality of sense amplifiers are formed in a fourth area which is adjacent to said first and third areas.

35. A semiconductor memory device according to claim 34,

wherein said first and second, third and fourth areas are quadrilateral areas, and

wherein said third area is an intersection area which is indicated by extending said second and fourth areas.

36. A semiconductor memory device according to claim 35, further comprising:

a first line for delivering a first selection signal to be supplied to an input terminal of said first driver; and

a second line for delivering a second selection signal to be supplied to an input terminal of said second driver,

wherein first and second lines, said main word line and said first and second subword lines are extended to the same direction in said first area.

37. A semiconductor memory device according to claim 36,

wherein each of said first and second subdecoders has (a) a first MOSFET having a gate coupled to said first input terminal and a source-drain path provided between said second input terminal and said output terminal, (b) a second MOSFET having a gate coupled to said first input terminal and a source-drain path provided between said output terminal and a ground potential and (c) a third MOSFET having a source-drain path coupled to said source-drain path of said second MOSFET in parallel.

38. A semiconductor memory device according to claim 37,

wherein said first and second drivers are invertor circuits.

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39. A semiconductor memory device according to claim 37, wherein said first MOSFET is an p-type, and wherein said second and third MOSFETs are n-type.

40. A semiconductor memory device according to claim 39, wherein a gate width of said third MOSFET is narrower than that of said second MOSFET.

41. A semiconductor memory device according to claim 40, wherein a voltage level of a selected subword line is higher than a high level voltage of said data lines.

42. A semiconductor memory device comprising:

a memory array having a main word line, a plurality of subword lines corresponding to said main word line, a plurality of data lines and a plurality of memory cells each of which is arranged to correspond to an intersection of one of said data lines and one of said subword lines;

a plurality of subdecoder circuits each of which includes (a) p-type first MOSFET having a drain coupled to corresponding one of said subword lines and a gate coupled to said main word line, (b) an n-type second MOSFET having a source receiving a ground potential, a drain coupled to said drain of said first MOSFET and a gate coupled to said main word line and (c) a third MOSFET having a source-drain path coupled between said drain and source of said second MOSFET;

a plurality of signal lines each of which is coupled to a gate of corresponding said third MOSFET, wherein one of said signal lines is set to a selection level; and

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a plurality of drivers each of which has an input terminal coupled to corresponding one of said signal lines and an output terminal coupled to a source of corresponding said first MOSFET,

wherein said memory array is formed in a first quadrilateral region,

wherein said subdecoder circuits are formed in a second quadrilateral region which is adjacent to said first quadrilateral region, and

wherein said drivers are formed in a third quadrilateral region which is adjacent to said second quadrilateral region.

43. A semiconductor memory deice according to claim 42,

wherein said third MOSFET is an n-type,

wherein said selection level is low level, and

wherein said drive circuits are invertor circuits.

44. A semiconductor memory device according to claim 43,

wherein a voltage level of a selected subword line is higher than a high level voltage of said data lines.

45. A semiconductor memory device according to claim 44, further comprising:

a plurality of sense amplifiers coupled to said data lines,

wherein said sense amplifiers are formed in a fourth quadrilateral region which is adjacent to said first and third quadrilateral regions.

46. A semiconductor memory device according to claim 45,

wherein a gate width of said third MOSFET is narrower than that of said second MOSFET.

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47. A semiconductor device comprising:

an array of electronic circuits;

an electrical port located outside said array;

a first conductor electrically connected to said electrical port and disposed over said array;

a second conductor disposed over said array, wherein said second conductor crosses said first conductor at a cross point in said array;

a peripheral circuit located outside of said array, wherein said peripheral circuit is electrically connected to said second conductor, and;

means for electrically connecting said first and second conductors at said cross point,

wherein said peripheral circuit is electrically connected to said electrical port via said first and second conductor.

48. The apparatus of claim 47 further comprising:

a third conductor disposed outside of said array, wherein said third conductor crosses said second conductor at a second cross point outside of said array and,

means for electrically connecting said second and third conductors at said second cross point,

wherein said peripheral circuit is electrically connected to said second conductor via said third conductor.

49. The apparatus of claim 47 wherein said second conductor is formed in a separate layer from said first conductor.

50. The apparatus of claim 48 wherein said second conductor is formed in a separate layer from said third conductor.

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51. The apparatus of claim 47 wherein said array is a memory array and said electronic circuits are memory cells.

52. The apparatus of claim 47 wherein said peripheral circuit is a sense amplifier driver.

53. The apparatus of claim 47 wherein said means for electrically connecting comprises a through-hole.

54. The apparatus of claim 47 wherein said electrical port is a power pad, said first and second conductors are power buses.

55. The apparatus of claim 52 further comprising:

a first signal bus disposed over said array;

a second signal bus disposed over said array, wherein said second signal bus crosses said first signal bus at a second cross point in said array; and

means for electrically connecting said first and second signal buses at said second cross point.

56. The apparatus of claim 51 wherein each of said memory cells comprises:

a memory storage circuit;

a subword line; and

a main word line;

wherein said main word line is arranged in a hierarchical structure with said subword line.

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57. The apparatus of claims 56 further comprising a subdecoder circuit comprising three transistors.

58. The apparatus of claim 57 wherein said subdecoder circuit is connected to said peripheral circuit.

59. A method for supplying power and signals on an array-type semiconductor device comprising:

supplying power to a power source located outside said array;

forming a first power bus connected to said power source and disposed over said array;

forming a second power bus over said array, such that said second power bus crosses said first power bus at a cross point in said array;

electrically connecting a peripheral circuit located outside of said array to said second power bus; and

electrically connecting said first and second power buses at said cross point.

60. The method of claim 59 further comprising:

forming a third power bus outside said array such that said third power bus crosses said second power bus at a second cross point outside said array;

electrically connecting said third power bus to said second power bus outside said array; and

electrically connecting said peripheral circuit to said second power bus via said third power bus.

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61. The method of claim 59 wherein said first power bus is formed in a third metal layer and said second power bus is formed in a second metal layer.

62. The apparatus of claim 59 wherein said first power bus is formed in a separate layer from said second power bus.

63. The method of claim 59 wherein said array is a memory array.

64. The method of claim 63 wherein said peripheral circuit is a sense amplifier driver.

65. The method of claim 59 wherein said electrically connecting said first and second power buses is accomplished using a through-hole.

66. The method of claim 59 further comprising:

forming a first signal bus over said array;

forming a second signal bus over said array, such that said second power bus crosses said first signal bus at a second cross point in said array; and

electrically connecting said first and second signal buses at said second cross point.

67. The method of claim 66 wherein said electrically connecting said first and second signal buses is accomplished using a through-hole.

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