Method of Making Field Effect Transistors

This invention relates to the field of semiconductor device fabrication, and more particularly to methods for making field effect transistors. It is particularly applicable to short-channel devices, by which is meant those with source to drain lengths of less than about 2 micron.

In the manufacture of short channel devices with polycrystalline silicon gate electrodes, it is difficult to control the length of the polycrystalline silicon ("polysilicon") layer defining the gate and hence the channel length: this length is thus subject to fluctuations from device to device in the usual techniques of mass fabrication of many such devices at the surface of a single crystal silicon wafer. Specifically, the actual length of the channel is so small in many of the devices whose channels are supposed to be a micron in length that an undesirable "punch-through" (or "reach-through") of the depletion region of the drain to the source occurs during operation; thereby, performance of the device is degraded.

It has been recognized by workers in the art of metal oxide semiconductor field effect transistor (MOSFET) structures that a shallow source or drain diffusion (small junction depth) can yield desirable device characteristics. For example, in an article by R. Hori et al. entitled "Short Channel MOS-IC Based on Accurate

Two-Dimensional Device Design," published in Supplement to Japanese Journal of Applied Physics, Vol.15, pp. 193-199 (1976), it was recognised that relatively shallow source and drain junction depths could help yield a relatively low threshold voltage shift in a short-channel MOSFET structure as well as a relatively high punch-through breakdown voltage.

A short-channel MOSFET made by conventional techniques suffers from undesirable device properties stemming from a relatively high parasitic capacitance between the polycrystalline silicon ("polysilicon") gate electrode and the source or drain (or both). Similarly, a conventionally fabricated short-channel metal gate (Schottky barrier) field effect transistor (MESFET) device structure suffers from the problem of undesirably high ohmic resistance along a path from source or drain electrode (or both) to the conducting portion of the channel during operation in the ON state of the device.

In the invention set out in the claims an oxide coating on the side walls of a polycrystalline gate electrode act as part of a mask to delineate the source and drain regions, which are formed by treating (e.g. bombarding) exposed silicon areas with a transition metal such as platinum, cobalt, hafnium, titanium or tantalum to form a silicide. Shallow source and drain regions may thus be formed and, since the source and drain are almost entirely covered with conductive metal silicide the source and drain resistances are low.

Some embodiments of the invention will now be described by way of example with reference to the accompanying drawings of which:-

FIGS. 1-6 show in section a sequence of various stages in the fabrication of a MOSFET in accordance with the invention,

FIGS. 7-12 illustrate in section a sequence of

various stages in the fabrication of another form of MOSFET in accordance with the invention; and

FIG. 13 illustrates in section the final stage of a MESFET, in accordance with the invention.

As shown in the sequence, FIGS. 1-6, a short-channel MOSFET device (FIG. 6) is fabricated at a top major surface of a p-type (N-MOS technology) surface region or zone 10. As indicated in FIG. 1, this P-type region 10 is initially prepared with significant impurity doping to provide suitable electrical conductivities at the respective interfaces of this P-region 10 with a relatively thick field oxide layer 11 and a relatively thin gate oxide layer 112, as known in the art. A polycrystalline silicon ("polysilicon") layer 113 (FIG. 1) is then deposited over the field and gate oxide layers 11 and 112, to a thickness typically in the range of about 350 to 500 nanometres (3500 to 5000 angstroms). This polysilicon layer 113 is doped with significant donor impurities such as arsenic or phosphorus, particularly in the regions overlying the ultimate transistor devices and in regions of interconnections, in order to increase the electrical conductivity of the polysilicon to a range of values typically of about 10 to 100 ohms/square, which is suitable for a gate electrode in regions overlying the gate oxide where the polysilicon layer will function as a gate electrode and, at the same time, suitable for electrically conductive interconnections in regions overlying the field oxide where the polysilicon layer will function as an electrical interconnection (FIG. 6). Then a silicon dioxide masking layer 114, typically having a thickness in the range of about 100 to 200 nanometres (1000 to 2000 angstroms), is deposited on the exposed surface of the polysilicon layer by a conventional process such as oxidation in a dry atmosphere. By conventional photoresist, or electron beam or X-ray lithographic masking and etching, the oxide layer 114 and the polysilicon layer 113 are removed except at locations where a polysilicon gate

electrode layer 13 on the gate oxide 112 and a polysilicon interconnect layer 23 on the field oxide 11 are desired (FIG. 2). This gate electrode layer 13 will thus be coated on its top surface by a silicon dioxide gate masking layer 14'. Likewise, the polysilicon interconnecting layer 23 will thus be coated on its top surface with a silicon dioxide interconnect masking layer 24'. The width of the gate-electrode layer 13, in particular, can be as low as 0.8 micron, for short-channel devices.

Next, by thermal oxidation (FIG. 3), the sidewalls of the polysilicon layers 13 and 23 are coated with a thermally grown sidewall gate oxide layer 15 and a sidewall interconnect oxide layer 25, respectively. Typically, the thickness of these oxide layers 15 and 25 is in the range of about 20 to 50 nanometres (200 to 500 angstroms). Simultaneously with the growth of the oxide layer 15 and 25, the respective thicknesses of the oxide layers 14' and 24', as well as the field oxide layer 11, will all increase somewhat as a result of the respective simultaneous thermal oxidation of the underlying silicon or polysilicon. In case the length of the polysilicon layer 13 is less than what is desired for defining the length of the gate, a somewhat thicker oxide layer can be deposited on the sidewalls of the polysilicon, as by plasma deposition or low pressure chemical vapour deposition; so that the resulting thicker sidewall oxide then supplies a longer mask against the subsequent diffusion of source and drain impurities, thereby reducing impurity underdiffusion in the gate region and thus increasing the source to drain distance, as is desired in such a case.

Next (FIG. 4), the top surface of the body 10 is exposed to an anisotropic etching of the oxide layers, whereby the sidewall oxides 15 and 25 remain substantially intact while the oxide layers 14' and 24' are reduced in thickness to become oxide layers 14 and 24, respectively; and while the gate oxide layer 12

remains only in the gate region underlying the polysilicon layer 13 plus sidewall oxide 15, while the gate oxide layer 12 is completely removed in the regions between the sidewall oxide 15 and the field oxide 11, i.e., in the regions of the ultimate source and drain. A chemically reactive sputter etching (backsputtering) process using fluoride ions in a plasma produced by CHF_3 is employed for this anistropic etching of the oxide layers, as is described more fully below with reference to FIG. 9. This backsputtering process is terminated when the surface of the silicon body 10 is exposed in the source and drain regions, or a short time thereafter, so that there still remains some oxide in the layers 14 and 24 covering the top surface of the polysilicon electrode layers 13 and 23, respectively. Since the thickness of the masking oxide 114 is considerably greater than that of the gate oxide 12, a considerable margin thus exists to enable the remaining oxide layers 14 and 24 to be of sufficient thickness, typically of about 100 nanometres (1000 angstrom), to prevent the formation of silicide on the gate electrode 13.

Next, a donor impurity is introduced, as by ion implantation and diffusion, into the source and drain areas, to form diffused source and drain regions 10.1 and 10.2, respectively (FIG. 5), contiguous with the surface of the silicon body. For example, a dose of arsenic is implanted at about 30 Kev and diffused to a concentration typically in the range of about 10^{19} to 10^{20} per cubic centimetre. By "diffused" in this context is meant to include any thermal diffusion step either simultaneous with or subsequent to the impurity implantation step. Then the top surface of the body 10 is subjected to a bombardment with a metal, such as titanium, which forms metal silicide layers 16, 17, typically of a thickness of a few tens of nanometres (a few hundred angstroms), at the exposed portions of the silicon. The metal which remains after bombardment on the surface of the oxide areas is removed by etching; for example, titanium can be etched with

ethylene-diamine-tetra-acetic-acid (EDTA). This etching, however, leaves intact the metal silicide layers 16, 17. The amount of metal deposited on the oxide may be minimized by suitable adjustment of the various parameters of the metal bombardment so that the removal rate of titanium at the exposed oxide surfaces is greater than the arrival rate.

Next, the top surface of the body 10 is coated at selected areas by conventional deposition, masking, and etching techniques, with an insulating layer 22, such as tetra-ethyl-ortho-silicate, typically of a thickness in the range of about 0.5 to 1μm (5000 to 10,000 angstroms). By further conventional techniques, metallization is then applied contacting the metal silicide layers 16 and 17, in order to form the respective electrode metallization contacts 19 and 21 for the source and drain; at the same time, this metallization is also applied contacting the polysilicon layers 13 and 23 through apertures in the insulating layer 22, in order to form electrode metallization contacts 18 and 28 for the gate and the interconnections. It will be apparent from this description that reduced parasitic lateral resistance in the shallow source 10.1 and shallow drain 10.2 is afforded by the metal silicide layers 16 and 17, and that a reduced gate electrode overlap parasitic capacitance also results, as compared with more conventional methods.

As shown in the sequence of drawings, FIGS. 7-12, a short-channel MOSFET device 40 (FIG. 12) is fabricated on a top major surface of a monocrystalline semiconductive silicon body 30. As known in the art of semiconductor multiple device fabrication ("batch techniques"), many similar MOSFET devices can be simultaneously fabricated in such a body, all of these devices being mutually electrically isolated by relatively thick ("field") oxide region 31.

The body 30 is formed by a single crystal semiconductor bulk portion 29 upon a major planar surface of which has been grown an epitaxial semiconductor

layer 30.5. Typically, the semiconductor 29 is π-type conductivity silicon; that is, having a relatively low P-type conductivity, for example, a bulk conductivity of about 10 ohm cm. The epitaxial layer 30.5 is advantageously of moderate electrical conductivity, typically P-type, owing to a net significant acceptor impurity concentration ordinarily of the order of about 10^{15} to 10^{17} per cm^3, typically about 10^{16} per cm^3. The thickness of this epitaxial layer is typically about one or two micron or less.

In order to fabricate the MOSFET device 40 (FIG. 12), a thin ("gate oxide") silicon dioxide layer 32 (FIG. 7) is thermally grown on the exposed portion of the top surface of the body 30 typically to a thickness of about a few tens of nanometres (a few hundred angstrom). Either before or after the formation of this thin oxide layer, relatively thick oxide regions 31 are embedded, by means of a conventional thermal oxidation process, at selected portions of the epitaxial P layer down to the underlying π-type original crystal, in order to provide conventional oxide isolation between neighbouring devices. It should be understood that electron beam or x-ray lithography, as well as photolithography, can be used in combination with standard resist masks to define the areas of selective formation of the thick oxide. Then an electrically conductive N-type polycrystalline silicon layer 33' is deposited on a pre-selected area of the exposed surface of the thin oxide as formed by conventional resist masking and etching techniques applied to a polycrystalline layer originally deposited all over the top surface, using lithography (electron beam, x-ray, or photo) techniques to shape the mask. This polycrystalline layer 33' is typically N-type semiconductor owing to its being doped with significant donor impurities--such as arsenic--to increase its electrical conductivity, and it has a length of typically about 1.0 micron in the direction of the source to drain channel of the completed device and a width of typically a few microns in the transverse

direction thereto. This polysilicon layer is thus useful as the gate electrode of the completed transistor device.

Next, the exposed top and side surfaces of the polycrystalline silicon layer 33' are subjected to a conventional oxidation technique, which oxidizes the polycrystalline silicon to yield a thin silicon dioxide coating layer 34 on the surfaces of the thus remaining, unoxidized N-type polycrystalline layer 33 (FIG. 8). Typically, this oxide coating 34 has a thickness of about 50 nanometres (500 angstrom). As a result of this oxidation of the polycrystalline layer, the thickness of the original oxide layer 32 (FIG. 7) is increased somewhat, as indicated by oxide layer 32' (FIG. 8).

Then, the exposed portion of the thin oxide layer 32' and the top portion (but not side portions) of the thin oxide layer 34 are removed (FIG. 9) by an anisotropic etching technique, such as chemically reactive backsputtering (reactive ion etching) with fluoride ions (F^+) in a plasma produced by CHF_3. By "anisotropic" etching is meant etching preferentially in the direction perpendicular to the major surface of the body 30. For example, a cathode plate 52, typically of platinum, is located at a distance typically of several times 2.5 cm from the body 10 in an evacuated chamber (not shown). This body is mounted on an electrically conducting plane (not shown) connected through a capacitor C to an RF voltage source E, typically about 500 volts peak to peak at a frequency in the range of about 200KHz to 14MHz, typically 13.5MHz. The pressure in the chamber is reduced to below about 130 Pa (1mm Hg), typically about 6.5 Pa (50 micron Hg), in order that, while a plasma forms in the neighbourhood of the cathode plate 52, the top surface of the epitaxial layer 30.5 remains inside a dark space region of the discharge from the cathode plate 52. The RF power is typically about 20 to 100 watts for a cathode several times 2.5cm in diameter, and the temperature of the body is maintained at typically about 500°C. In this manner, the fluoride ions bombarding any element (including

the oxide and polysilicon layer) located at the top surface of the body 30 strike it from a direction which is essentially normal to the top major surface of the epitaxial layer 30.5; thereby these ions completely remove the thin oxide only at the surface portions where the normal to the surface is parallel to the velocity vector of the bombarding ion, but not at the side portions. In so removing the thin oxide portions, however, it is important that the side surfaces of the polysilicon layer 33 thus remain coated with the thus remaining (sidewall) portions of the oxide layer 34. The thickness (in the horizontal direction) of this remaining sidewall oxide is typically about 50 nanometres (500 angstrom), and is in any event advantageously equal to, or less than, approximately the Debye length in the silicon in the region of the source-channel interface of the ultimately completed device.

Next, as indicated in FIG. 10, positively charged argon ions are directed upon a platinum cathode target 51 in order to sputter platinum from the target onto the body 30. These positive argon ions have suitable kinetic energies due to an accelerating voltage E_1 (of negative polarity) applied to the target. This sputtering of platinum results in the arrival of platinum atoms and/or platinum ions at the exposed top surface of the epitaxial layer 30.5 where the platinum accumulates on the exposed silicon as metal-like platinum silicide electrode layers 35, 36 and 37. The voltages E_1 and E_2 are adjusted so that the removal rate of platinum from the exposed oxide portions of the top surface is greater than the arrival rate. Thus, essentially no metal or metal-like substance of any kind (platinum or platinum silicide) accumulates on any portion of exposed oxide, either the field oxide or the gate oxide. However, if any metal should accumulate on the oxide, a subsequent treatment with a conventional etching solution, such as aqua regia, can be used to remove this metal but not the silicide or oxide layers.

The donor impurity dopant arsenic or antimony

(or both) can advantageously be added to the target 51 for the purpose of simultaneously forming by "co-sputtering" a pair of spaced apart, self-aligned N+ zones 30.1 and 30.2 during the bombardment with platinum. These N+ zones are formed by rejection from the platinum silicide of the impurity dopant into the silicon ("segregation"). Because all subsequent processing temperatures are well below the temperature at which significant diffusion of impurities in silicon occurs, the depth of the resulting N+ P junctions in the silicon (beyond the platinum silicide) can be as little as 10 nanometres (100 angstrom) or less.

Alternatively, the N+ zones 30.1 and 30.2 can be formed at an earlier stage of the fabrication--for example, by means of conventional techniques as ion implantation and diffusion of donor impurities using the polycrystalline layer 33 with sidewall oxide 34 as a mask which is impervious to these impurities.

Typical values of the parameters useful for this platinum bombardment step are: E_1 is a direct voltage equal to about 1000 volts, and E_2 is an RF voltage in the range of typically about 500 to 1000 volts peak to peak at a frequency of about 13 MHz. The RF power is typically about 20 to 100 watts for a cathode 51 of several times 2.5cm in diameter. The frequency and amplitude of E_2 control the removal rate of platinum and platinum silicide during the bombardment. The fact that the removal rate of platinum is thus made to be about two or more times that of platinum silicide tends to ensure the net removal of any metallic platinum initially arriving on the exposed oxide while the net permanent formation and accumulation of platinum silicide occurs on the exposed silicon (whether monocrystalline or polycrystalline). The temperature of the body 30 during this sputtering process is typically about 625°C., while the ambient pressure of argon is typically about 1.3 to 2.6 Pa (10 to 20 micron Hg).

After the formation of the platinum silicide layers 35, 36 and 37 on the exposed silicon surfaces to a

thickness of typically about a few tens of nanometres (a few hundred angstrom), the top surface of the body 30 is coated at selected areas with an insulating layer 42 (FIG. 11) by conventional deposition, masking, and etching techniques. This layer 42 is typically tetra-ethyl-ortho-silicate having a thickness of, for example, about 500 nanometres (5000 angstrom). By conventional techniques, metallization such as aluminum is then applied through apertures in the layer 42 to contact the platinum silicide layers 35, 36, and 37, in order to form the respective electrode metallization contacts 38, 39, and 41 for the gate, source, and drain, respectively, of the completed MOSFET device 40 (FIG. 12).

It should be noted that during operation, a back-gate (substrate) bias voltage of magnitude two volts or more is desirable, in order to prevent short circuits of different devices due to surface channels under the thick (field) oxide. Alternatively, such channels can be avoided by using a ν-type (low conductivity N-type) body 30.

For good transistor device performance, it is useful to have the source and drain regions 30.1 and 30.2 as shallow as possible; that is, the implantation process for these regions should limit their depths beneath the surface of the semiconductor body to a value of about a few tens of nanometres (a few hundred angstrom), which can be achieved by using a semiconductor body temperature of no greater than 500°C during any fabrication step subsequent to the diffusion of these N+ zones.

As illustrated in FIG. 13, the growth of the thin oxide layer 32 can be completely omitted, so that the N-type polycrystalline silicon layer 33 directly contacts the top surface of the silicon semiconductor body 30, thereby forming a PN junction thereat. The resulting device is thus a junction FET device ("JFET"). In this device (FIG. 13), the N+ regions 30.1 and 30.2 are replaced by P+ regions 51.1 and 51.2, respectively,

so that the device has a relatively low barrier Schottky source and a relatively low barrier Schottky drain; for example, a barrier of 0.25 volts in the case of platinum silicide on P-type silicon. Conversely, on this P-type silicon, a relatively high Schottky barrier of about 0.65 volt is formed by using hafnium silicide in place of platinum silicide,

The distance between drain and gate can be made larger than that between source and gate, by locating the electrode 37 farther away from the polysilicon layer 33, so that this electrode does not directly physically contact the oxide layer 34, in order to provide a longer drift region in the neighbourhood of the drain. On the other hand, the P+ regions 51.1 or 51.2 (or both) can be omitted in the device illustrated in FIG. 13. Also, care must be taken that the diffusion of these regions 51.1 and 51.2 does not extend either of these regions laterally to the polycrystalline layer 33; otherwise, an undesirable short circuit of the gate electrode to source or drain (or both) will occur.

Moreover, again omitting the thin oxide layer 32, a metal gate FET ("MESFET") structure can be obtained by carrying out the metal bombardment step (FIG. 10) for sufficiently long a time that the polycrystalline layer 33 is completely converted to metal-silicide. In such a case, it is advantageous to use a relatively high barrier Schottky metal such as hafnium for forming the silicide in the case of a P-type silicon layer 30.5. (platinum for N-type silicon), together with a pair of localized diffused P+ type zones instead of the localized N+ zones 30.1 and 30.2 in the P-type silicon layer 30.5 (or to retain the localized N+ zones 30.1 and 30.2 but in an N-type epitaxial layer instead of the P-type layer 30.5). Again, each (or both) of the localized diffused zones can be omitted (specially at the source region), whereby the source or (and) the drain can be of the Schottky barrier type.

Instead of growing the epitaxial P-type layer 30.5,

the top surface of the original π-type semiconductor base 29 can be treated with excess acceptor impurities. This π-type base 29 contains about 10^{16} per cm^3 excess significant acceptor impurities. In an example, solely for illustrative purposes, upon the top surface of the original π-type base 29 are successively formed a 35 nanometre (350 angstrom) thermally grown layer of silicon dioxide and a 120 nanometre (1200 angstrom) layer of silicon nitride. Using a photo or x-ray or electron beam resist material as a mask, the silicon nitride layer is removed from the areas where the thick isolation oxide is to be formed; that is, the nitride layer is removed only in the complement of the GASAD (gate and source and drain) areas. Leaving the resist in place as an impervious mask against ion implantation, a channel ("chan") stop is formed by implanting boron ions of typically about 100 kev to a dose of typically about 10^{12} to 10^{13} per square centimetre in the complement of the GASAD areas. Then the resist material is removed, leaving the nitride layer in place, and a thick 900 nanometre (9000 angstrom) field oxide layer is thermally grown in the field oxide areas (complement of the GASAD areas) while the top portion of the nitride layer in the GASAD areas is converted into an oxynitride layer. Next, successively using etching solutions of buffered hydrofluoric acid and phosphoric acid, the oxynitride and nitride layers, respectively, are successively removed from the GASAD areas while only a small fraction of the oxide layer is thereby removed from the thick field oxide layer. Then thermal growth produces a total of 300 nanometre (3000 angstrom) of silicon dioxide in the GASAD areas and a total of about 950 nanometre (9500 angstrom) of silicon dioxide in the field oxide area. Next, all the oxide in the GASAD areas is removed by etching with buffered hydrofluoric acid, while the field oxide thickness is reduced to about 650 nanometre (6500 angstrom). Then another thermal growth step produces a layer of silicon dioxide in the GASAD areas having a thickness in the range of about 10 to 50

nanometre (100 to 500 angstrom), typically 12.5 nanometre (125 angstrom). Next, boron ions are implanted with 35 kev energy, sufficient to penetrate to the underlying silicon only in the GASAD areas, to a dose of 2×10^{12} boron ions per square centimetre, in order to provide a convenient operating threshold voltage in the ultimate transistor devices of the enhancement mode type. If depletion mode devices are also to be formed at some of the GASAD areas, then a resist material is applied to these areas prior to the 35 kev boron ion implantation. This resist is then removed after this boron implantation; next, the oxide is completely removed from all the GASAD areas (a small fraction from the field oxide areas); and finally the oxide layer 32 (FIG. 7) is thermally grown.

Although the invention has been described in terms of specific embodiments, various modifications can be made without departing from the scope of the invention. For example, in the embodiments described with reference to FIGS 7-13, the semiconductor base 29 can be ν-type (low conductivity N-type) instead of π-type. Moreover, N-type and P-type conductivity can be everywhere interchanged in all the above-described devices. Also, instead of using fluoride ions to remove the oxide (FIG.9), other ions, such as argon, may be used; that is, either a chemically reactive or nonreactive ion etching may be used for the oxide removal step. Moreover, instead of platinum, other transition metals can be used, such as cobalt, hafnium, titanium, or tantalum, each of which forms a metal-silicide suitable for a Schottky barrier on silicon. Moreover, the N+ region 30.1 or 30.2 (or both) can also be omitted from the device shown in FIG. 12, thereby forming a Schottky barrier source or drain (or both) in a MOSFET structure. Instead of forming the platinum silicide by sputtering, platinum itself can first be evaporated all over the surface and then be converted into platinum silicide by means of a temperature "spike" treatment typically of about 400 to 650°C for typically about 2 to 6 minutes; the platinum remaining as such or the oxide can thereafter be removed by etching with hot aqua regia.

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CLAIMS

1. A method of making a short-channel field effect transistor in a silicon semiconductor body wherein a polycrystalline silicon gate electrode is formed with a silicon dioxide coating on the side walls thereof, a silicon source area and drain area in the body being left uncovered and the body is treated with a transition metal so as to form a layer of conductive metal silicide on the exposed silicon areas to form source and drain regions.

2. A method as claimed in claim 1 wherein the oxide layer initially extends over the source and drain area and including an anisotropic etching step which preferentially removes oxide from the source and drain areas rather than from the side surfaces of the gate electrode and which is carried out for a time which is sufficiently long that the oxide is completely removed from the said areas.

3. A method as claimed in claim 2 wherein prior to the anisotropic etching step there is an oxide layer on the top surface of the gate electrode which is thicker than the oxide on the said areas and the time for which the etching step is carried out is short enough to leave an oxide layer on the top surface of the gate electrode.

4. A method as claimed in claim 1 or claim 2 wherein at the time of the transition metal treatment the upper surface of the gate electrode is uncovered so that metal silicide is formed on the gate electrode.

5. A method as claimed in claim 4 wherein the metal silicide extends throughout the whole thickness of the gate electrode.

6. A method as claimed in any of the preceding claims wherein the transition metal treatment comprises bombarding the body with the transition metal.

7. A method as claimed in claim 6 wherein during the bombardment a voltage is applied to the body such that substantially no metal or metal silicide accumulates on any oxide-covered portions of the body.

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8. A method as claimed in any of the preceding claims wherein the transition metal is platinum, cobalt, hafnium, titanium or tantalum.

9. A method as claimed in any of the preceding claims in which a polycrystalline interconnect electrode is formed on a field oxide layer simultaneously with the forming of the gate electrode, the field oxide layer being sufficiently thick that it is not completely removed by the etching step.

10. A method as claimed in claim 9 in which an oxide layer is formed on a side surface of the interconnect electrode simultaneously with the forming of the oxide layer on the side surfaces of the gate electrode.

11. A method for forming a field effect transistor substantially as herein described with reference to FIGS. 1 to 6 or FIGS. 7 to 14, or FIGS. 7 to 12 with FIG. 13 of the accompanying drawings.

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