

CLAIMS

1. A method for forming a semiconductor device, the method comprising:
forming a nanosheet stack over a substrate;
forming a dielectric pillar adjacent to the nanosheet stack, the dielectric pillar positioned on a shallow trench isolation region of the substrate;
recessing the nanosheet stack to expose a surface of the shallow trench isolation region;
forming a source or drain (S/D) region on the exposed surface of the shallow trench isolation region; and
forming a contact trench exposing a surface of the S/D region and a surface of the dielectric pillar.
2. The method of claim 1 further comprising forming a bottom isolation structure between the substrate and the nanosheet stack.
3. The method of claim 1 further comprising forming a conformal liner over the S/D region and the dielectric pillar.
4. The method of claim 3 further comprising forming an interlayer dielectric over the conformal liner.
5. The method of claim 4, wherein forming the contact trench comprises removing a portion of the interlayer dielectric and a portion of the conformal liner.
6. The method of claim 1 further comprising forming a trench silicide in the contact trench.
7. The method of claim 1, the method comprising:
forming a bottom isolation structure on a substrate;
forming the nanosheet stack on the bottom isolation structure, the bottom isolation structure between the nanosheet stack and the substrate;
forming a conformal liner over the S/D region and the dielectric pillar;
forming an interlayer dielectric over the conformal liner;
removing a portion of the interlayer dielectric and a portion of the conformal liner to form the contact trench; and
forming a trench silicide in the contact trench.
8. The method of claim 1 or claim 7 further comprising, prior to forming the dielectric pillar, forming a sacrificial region over the nanosheet stack.
9. The method of claim 8 further comprising recessing the nanosheet stack to expose a surface of the shallow trench isolation region.

10. The method of claim 8, wherein recessing the nanosheet stack comprises removing the sacrificial region.
11. The method of claim 5 or 7, wherein the dielectric pillar serves as an etch stop while forming the contact trench.
12. A semiconductor device comprising:
 - a nanosheet stack positioned over a substrate;
 - a dielectric pillar adjacent to the nanosheet stack, the dielectric pillar positioned on a shallow trench isolation region of the substrate;
 - a source or drain (S/D) region on a surface of the shallow trench isolation region; and
 - a trench silicide on a surface of the S/D region and a surface of the dielectric pillar.
13. The semiconductor device of claim 12, wherein the S/D region is confined between opposite sidewalls of the dielectric pillar.
14. The semiconductor device of claim 12 further comprising a bottom isolation structure between the substrate and the nanosheet stack.
15. The semiconductor device of claim 12 further comprising a conformal liner over the dielectric pillar.
16. The semiconductor device of claim 15 further comprising an interlayer dielectric over the conformal liner, wherein the trench silicide is positioned between opposite sidewalls of the interlayer dielectric.