plurality of contacts 32, a plurality of interconnection layers 33, and a plurality of vias 34.

[0024]

The plurality of transistors 31 are provided on the semiconductor substrate 21. The transistor 31 is, for example, a field effect transistor. In the present embodiment, the transistor 31 is a metal oxide semiconductor field effect transistor (MOSFET). The transistor 31 includes, for example, a source region and a drain region formed on an upper surface portion of the semiconductor substrate 21.

[0025]

The plurality of contacts 32 have conductivity and extend in the Z direction. Each of the contacts 32 is in contact with a source region, a drain region, or a gate electrode of the transistor 31. The plurality of interconnection layers 33 are disposed above the plurality of transistors 31. The plurality of interconnection layers 33 are separately disposed at a plurality of heights. Each of the interconnection layers 33 includes a plurality of interconnections 33a extending in the X direction or the Y direction. The plurality of interconnections 33a each include an interconnection 33a connected to the contact 32. Each via 34 extends in the Z direction and connects two interconnections 33a disposed at different heights.

[0026]

The first insulating portion 23 is an insulating portion provided on the semiconductor substrate 21. The first insulating portion 23 covers the plurality of transistors 31, the plurality of contacts 32, the plurality of interconnection layers 33, and the plurality of vias 34. The first insulating portion 23 is formed of an insulating material such as, for example, silicon oxide. The first insulating portion 23 is formed of, for example, a silicon oxide deposited using tetraethyl orthosilicate (TEOS,

33 inside the first chip 2. The first through contact 121 is connected to the first interconnection 101A included in the upper layer interconnection portion 100 inside the second chip 3 (for example, at a position above the upper end 55b of the memory pillar 55).

[0087]

The second electrical connection portion 112 is a connection portion that electrically connects another transistor 31 included in the peripheral circuit 22 and the second interconnection 101B included in the upper layer interconnection portion 100. That is, the second electrical connection portion 112 electrically connects the transistor 31 included in the peripheral circuit 22 and the bit line BL. The second electrical connection portion 112 includes a second through contact 122. The second through contact 122 has conductivity and extends in the Z direction.

[0088]

The second through contact 122 penetrates the second insulating portion 42 of the second chip 3 and at least a part of the first insulating portion 23 of the first chip 2. The second through contact 122 extends in the Z direction from below the source line SL to above the upper end 55b of the memory pillar 55, and electrically connects the transistor 31 of the peripheral circuit 22 to the bit line BL. The second through contact 122 is connected to the interconnection 33a included in the interconnection layer 33 inside the first chip 2. The second through contact 122 is connected to the interconnections 101B included in the upper layer interconnection portion 100 inside the second chip 3 (for example, at a position above the upper end 55b of the memory pillar 55).

[0089]

The third electrical connection portion 113 is a connection portion that

electrically connects another transistor 31 included in the peripheral circuit 22 and the third interconnection 101C included in the upper layer interconnection portion 100. That is, the third electrical connection portion 113 connects the transistor 31 included in the peripheral circuit 22 and the pad 44. The third electrical connection portion 113 includes a third through contact 123. The third through contact 123 has conductivity and extends in the Z direction.

[0090]

The third through contact 123 penetrates the second insulating portion 42 of the second chip 3 and at least a part of the first insulating portion 23 of the first chip 2 in the Z direction. The third through contact 123 is connected to the interconnection 33a included in the interconnection layer 33 inside the first chip 2. The third through contact 123 is connected to the interconnection 101C included in the upper layer interconnection portion 100 inside the second chip 3 (for example, at a position above the upper end 55b of the memory pillar 55).

[0091]

<7. Other configurations>

As shown in FIGS. 3 and 7, in the present embodiment, there is no copper pad for bonding the first chip 2 and the second chip 3 together. In other words, there is no copper pad between the source line SL and the semiconductor substrate 21.

[0092]

<8. Manufacturing method>

Next, a method of manufacturing the semiconductor storage device 1 will be described.

FIG. 9 is a diagram showing a flow of a method of manufacturing the semiconductor storage device 1. FIGS. 10A to 10P are views for explaining a method

storage device 1 shown in FIG. 16. In the present embodiment, as described above, the staircase portion 80 is provided at the center of the multi-layered body 51 in the X direction. The plurality of contacts 81 are provided at the center of the multi-layered body 51 in the X direction to correspond to an upper side of the staircase portion 80. The plurality of contacts 81 have different lengths in the Z direction. A lower end of each of the contacts 81 is in contact with a terrace portion of the corresponding conductive layer 61.

[0136]

For example, the plurality of contacts 81 include a first contact 81A, a second contact 81B, and a third contact 81C. The first contact 81A is provided corresponding to a terrace portion of the first conductive layer 61A and is in contact with the terrace portion of the first conductive layer 61A. The second contact 81B extends further downward than the first contact 81A. The second contact 81B is provided corresponding to a terrace portion of the second conductive layer 61B and is in contact with the terrace portion of the second conductive layer 61B. The third contact 81C extends further downward than the second contact 81B. The third contact 81C is provided corresponding to a terrace portion of the third conductive layer 61C and is in contact with the terrace portion of the third conductive layer 61C.

[0137]

According to such a configuration, as in the first embodiment, a source line SL can be formed in a state in which the source line SL is positioned above a multi-layered body 210. Therefore, manufacturability of the semiconductor storage device 1 can be improved.

[0138]

According to at least one of the embodiments described above, a semiconductor

source line extending at least in a second direction intersecting the first direction, wherein

the pillar has a first end and a second end,

the first end is in contact with the source line,

the second end is positioned on a side opposite to the first end in the first direction,

the first end has a width in the second direction, and

the width of the first end is larger than a width of the second end in the second direction.

[0141]

[2] In the semiconductor storage device described in [1],

the source line has a surface facing the multi-layered body, and

the memory film extends in the first direction within the pillar,

the memory film is in contact with the surface of the source line, and

the memory film does not protrude to a side of the substrate beyond the surface of the source line.

[0142]

[3] In the semiconductor storage device described in [1] or [2],

the pillar includes a first connection portion,

the first connection portion is disposed at least between the insulating core and the source line, and

the first connection portion contains polysilicon.

[0143]

[4] In the semiconductor storage device described in [1] or [2],

the source line has a surface facing the multi-layered body,

CLAIMS

[Claim 1] A semiconductor storage device comprising:

a substrate;

a transistor provided on the substrate;

a multi-layered body disposed on a side opposite to the substrate with respect to the transistor, the multi-layered body including a plurality of gate electrode layers and a plurality of insulating layers, the plurality of gate electrode layers and the plurality of insulating layers being alternately stacked one by one in a first direction;

a pillar extending in the first direction within the multi-layered body, the pillar including an insulating core, a channel layer, and a memory film, the channel layer being disposed between the plurality of gate electrode layers and the insulating core, the memory film being disposed between the plurality of gate electrode layers and the channel layer; and

a source line disposed between the multi-layered body and the substrate, the source line extending at least in a second direction intersecting the first direction, wherein

the pillar has a first end and a second end,

the first end is in contact with the source line,

the second end is positioned on a side opposite to the first end in the first direction,

the first end has a width in the second direction, and

the width of the first end is larger than a width of the second end in the second direction.

[Claim 2] The semiconductor storage device according to claim 1, wherein

the source line has a surface facing the multi-layered body,

the memory film extends in the first direction within the pillar,

the memory film is in contact with the surface of the source line, and

the memory film does not protrude to a side of the substrate beyond the surface of the source line.

[Claim 3] The semiconductor storage device according to claim 1, wherein

the pillar includes a first connection portion,

the first connection portion is disposed at least between the insulating core and the source line, and

the first connection portion contains polysilicon.

[Claim 4] The semiconductor storage device according to claim 1, wherein

the source line has a surface facing the multi-layered body,

the insulating core extends in the first direction within the pillar,

the insulating core is in contact with the surface of the source line, and

the insulating core does not protrude to a side of the substrate beyond the surface of the source line.

[Claim 5] The semiconductor storage device according to claim 1, wherein

a copper pad is not present between the source line and the substrate.

[Claim 6] The semiconductor storage device according to claim 1, wherein

the source line contains at least one of silicon and tungsten.

[Claim 7] The semiconductor storage device according to claim 1, further comprising

a bit line disposed on a side opposite to the source line with respect to the pillar, the bit line extending in a third direction intersecting the first direction and the second direction, wherein

the second end of the pillar is electrically connected to the bit line.

[Claim 8] The semiconductor storage device according to claim 7, further comprising:

a peripheral circuit including the transistor; and

a contact, wherein

when a side on which the multi-layered body is positioned is defined as an upper side as viewed from the substrate, the contact extends in the first direction from below the source line to above the second end of the pillar,

the contact electrically connects the peripheral circuit and the bit line.

[Claim 9] The semiconductor storage device according to claim 7, further comprising a connection interconnection portion, wherein

the pillar has a second connection portion,

the second connection portion is disposed between at least the insulating core and the bit line,

the second connection portion contains polysilicon,

the connection interconnection portion includes a plurality of copper interconnections,

the plurality of copper interconnections are disposed above the second connection portion in the semiconductor storage device, and

copper interconnections are not present below the second connection portion.

[Claim 10] The semiconductor storage device according to claim 1, further comprising a plurality of contacts, wherein

the plurality of gate electrode layers include a first gate electrode layer, a second gate electrode layer, and a third gate electrode layer,

the second gate electrode layer is disposed between the first gate electrode layer and the substrate,

the third gate electrode layer is disposed between the second gate electrode layer and the substrate,

the plurality of contacts include a first contact, a second contact, a third contact,

the first contact is in contact with the first gate electrode layer,

the second contact extends further to a side of the substrate than the first contact,

the second contact is in contact with the second gate electrode layer,

the third contact extends further to a side of the substrate than the second contact, and

the third contact is in contact with the third gate electrode layer.

[Claim 11] The semiconductor storage device according to claim 1, further comprising

a dividing portion penetrating the multi-layered body in the first direction, the dividing portion extending in the second direction, the dividing portion dividing each of the plurality of gate electrode layers in a third direction intersecting the first direction and the second direction, wherein

the dividing portion has a third end and a fourth end,

the third end is in contact with the source line,

the fourth end is positioned on a side opposite to the third end in the first

direction,

the third end has a width in the third direction, and

the width of the third end is smaller than a width of the fourth end in the third direction.

[Claim 12] The semiconductor storage device according to claim 1, further comprising

a dividing portion penetrating the multi-layered body in the first direction, the dividing portion extending in the second direction, the dividing portion dividing each of the plurality of gate electrode layers in a third direction intersecting the first direction and the second direction, wherein

the dividing portion has a third end and a fourth end,

the third end is in contact with the source line,

the fourth end is positioned on a side opposite to the third end in the first direction,

the third end has a width in the third direction, and

the width of the third end is larger than a width of the fourth end in the third direction.

[Claim 13] A semiconductor storage device comprising:

a substrate;

a transistor provided on the substrate;

a multi-layered body disposed on a side opposite to the substrate with respect to the transistor, the multi-layered body including a plurality of gate electrode layers and a plurality of insulating layers, the plurality of gate electrode layers and the plurality of insulating layers being alternately stacked one by one in a first direction;

a pillar extending in the first direction within the multi-layered body, the pillar including an insulating core, a channel layer, and a memory film, the channel layer being disposed between the plurality of gate electrode layers and the insulating core, the memory film being disposed between the plurality of gate electrode layers and the channel layer; and

a source line disposed between the multi-layered body and the substrate, the source line extending at least in a second direction intersecting the first direction, wherein

the source line has a surface facing the multi-layered body, and

the memory film extends in the first direction within the pillar,

the memory film is in contact with the surface of the source line, and

the memory film does not protrude to a side of the substrate beyond the surface of the source line.

[Claim 14] A semiconductor storage device comprising:

a substrate;

a transistor provided on the substrate;

a multi-layered body disposed on a side opposite to the substrate with respect to the transistor, the multi-layered body including a plurality of gate electrode layers and a plurality of insulating layers, the plurality of gate electrode layers and the plurality of insulating layers being alternately stacked one by one in a first direction;

a pillar extending in the first direction within the multi-layered body, the pillar including an insulating core, a channel layer, and a memory film, the channel layer being disposed between the plurality of gate electrode layers and the insulating core, the memory film being disposed between the plurality of gate electrode layers and the

channel layer; and

a source line disposed between the multi-layered body and the substrate, the source line extending at least in a second direction intersecting the first direction, wherein

the pillar includes a first connection portion,

the first connection portion is disposed at least between the insulating core and the source line, and

the first connection portion contains polysilicon.

[Claim 15] A semiconductor storage device comprising:

a substrate;

a transistor provided on the substrate;

a multi-layered body disposed on a side opposite to the substrate with respect to the transistor, the multi-layered body including a plurality of gate electrode layers and a plurality of insulating layers, the plurality of gate electrode layers and the plurality of insulating layers being alternately stacked one by one in a first direction;

a pillar extending in the first direction within the multi-layered body, the pillar including an insulating core, a channel layer, and a memory film, the channel layer being disposed between the plurality of gate electrode layers and the insulating core, the memory film being disposed between the plurality of gate electrode layers and the channel layer; and

a source line extending at least in a second direction intersecting the first direction, wherein

the pillar has a first end and a second end,

the first end is in contact with the source line,

the second end is positioned on a side opposite to the first end in the first direction,

the first end has a width in the second direction,

the width of the first end is larger than a width of the second end in the second direction, and

a copper pad is not present between the source line and the substrate.

[Claim 16] A semiconductor storage device comprising:

a substrate;

a transistor provided on the substrate;

a multi-layered body disposed on a side opposite to the substrate with respect to the transistor, the multi-layered body including a plurality of gate electrode layers and a plurality of insulating layers, the plurality of gate electrode layers and the plurality of insulating layers being alternately stacked one by one in a first direction;

a pillar extending in the first direction within the multi-layered body, the pillar including an insulating core, a channel layer, and a memory film, the channel layer being disposed between the plurality of gate electrode layers and the insulating core, the memory film being disposed between the plurality of gate electrode layers and the channel layer; and

a source line extending at least in a second direction intersecting the first direction, and

a plurality of contacts, wherein

the pillar has a first end and a second end,

the first end is in contact with the source line,

the second end is positioned on a side opposite to the first end in the first

direction,

the first end has a width in the second direction,

the width of the first end is larger than a width of the second end in the second direction,

the plurality of gate electrode layers include a first gate electrode layer, a second gate electrode layer, and a third gate electrode layer,

the second gate electrode layer is disposed between the first gate electrode layer and the substrate,

the third gate electrode layer is disposed between the second gate electrode layer and the substrate,

the plurality of contacts include a first contact, a second contact, a third contact,

the first contact is in contact with the first gate electrode layer,

the second contact extends further to a side of the substrate than the first contact,

the second contact is in contact with the second gate electrode layer,

the third contact extends further to a side of the substrate than the second contact, and

the third contact is in contact with the third gate electrode layer.

[Claim 17] A semiconductor storage device comprising:

a substrate;

a transistor provided on the substrate;

a multi-layered body disposed on a side opposite to the substrate with respect to the transistor, the multi-layered body including a plurality of gate electrode layers and a plurality of insulating layers, the plurality of gate electrode layers and the plurality of insulating layers being alternately stacked one by one in a first direction;

a pillar extending in the first direction within the multi-layered body, the pillar including an insulating core, a channel layer, and a memory film, the channel layer being disposed between the plurality of gate electrode layers and the insulating core, the memory film being disposed between the plurality of gate electrode layers and the channel layer; and

a dividing portion penetrating the multi-layered body in the first direction, the dividing portion extending in a second direction intersecting the first direction, the dividing portion dividing each of the plurality of gate electrode layers in a third direction intersecting the first direction and the second direction; and

a source line extending at least in the second direction intersecting the first direction, wherein

the pillar has a first end and a second end,

the first end is in contact with the source line,

the second end is positioned on a side opposite to the first end in the first direction,

the first end has a width in the second direction,

the width of the first end is larger than a width of the second end in the second direction, and

the dividing portion has a third end and a fourth end,

the third end is in contact with the source line,

the fourth end is positioned on a side opposite to the third end in the first direction,

the third end has a width in the third direction, and

the width of the third end is smaller than a width of the fourth end in the third direction.

[Claim 18] A method of manufacturing a semiconductor storage device comprising:

preparing a first chip and a second chip, wherein

the first chip includes:

a substrate;

a transistor provided on the substrate; and

a first insulating portion covering the transistor, and

the second chip includes:

a multi-layered body including a plurality of first layers and a plurality of second layers, the plurality of first layers and the plurality of second layers being alternately stacked one by one in a first direction;

a pillar extending in the first direction within the multi-layered body, the pillar including an insulating core, a channel layer, and a memory film, the channel layer being disposed between the first layer and the insulating core, the memory film being disposed between the first layer and the channel layer;

a source line extending at least in a second direction intersecting the first direction; and

a second insulating portion covering the source line, and

wherein

the method comprises bonding the first insulating portion and the second insulating portion together such that the source line is positioned between the multi-layered body and the first chip.

[Claim 19] The method of manufacturing a semiconductor storage device according to claim 18, wherein

the first layer is a sacrificial layer replaced with a conductive layer after the first insulating portion and the second insulating portion are bonded to each other.

[Claim 20] The method of manufacturing a semiconductor storage device according to claim 18, wherein

the first layer is a conductive layer.