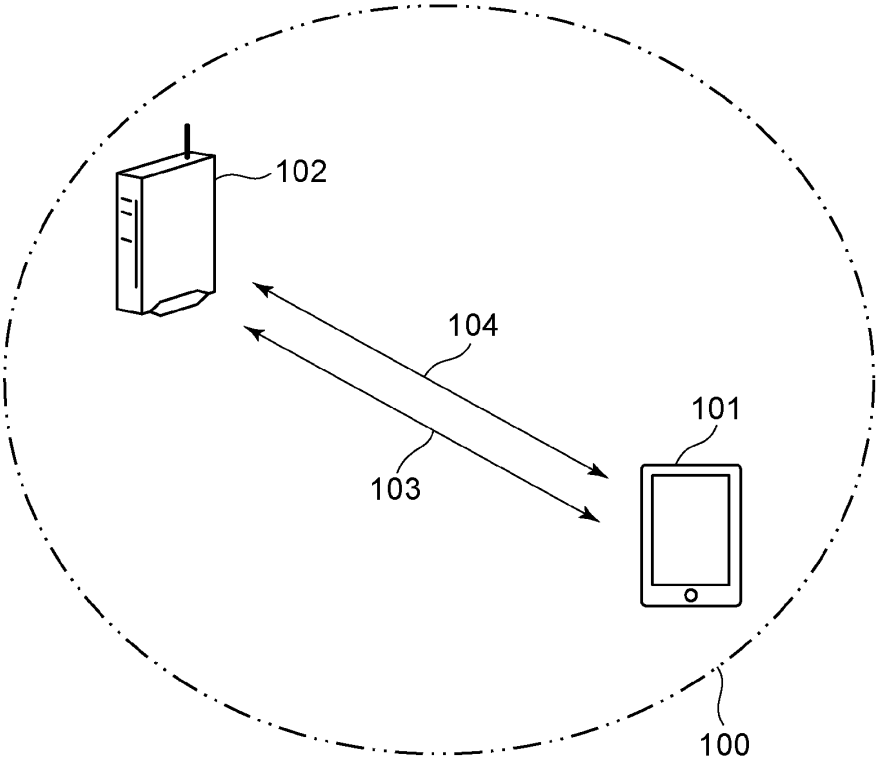
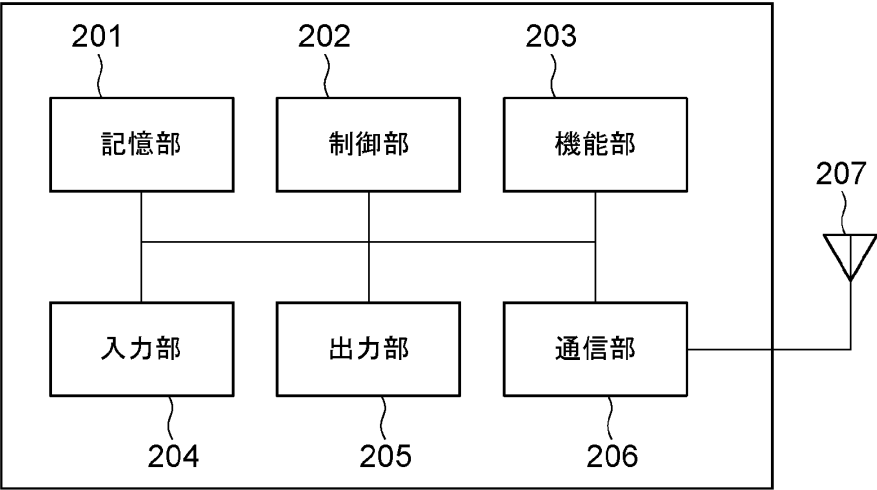


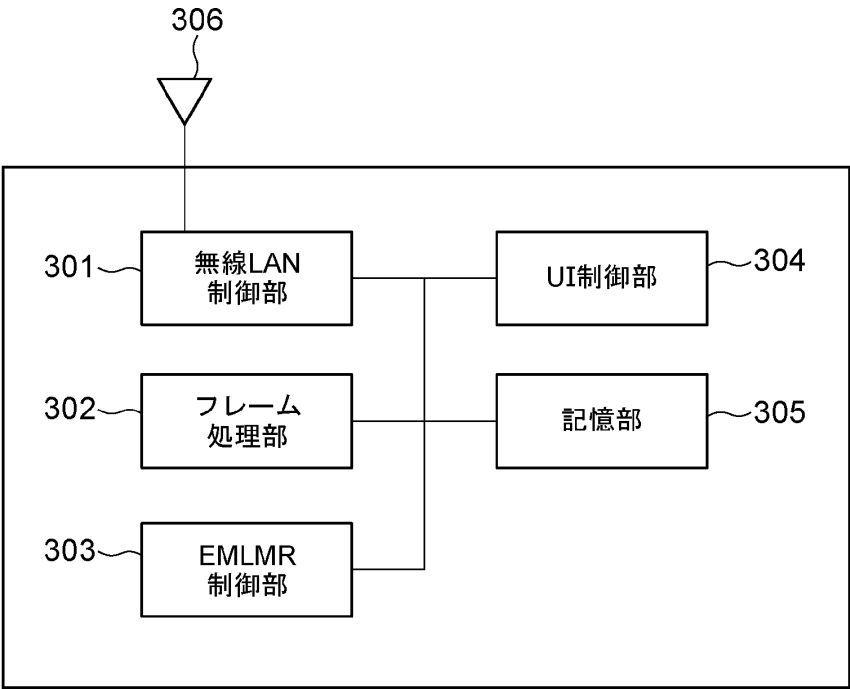
[図1]



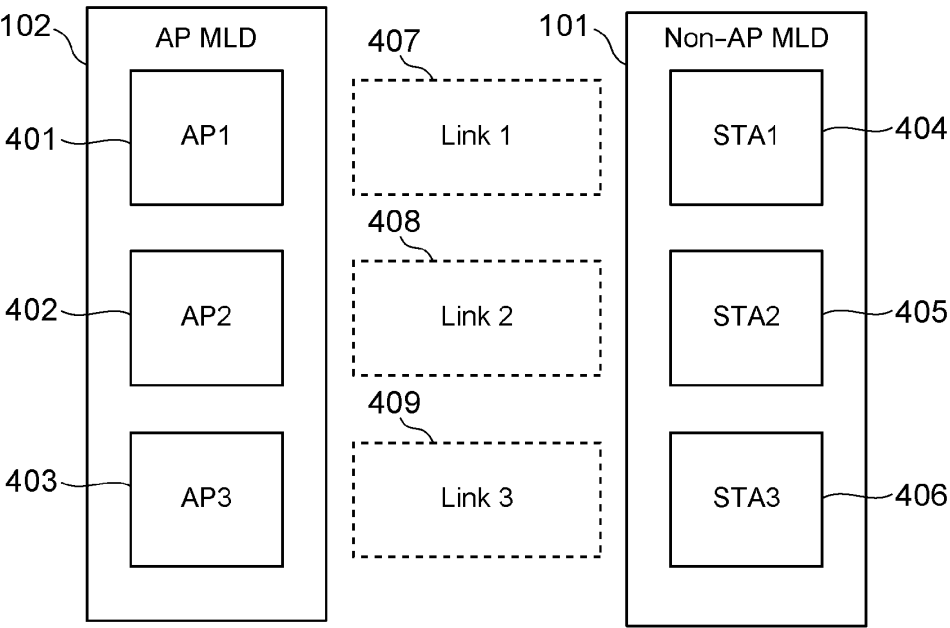
[図2]



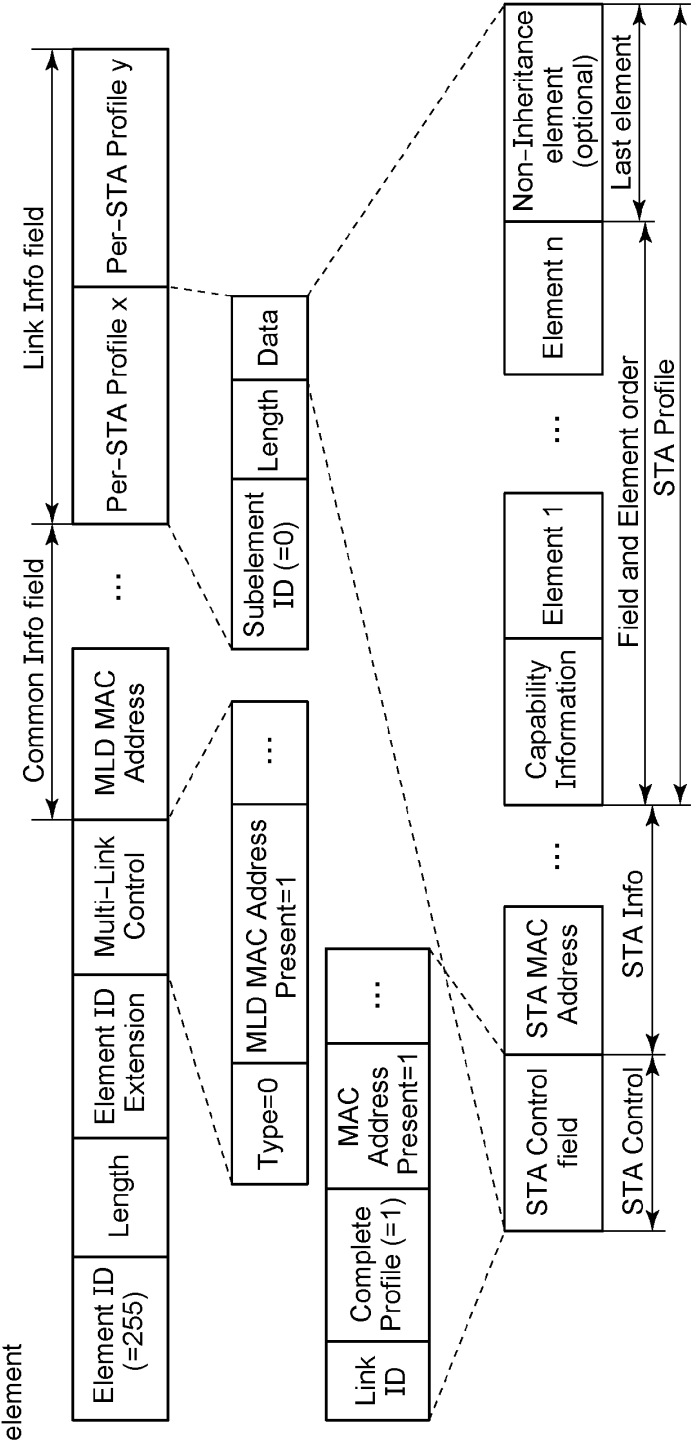
[図3]



[図4]



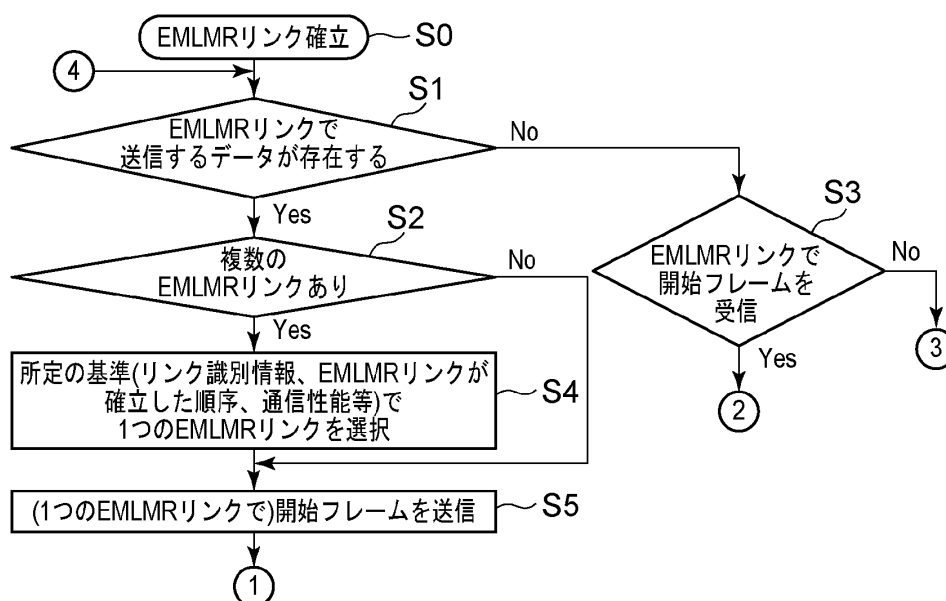
[図5A]



[図5B]

	B0	B1	B3	B4	B5	B7	B8	B11	B12	B13	B14	B15	B16	B39/63/87
	EMLSR Support	EMLSR Delay	EMLMR Support	EMLMR Delay	Transition Timeout	MCS Map Count	Reserved	EMLMR Supported MCS And NSS Set						
Bits:	1	3	1	3	4	2	2	Variable						

[図6A]



[図6B]

