

SPECIFICATION

Switchable signal compressor/signal expander

5 The present invention relates to a noise reduction system which is provided with a signal compressor and a signal expander. 5

It has previously been known that, in order to improve the signal-to-noise ratio of a certain specified communication system or specified recording and playing system, a noise reduction system provided with a signal compressor and a signal expander is employed for the specified 10 system. 10

In particular, a noise reduction system which shares circuit constituent parts of the signal compressor and those of the signal expander and which can switch the function of the signal compressor and that of the signal expander through the change-over of a mode switch has been proposed in "The Journal of the Society of Electronic and Radio Technicians" (hereinafter referred to as the SERT Journal), Vol. 8, May/June 1974. 15

Fig. 1 of the accompanying drawings shows a block circuit diagram of the SERT Journal switchable signal compressor/signal expander. The switchable signal compressor/signal expander of this type is well known to those skilled in the art as the "Dolby B-type Noise Reduction System" (the word "Dolby" is a Registered Trademark of Dolby Laboratories). 20

When switched to the signal compressor, the "Dolby" B-type noise reduction system serves as an encoder. The signal compressor (encoder) compresses the dynamic range of input signals before the input signals are recorded on a recording tape. When switched to the signal expander, this system serves as a decoder. The signal expander (decoder) restores the linearity of the dynamic range for the input signals. Noise to be introduced in the recording/playing 25 process are considerably reduced, so that the combination of the signal compressor and the signal expander functions as the noise reduction system. 25

In the "Dolby" B-type reduction system, the operations of signal compression/signal expansion are performed usually for signal components which are higher than a frequency value of 200 Hz.

30 Referring to Fig. 1, the well-known encoder/decoder will now be described in greater detail. 30

The noise reduction system shown in Fig. 1 has a main channel z_m which extends between an input terminal T_1 and an output terminal T_2 , and a side channel z_s which extends between a mode switch SW for the encoder/decoder switching and the output terminal T_2 .

The main channel z_m includes a combining network 10 and an inverter 11 connected in series 35 between the terminals T_1 and T_2 . 35

The side channel includes a variable filter 12, a signal amplifier 13, a control amplifier 14, a rectifier and integrator circuit 15, and an overshoot suppressor 16.

In the case where the mode switch SW is connected to a terminal T_3 , this circuit arrangement serves as the encoder. The combining network 10 and the inverter 11 in the main path z_m 40 execute the linear amplification. 40

In response to a control signal S_c generated by the rectifier and integrator circuit 15, the variable filter 12 changes the quantity of transfer for a signal component having a frequency above 200 Hz. More specifically, when the level of an input signal at a common terminal T_s of the mode switch SW has fallen, the quantity of transfer from the variable filter 12 increases 45 owing to a feedback loop which consists of the variable filter 12, the signal amplifier 13, the control amplifier 14 and the rectifier and integrator circuit 15. With the falling of the level of the input signal therefore, the signal component at the frequency above 200 Hz, present in the side channel z_s , increases. 45

In the case where the circuit blocks are arranged into the encoder, the signal on the side channel z_s is added to the signal in the main channel z_m . As shown in the amplitude-frequency characteristics of Fig. 2 of the accompanying drawings, signal components above 200 Hz gradually have greater values of amplitude as the signal levels decrease down to -40dB as shown in Fig. 2. 50

On the other hand, in the case where the mode switch SW is connected to a terminal T_4 , the circuit blocks constitute the decoder. The inverter 11 in the main channel z_m is constructed as a signal inverter, and an output signal from the inverter 11 is applied to the common terminal T_s of the mode switch SW, so that the side channel z_s is supplied with the signal having a phase opposite to that of an input signal applied to the input terminal T_1 . Accordingly, the signal on the side channel z_s is subtracted from the signal on the main channel z_m . In the amplitude-frequency characteristics of output signals from the decoder, therefore, the signal components 60 above 200 Hz gradually have smaller values of amplitude as the signal levels decrease. 60

The overshoot suppressor 16 limits the amplitude value of the terminal voltage which is to be applied to the variable filter 12. Unless the overshoot suppressor 16 is present in the circuit, an undesired change will develop in a transient signal of high level.

65 We have found that the above described known switchable signal compressor/expander 65

involves a great deviation in the detection characteristic of the rectifier and integrator circuit 15 arranged in the side channel. This disadvantage is even more evident in the case where the output terminal of the signal amplifier 13 and the input terminal of the control amplifier 14 are D.C.-coupled. In a monolithic semiconductor integrated circuit, a decrease in the number of terminals is required in order to reduce the cost, and hence, the D.C. coupling between circuits is essential. However, it is essential that even with such D.C. coupling, various circuit characteristics do not depart from permissible ranges with respect to desired design values.

We have noted that the disadvantage of the prior constructions is due to the fact that, on account of the cascade connection of the signal amplifier 13 and the control amplifier 14, a D.C. offset voltage at the output terminal of the signal amplifier 13 and a D.C. offset voltage at the input terminal of the control amplifier 14 afford an undesirable deviation in the operating point of the rectifier and integrator circuit 15.

It is an object of the present invention to provide a switchable signal compressor/signal expander whose circuit characteristics do not substantially depart from the desired design values thereof on account of the D.C. coupling between circuits.

It is a further object of the present invention to provide a switchable signal compressor/signal expander whose detection characteristic has only a small deviation.

According to the present invention there is provided a switchable signal compressor/signal expander including: a combining network and an inverter which are arranged in a main channel extending between an input terminal and an output terminal; a variable filter and a signal amplifier which are arranged in a side channel coupled to said combining network; a control amplifier and a rectifier and integrator circuit which are arranged so as to control a quantity of transfer of said variable filter; and a mode switch (SW) which serves to feed said side channel with either an input signal of said combining network or an output signal of said inverter; wherein means are provided for preventing a substantial deviation in the detection characteristic of the rectifier and integrator circuit.

The present invention will now be described in greater detail by way of example with reference to the remaining figures of the accompanying drawings, wherein:

Figure 3 is a circuit diagram partly in block form of a first embodiment of a switchable signal compressor/signal expander;

Figure 4 is a circuit diagram partly in block form of a second embodiment of a switchable signal compressor/signal expander; and

Figure 5 is a circuit diagram partly in block form of a modified embodiment of a switchable signal compressor/signal expander.

Referring first to Fig. 3, it should be noted that components within broken lines IC are formed as a monolithic semiconductor integrated circuit. Numerals enclosed with circles indicate terminal numbers of the integrated circuit.

A combining network 10 and an inverter 11 are arranged in a main channel z_m which extends between an input terminal T_1 and an output terminal T_2 . The input terminal T_1 is connected to terminal 1 of the integrated circuit through an input coupling capacitor C_1 . An input amplifier 20 is formed as an operational amplifier, and has a non-inverting input terminal (+), an inverting input terminal (-) and an output terminal. The non-inverting input terminal (+) is connected to the terminal 1. The output terminal of this amplifier is connected to a terminal T_3 of a mode switch SW outside the integrated circuit through terminal 3 of the integrated circuit, and is also connected to the main channel z_m . A negative feedback network 21 consisting of resistors R_1 and R_2 is connected between the output terminal and the inverting input terminal (-) of the input amplifier 20, whereby the voltage gain of this input amplifier 20 is set.

One end of the resistor R_2 of the negative feedback network 21 is earthed A.C.-wise by a capacitor C_3 through a terminal 4 of the integrated circuit. A reference voltage generator 22 feeds the terminal 4 with a D.C. reference voltage V_{REF} which is set at a level equal to about one half of a supply voltage V_{CC} . A resistor R_{100} is connected between the terminals 1 and 4, whereby the D.C. reference voltage V_{REF} is fed to the terminal 1. Accordingly, the D.C. potential of the output terminal of the input amplifier 20 is at a level approximately equal to the D.C. reference voltage V_{REF} .

On the side channel z_s extending between the mode switch SW and the output terminal T_2 , there are arranged a variable filter 12, a signal amplifier 13, a control amplifier 14, a rectifier and integrator circuit 15 and an overshoot suppressor 16. One input terminal of the signal amplifier 13 and one input terminal of the control amplifier 14 are connected to the variable filter 12.

The variable filter 12 consists of capacitors C_4 and C_5 , resistors R_{101} and R_{102} and a variable impedance 23.

The mode switch SW is connected to terminal 5 of the integrated circuit through the capacitors C_4 and C_5 . The variable impedance 23 is also connected to the terminal 5.

The signal amplifier 13 is formed as an operational amplifier, and has a non-inverting input terminal (+), an inverting input terminal (-) and an output terminal. The non-inverting input

terminal (+) is connected to terminal 5 and the variable impedance 23. A negative feedback network 24 consisting of resistors R_3 and R_4 is connected between the output terminal and inverting input terminal (-) of the signal amplifier 13, whereby the voltage gain of this signal amplifier 13 is set. An output signal at the output terminal of the signal amplifier 13 is supplied

5 to the overshoot suppressor 16.

The overshoot suppressor 16 consists of a resistor R_5 and clamping diodes D_1 and D_2 , and prevents the occurrence of an undesirable change due to a transient signal of high level.

10 An output signal from the overshoot suppressor 16 is transmitted to the side channel z_s of the combining network 10 through a buffer circuit 25 which is constructed as an emitter follower circuit.

The control amplifier 14 is also formed as an operational amplifier and has a non-inverting input terminal (+), an inverting input terminal (-) and an output terminal. The non-inverting input terminal (+) is connected to terminal 5 and the variable impedance 23. The voltage gain of the control amplifier 14 is set by connecting a negative feedback network 26 which consists

15 of resistors R_6 , R_7 and R_{103} and capacitors C_6 and C_7 . Terminal 6 is provided to connect the resistor R_{103} and the capacitors C_6 and C_7 of the negative feedback network 26 which are outside the semiconductor integrated circuit to the resistors R_6 and R_7 . An output signal of the control amplifier 14 is transmitted to the rectifier and integrator circuit 15.

20 The rectifier and integrator circuit 15 includes a rectifier 15a which consists of a diode D_3 , and also includes an integrator 15b consisting of capacitors C_8 and C_9 , resistors R_{104} and R_{105} and a diode D_4 . The diode D_4 adjusts the so-called attack time and recovery time to appropriate values. Terminals 7 and 8 are provided in order to connect the capacitors C_8 and C_9 and the resistors R_{104} and R_{105} of the integrator 15b which are outside the semiconductor integrated circuit to the diodes D_3 and D_4 . The output voltage of the integrator 15b is transmitted to a

25 voltage-current converter 27.

This voltage-current converter 27 provides at its output a control signal current S_c corresponding to the output voltage of the integrator 15b. The magnitude of the impedance of the variable impedance 23 of the variable filter 12 is controlled in accordance with the magnitude of the control signal current S_c .

30 The variable filter 12, control amplifier 14, rectifier and integrator circuit 15 and voltage-current converter 27 control the magnitude of the impedance of the variable impedance 23 with the falling of a signal level at a common terminal T_s of the mode switch SW. Therefore, the level of a signal component at a frequency of above 200 Hz to be transmitted to the side channel z_s through the signal amplifier 13 and the overshoot suppressor 16 increases.

35 The combining network 10 consists of a resistor R_8 arranged in the main channel z_m and a resistor R_9 arranged in the side channel z_s . A signal which is the added result between a signal component in the main channel z_m and a signal component in the side channel z_s is obtained at the junction between the resistors R_8 and R_9 .

40 The inverter 11 is formed as an operational amplifier, and has a non-inverting input terminal (+), an inverting input terminal (-) and an output terminal. The non-inverting input terminal (+) is connected to the terminal 4, the inverting input terminal (-) is connected to the junction between the resistors R_8 and R_9 , and the output terminal is connected to the terminal 2. By properly setting the value of the resistance of a resistor R_{10} connected between the output terminal and inverting input terminal (-) of the inverter 11 and the values of resistance of the

45 resistors R_8 and R_9 , it is possible to set the level of an output signal of the switchable signal compressor/signal expander, which signal is output from the terminal 2.

In the case where the mode switch SW is connected to the terminal T_3 , an output signal of the input amplifier 20 in the main channel z_m is transmitted to the common terminal T_s of the switch. In this case, the signal component in the main channel z_m and the signal component in the side channel z_s are added, so that the circuit blocks operate as an encoder.

50 On the other hand, in the case where the mode switch SW is connected to the terminal T_4 , the output from the inverter 11 is transmitted to the terminal T_s of the switch. In this case, the signal in the side channel z_s is subtracted from the signal in the main channel z_m , so that the circuit blocks operate as a decoder.

55 Terminal 9 of the integrated circuit is connected to a controller 28. When the terminal 9 is connected to earth by means of a switch X, the controller 28 stops the operation of the voltage-current converter 27 through appropriate means (not shown). Terminal 10 of the integrated circuit is a supply voltage-feeding terminal, and terminal 11 is an earthed terminal.

60 It should be noted that the non-inverting input terminal (+) of the control amplifier 14 in the side channel z_s is not D.C.-coupled to the output terminal of the signal amplifier 13 but is connected to the variable impedance 23 within the variable filter 12. This variable 23 is supplied with the reference voltage V_{REF} from the reference voltage generator 22 through the resistors R_{101} and R_{102} of the variable filter 12. The input impedance at the non-inverting input terminal (+) and the input impedance at the inverting input terminal (-) of the control

65 amplifier 14 are both very high and the D.C. negative feedback is performed 100% from the

output terminal to the inverting input terminal thereof through the negative feedback network 26, so that the respective D.C. potentials of the non-inverting input terminal (+), inverting input terminal (-) and output terminal of the control amplifier 14 are set at levels approximately equal to the reference voltage V_{REF} . Accordingly, the operating point of the rectifier 15a is set to a potential the level of which is approximately equal to the reference voltage V_{REF} .

If the non-inverting input terminal (+) of the control amplifier 14 is D.C.-coupled to the output terminal of the signal amplifier 13 in accordance with the known circuit shown in Fig. 1, the operating point of the rectifier 15a has a great deviation, with the result that the transfer characteristic of the side channel z_s also has a great deviation. More specifically, even when the input impedances at the non-inverting input terminal (+) and inverting input terminal (-) of the signal amplifier 13 are very high, D.C. input currents $i_{(+)\text{IN}}$ and $i_{(-)\text{IN}}$ which are not negligible flow into the non-inverting input terminal (+) and the inverting input terminal (-) respectively. Accordingly, in such a case a D.C. voltage V_o at the output terminal of the signal amplifier 13 departs from the reference voltage V_{REF} as indicated by the following equation assuming that the D.C. offset current $i_{(-)\text{IN}}$ flowing into the inverting input terminal (-) is sufficiently smaller than a D.C. current i_i flowing through the resistors R_3 and R_4 .

$$V_o = V_{REF} - \frac{(R_3 + R_4)}{R_4} \cdot (R_{101} + R_{102}) \cdot i_{(+)\text{IN}} = V_{REF} - V_{\text{off}} \quad (1)$$

Accordingly, the D.C. offset voltage V_{off} of the output voltage V_o of the signal amplifier 13 has a great deviation dependent upon the values of resistance of the resistors R_3 , R_4 , R_{101} and R_{102} and the D.C. input current $i_{(+)\text{IN}}$. Furthermore, this D.C. offset voltage V_{off} also has a deviation dependent upon the voltage-current characteristics of the clamping diodes D_1 and D_2 of the overshoot suppressor 16.

In contrast, in the circuit arrangement shown in Fig. 3, the non-inverting input terminal (+) of the control amplifier 14 is not affected by the output voltage of the signal amplifier 13 having the D.C. offset voltage V_{off} of such a great deviation.

It should be further noted that, since the D.C. blocking capacitor C_6 is arranged in the negative feedback network 26 of the control amplifier 14, no D.C. current flows through the resistor R_7 of the negative feedback network 26.

Consequently, D.C. input currents $i'_{(+)\text{IN}}$ and $i'_{(-)\text{IN}}$ which flow into the non-inverting input terminal (+) and inverting input terminal (-) of the control amplifier 14 respectively and a voltage V_o' at the output terminal thereof are given by the following equation, and the output voltage V_o' of the control amplifier 14 has only a very small D.C. offset voltage V'_{off} .

$$V_o' = V_{REF} - (R_{101} + R_{102}) \cdot i'_{(+)\text{IN}} + R_8 \cdot i'_{(-)\text{IN}} = V_{REF} - V'_{\text{off}} \quad (2)$$

As a result, the D.C. offset voltage V'_{off} which is developed at the output of the control amplifier 14 can be handled by the rectifier 15a in the circuit arrangement shown in Fig. 3.

In the known circuit shown in Fig. 1, the signal on the side channel z_s is amplified by the signal amplifier 13 and the control amplifier 14 and then transmitted to the rectifier 15a, whereas in the circuit shown in Fig. 3, the signal on the side channel z_s is amplified by only the control amplifier 14 and then transmitted to the rectifier 15a. Accordingly, the ratio between the values of resistance of the resistors R_6 and R_7 of the negative feedback network of the control amplifier 14 must be set at a value of resistance greater than in the known circuit arrangement shown in Fig. 1.

As shown in Fig. 3, the D.C. reference voltage V_{REF} to be generated by the reference voltage generator 22 is set at a level equal to about one half of the supply voltage V_{CC} , whereby the respective output D.C. levels of the signal amplifier 13, control amplifier 14, input amplifier 20 and inverter 11 can be maintained at levels equal to about one half of the supply voltage V_{CC} , and hence, the dynamic ranges of the respective outputs can have large values.

In a modified form, in order to set the Dolby Level at a predetermined value, a method can be used in which, in setting each of the values of resistance of the resistors R_1 to R_{10} within the monolithic semiconductor integrated circuit, a resistor of the most appropriate value of resistance is selectively connected from among a plurality of resistors by the use of the master slice of an aluminium interconnection.

Referring now to Fig. 4, it should be noted that components with broken lines IC are formed as a monolithic semiconductor integrated circuit. Numerals enclosed with circles indicate terminal numbers of the integrated circuit.

A combining network 10 and an inverter 11 are arranged in a main channel z_m which extends between an input terminal T_1 and an output terminal T_2 . The input terminal T_1 is connected to terminal 1 of the integrated circuit through an input coupling capacitor C_1 . An input amplifier 20

is formed as an operational amplifier, and has a non-inverting input terminal (+), an inverting input terminal (-) and an output terminal. The non-inverting input terminal (+) is connected to the terminal 1. The output terminal of this amplifier is connected to a terminal T_3 of a mode switch SW outside the integrated circuit through terminal 3 of the integrated circuit, and is also connected to the main channel z_m . A negative feedback network 21 consisting of resistors R_1 and R_2 is connected between the output terminal and the inverting input terminal (-) of the input amplifier 20, whereby the voltage gain of this input amplifier 20 is set.

One end of the resistor R_2 of the negative feedback network 21 is earthed A.C.-wise by a capacitor C_3 through a terminal 4 of the integrated circuit. A reference voltage generator 22 feeds the terminal 4 with a D.C. reference voltage V_{REF} . A resistor R_{100} is connected between the terminals 1 and 4, whereby the D.C. reference voltage V_{REF} is fed to the terminal 1. Accordingly, the D.C. potential of the output terminal of the input amplifier 20 is at a level approximately equal to the D.C. reference voltage V_{REF} .

On a side channel z_s extending between the mode switch SW and the output terminal T_2 , there are arranged a variable filter 12, a signal amplifier 13, a control amplifier 14, a rectifier and integrator circuit 15 and an overshoot suppressor 16.

The variable filter 12 consists of capacitors C_4 and C_5 , resistors R_{101} and R_{102} and a variable impedance 23.

The mode switch SW is connected to terminal 5 of the integrated circuit through the capacitors C_4 and C_5 . The variable impedance 23 is also connected to the terminal 5.

The signal amplifier 13 is formed as an operational amplifier, and has a non-inverting input terminal (+), an inverting input terminal (-) and an output terminal. The non-inverting input terminal (+) is connected to terminal 5 and the variable impedance 23. A negative feedback network 24 consisting of resistors R_3 and R_4 is connected between the output terminal and inverting input terminal (-) of the signal amplifier 13, whereby the voltage gain of this signal amplifier 13 is set. An output signal at the output terminal of the signal amplifier 13 is supplied to the overshoot suppressor 16.

The overshoot suppressor 16 consists of a resistor R_5 and clamping diodes D_1 and D_2 , and prevents the occurrence of an undesirable change due to a transient signal of high level.

An output signal from the overshoot suppressor 16 is transmitted to the side channel z_s of the combining network 10 through buffer circuit 25 which is constructed as an emitter follower circuit.

The control amplifier 14 is also formed as an operational amplifier and has a non-inverting input terminal (+), an inverting input terminal (-) and an output terminal. The non-inverting input terminal (+) of this amplifier is connected to the output terminal of the signal amplifier 13. The voltage gain of the control amplifier 14 is set by connecting a negative feedback network 26 which consists of resistors R_6 , R_7 and R_{103} and capacitors C_6 and C_7 . Terminal 6 is provided to connect the resistor R_{103} and the capacitors C_6 and C_7 of the negative feedback network 26 which are outside the semiconductor integrated circuit to the resistors R_6 and R_7 . An output signal of the control amplifier 14 is transmitted to the rectifier and integrator circuit 15.

The rectifier and integrator circuit 15 includes a rectifier 15a which consists of a diode D_3 , and also includes an integrator 15b consisting of capacitors C_8 and C_9 , resistors R_{104} and R_{105} and a diode D_4 . The diode D_4 adjusts the so-called attack time and recovery time to appropriate values. Terminals 7 and 8 are provided in order to connect the capacitors C_8 and C_9 and the resistors R_{104} and R_{105} of the integrator 15b which are outside the semiconductor integrated circuit to the diodes D_3 and D_4 . The output voltage of the integrator 15b is transmitted to a voltage-current converter 27.

This voltage-current converter 27 provides at its output a control signal current S_c corresponding to the output voltage of the integrator 15b. The magnitude of the impedance of the variable impedance 23 of the variable filter 12 is controlled in accordance with the magnitude of the control signal current S_c .

The variable filter 12, control amplifier 14, rectifier and integrator circuit 15 and voltage-current converter 27 control the magnitude of the impedance value of the variable impedance 23 with the falling of a signal level at a common terminal T_5 of the mode switch SW. Therefore, the level of a signal component at a frequency of above 200 Hz to be transmitted to the side channel z_s through the signal amplifier 13 and the overshoot suppressor 16 increases.

The combining network 10 consists of a resistor R_8 arranged in the main channel z_m and a resistor R_9 arranged in the side channel z_s . A signal which is the added result between a signal component in the main channel z_m and a signal component in the side channel z_s is obtained at the junction between the resistors R_8 and R_9 .

The inverter 11 is formed as an operational amplifier and as a non-inverting input terminal (+), an inverting terminal (-) and an output terminal. The non-inverting input terminal (+) is connected to the terminal 4, the inverting input terminal (-) is connected to the junction between the resistors R_8 and R_9 , and the output terminal is connected to the terminal 2. By properly setting the value of the resistance of a resistor R_{10} connected between the output

terminal and inverting input terminal (-) of the inverter 11 and the values of resistance of the resistors R_8 and R_9 , it is possible to set the level of an output signal of the switchable signal compressor/signal expander, which signal is output from the terminal 2.

In the case where the mode switch SW is connected to the terminal T_3 , an output signal of the input amplifier 20 in the main channel z_m is transmitted to the common terminal T_5 of the switch. In this case, the signal component in the main channel z_m and the signal component in the side channel z_s are added, so that the circuit blocks operate as an encoder.

On the other hand, in the case where the mode switch SW is connected to the terminal T_4 , the output terminal of the inverter 11 is transmitted to the common terminal T_5 of the switch. In this case, the signal in the side channel z_s is subtracted from the signal in the main channel z_m , so that the circuit blocks operate as a decoder.

Terminal 9 of the integrated circuit is connected to a controller 28. When the terminal 9 is connected to earth by means of a switch χ , the controller 28 stops the operation of the voltage-current converter 27 through appropriate means (not shown). Terminal 10 of the integrated circuit is a supply voltage-feeding terminal, and terminal 11 is an earthed terminal.

The reference voltage generator 22 supplies the D.C. reference voltage V_{REF} to the respective non-inverting input terminals (+) of the input amplifier 20, inverter 11 and signal amplifier 13, in order to maintain D.C. voltages at the output terminals of the respective amplifiers at levels approximately equal to this D.C. reference voltage. Since the output voltage of the signal amplifier 13 is supplied to the non-inverting input terminal (+) of the control amplifier 14, the output D.C. level of the control amplifier 14 is also maintained at a level which is approximately equal to the D.C. reference voltage.

In order to set the dynamic ranges of the output voltages of the respective amplifiers 20, 11, 13 and 14 to be high, the D.C. reference voltage V_{REF} is set at a level equal to about one half of the supply voltage V_{CC} fed to the terminal 10.

Accordingly, even when the magnitude of the supply voltage V_{CC} fed to the terminal 10 fluctuates, the reference voltage generator 22 generates the D.C. reference voltage V_{REF} of a level which is about one half of the supply voltage V_{CC} against the fluctuations.

As a result, the D.C. reference voltage V_{REF} to be produced from the reference voltage generator 22 fluctuates in correspondence with the fluctuation of the supply voltage V_{CC} . A disadvantage of the known circuit shown in Fig. 1 is that as a result of such fluctuation of the D.C. reference voltage V_{REF} , a charging current or discharging current flows through the rectifier and integrator to make the detection characteristic fluctuate undesirably.

In order to eliminate the above referred to disadvantage in the circuit shown in Fig. 4, the other ends of the capacitors C_8 and C_9 of the integrator 15b are not D.C.-earthed but are connected to terminal 4 so as to be supplied with the D.C. reference voltage V_{REF} produced from the reference voltage generator 22.

Furthermore, the other ends of the capacitor C_7 and the resistor R_{103} of the negative feedback network 26 of the control amplifier 14 are not D.C.-earthed, but are likewise connected to the terminal 4 so as to be supplied with the D.C. reference voltage V_{REF} produced from the reference voltage generator 22.

Thus, even when the D.C. reference voltage V_{REF} produced from the reference voltage generator 22 fluctuates, no charging current or discharging current flows through the capacitors C_8 and C_7 of the negative feedback network 26 of the control amplifier 14 or the capacitors C_8 and C_9 of the integrator 15b, and undesirable fluctuations of the detection characteristic can be prevented.

Referring lastly to the modified circuit shown in Fig. 5, which is similar to the first embodiment shown in Fig. 3 with regard to the arrangement of the signal amplifier 13 and control amplifier 14, the non-inverting input terminal (+) of the control amplifier 14 in the side channel z_s is not D.C.-coupled to the output terminal of the signal amplifier 13 but is connected to the variable impedance 23 within the variable filter 12.

Furthermore, it should be noted that in the circuit of Fig. 5, as in the embodiment shown in Fig. 4, the other ends of the capacitors C_8 and C_9 as well as the other ends of the capacitor C_7 and the resistor R_{103} of the negative feedback network 26 of the control amplifier 14 are not D.C.-earthed but connected to the terminal 1.

Alternatively, it would be possible to connect the other ends of the capacitor C_7 and the resistor R_{103} of the negative feedback circuit 26 as well as the other ends of the capacitors C_8 and C_9 to the terminal 4 as in the embodiment of Fig. 4. It will be appreciated that in this modified form the circuit would combine the principal advantages of both the first and second embodiments shown in Figs. 3 and 4 respectively.

CLAIMS

1. A switchable signal compressor/signal expander including: a combining network and an inverter which are arranged in a main channel extending between an input terminal and an output terminal; a variable filter and a signal amplifier which are arranged in a side channel



terminal and inverting input terminal (-) of the inverter 11 and the values of resistance of the resistors R_8 and R_9 , it is possible to set the level of an output signal of the switchable signal compressor/signal expander, which signal is output from the terminal 2.

In the case where the mode switch SW is connected to the terminal T_3 , an output signal of the input amplifier 20 in the main channel z_m is transmitted to the common terminal T_5 of the switch. In this case, the signal component in the main channel z_m and the signal component in the side channel z_s are added, so that the circuit blocks operate as an encoder.

On the other hand, in the case where the mode switch SW is connected to the terminal T_4 , the output terminal of the inverter 11 is transmitted to the common terminal T_5 of the switch. In this case, the signal in the side channel z_s is subtracted from the signal in the main channel z_m , so that the circuit blocks operate as a decoder.

Terminal 9 of the integrated circuit is connected to a controller 28. When the terminal 9 is connected to earth by means of a switch X, the controller 28 stops the operation of the voltage-current converter 27 through appropriate means (not shown). Terminal 10 of the integrated circuit is a supply voltage-feeding terminal, and terminal 11 is an earthed terminal.

The reference voltage generator 22 supplies the D.C. reference voltage V_{REF} to the respective non-inverting input terminals (+) of the input amplifier 20, inverter 11 and signal amplifier 13, in order to maintain D.C. voltages at the output terminals of the respective amplifiers at levels approximately equal to this D.C. reference voltage. Since the output voltage of the signal amplifier 13 is supplied to the non-inverting input terminal (+) of the control amplifier 14, the output D.C. level of the control amplifier 14 is also maintained at a level which is approximately equal to the D.C. reference voltage.

In order to set the dynamic ranges of the output voltages of the respective amplifiers 20, 11, 13 and 14 to be high, the D.C. reference voltage V_{REF} is set at a level equal to about one half of the supply voltage V_{CC} fed to the terminal 10.

Accordingly, even when the magnitude of the supply voltage V_{CC} fed to the terminal 10 fluctuates, the reference voltage generator 22 generates the D.C. reference voltage V_{REF} of a level which is about one half of the supply voltage V_{CC} against the fluctuations.

As a result, the D.C. reference voltage V_{REF} to be produced from the reference voltage generator 22 fluctuates in correspondence with the fluctuation of the supply voltage V_{CC} . A disadvantage of the known circuit shown in Fig. 1 is that as a result of such fluctuation of the D.C. reference voltage V_{REF} , a charging current or discharging current flows through the rectifier and integrator to make the detection characteristic fluctuate undesirably.

In order to eliminate the above referred to disadvantage in the circuit shown in Fig. 4, the other ends of the capacitors C_8 and C_9 of the integrator 15b are not D.C.-earthed but are connected to terminal 4 so as to be supplied with the D.C. reference voltage V_{REF} produced from the reference voltage generator 22.

Furthermore, the other ends of the capacitor C_7 and the resistor R_{103} of the negative feedback network 26 of the control amplifier 14 are not D.C.-earthed, but are likewise connected to the terminal 4 so as to be supplied with the D.C. reference voltage V_{REF} produced from the reference voltage generator 22.

Thus, even when the D.C. reference voltage V_{REF} produced from the reference voltage generator 22 fluctuates, no charging current or discharging current flows through the capacitors C_8 and C_7 of the negative feedback network 26 of the control amplifier 14 or the capacitors C_8 and C_9 of the integrator 15b, and undesirable fluctuations of the detection characteristic can be prevented.

Referring lastly to the modified circuit shown in Fig. 5, which is similar to the first embodiment shown in Fig. 3 with regard to the arrangement of the signal amplifier 13 and control amplifier 14, the non-inverting input terminal (+) of the control amplifier 14 in the side channel z_s is not D.C.-coupled to the output terminal of the signal amplifier 13 but is connected to the variable impedance 23 within the variable filter 12.

Furthermore, it should be noted that in the circuit of Fig. 5, as in the embodiment shown in Fig. 4, the other ends of the capacitors C_8 and C_9 as well as the other ends of the capacitor C_7 and the resistor R_{103} of the negative feedback network 26 of the control amplifier 14 are not D.C.-earthed but connected to the terminal 1.

Alternatively, it would be possible to connect the other ends of the capacitor C_7 and the resistor R_{103} of the negative feedback circuit 26 as well as the other ends of the capacitors C_8 and C_9 to the terminal 4 as in the embodiment of Fig. 4. It will be appreciated that in this modified form the circuit would combine the principal advantages of both the first and second embodiments shown in Figs. 3 and 4 respectively.

CLAIMS

1. A switchable signal compressor/signal expander including: a combining network and an inverter which are arranged in a main channel extending between an input terminal and an output terminal; a variable filter and a signal amplifier which are arranged in a side channel

- coupled to said combining network; a control amplifier and a rectifier and integrator circuit which are arranged so as to control a quantity of transfer of said variable filter; and a mode switch (SW) which serves to feed said side channel with either an input signal of said combining network or an output signal of said inverter; wherein means are provided for preventing a substantial deviation in the detection characteristic of the rectifier and integrator circuit. 5
2. A switchable signal compressor/signal expander according to Claim 1, wherein said deviation preventing means comprises a connection between an input terminal of said control amplifier and said variable filter without passing through said signal amplifier. 5
3. A switchable signal compressor/signal expander according to Claim 2, wherein both the signal amplifier and the control amplifier are formed as operational amplifiers, and the non-inverting input terminals of both amplifiers are connected to said variable filter. 10
4. A switchable signal compressor/signal expander according to Claim 2, wherein at least a variable impedance of said variable filter, said signal amplifier, and said control amplifier are formed within a monolithic semiconductor integrated circuit. 10
5. A switchable signal compressor expander/signal according to any one of the preceding claims 2 to 4, wherein a first negative feedback network is connected between the output terminal and the inverting input terminal of said signal amplifier, and a second negative feedback network is connected between the output terminal and the inverting input terminal of said control amplifier. 15
6. A switchable signal compressor/signal expander according to Claim 5, wherein said first negative feedback network includes a first resistor which is connected between said output terminal and said inverting input terminal of said signal amplifier, and a second resistor one end of which is connected to said inverting input terminal of said signal amplifier and the other end of which is connected to a predetermined operating potential, and wherein said second negative feedback network includes a third resistor which is connected between said output terminal and said inverting input terminal of said control amplifier, and a fourth resistor one end of which is connected to said inverting input terminal of said control amplifier and the other end of which is connected to a predetermined operating potential through a D.C. blocking capacitor. 20
7. A switchable signal compressor/signal expander according to Claim 6, wherein a reference voltage generator for producing a D.C. reference voltage is included within said monolithic semiconductor integrated circuit, and said D.C. reference voltage is fed to said non-inverting input terminal of said signal amplifier and said non-inverting input terminal of said control amplifier and is also fed to the other end of said second resistor of said first negative feedback network. 25
8. A switchable signal compressor/signal expander according to any one of the preceding claims, wherein an output signal of said signal amplifier is transmitted from said side channel to said combining network through an overshoot suppressor. 30
9. A switchable signal compressor/signal expander according to Claim 1, wherein said deviation preventing means comprises means for supplying a D.C. reference voltage to both the control amplifier and the rectifier and integrator circuit, so that fluctuations in the detection characteristic of the rectifier and integrator circuit is reduced. 35
10. A switchable signal compressor/signal expander according to Claim 9, wherein said rectifier and integrator circuit comprises a rectifier element, a first resistor, a second resistor, a first capacitor and a second capacitor; one end of said rectifier element being connected to an output terminal of said control amplifier; one end of the first resistor, the first capacitor and the second resistor being connected to the other end of said rectifier element; the other end of said second resistor and one end of said second capacitor being connected in common as an output terminal of said rectifier and integrator circuit; the other end of the first resistor, the first capacitor and the second capacitor being supplied with said D.C. reference voltage. 40
11. A switchable signal compressor/signal expander according to Claim 10, wherein the D.C. output level of the control amplifier is maintained at a level approximately equal to said D.C. reference voltage, which reference voltage is supplied from a reference generator. 45
12. A switchable signal compressor/signal expander according to any one of the preceding Claims 9 to 11, wherein both the signal amplifier and the control amplifier are formed as operational amplifiers. 50
13. A switchable signal compressor/signal expander according to Claim 12, wherein a first negative feedback network is connected between an output terminal and an inverting input terminal of said signal amplifier, wherein a second negative feedback network is connected between said output terminal and an inverting input terminal of said control amplifier, and wherein both a non-inverting input terminal of said signal amplifier and a non-inverting input terminal of said control amplifier are supplied with said D.C. reference voltage. 55
14. A switchable signal compressor/signal expander according to Claim 13, wherein said first negative feedback network includes a third resistor which is connected between said output terminal and said inverting input terminal of said signal amplifier, and a fourth resistor one end of which is connected to said inverting input terminal of said signal amplifier and the other end 60
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of which is supplied with said D.C. reference voltage and wherein said second negative feedback network includes a fifth resistor which is connected between said output terminal and said inverting input terminal of said control amplifier, and a sixth resistor one end of which is connected to said inverting input terminal of said control amplifier and the other end of which is
5 connected to said D.C. reference voltage through a D.C. blocking capacitor.

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15. A switchable signal compressor/signal expander according to any one of the preceding Claims 9 to 14, wherein an output signal of said signal amplifier is transmitted from said side channel to said combining network through an overshoot suppressor.

16. A switchable signal compressor/signal expander constructed substantially as herein
10 described with reference to and as illustrated in Fig. 3, or Fig. 4, or Fig. 5 of the accompanying drawings.

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