Box III TEXT OF THE ABSTRACT (Continuation of item 5 of the first sheet)

The technical features mentioned in the abstract do not include a reference sign between parentheses (PCT Rule 8.1(d)).

Memory access control logic (108) for controlling sequential and toggle mode burst accesses to a memory (109) in a computer system using toggle mode automatic increment logic (201B). The memory access control logic (108) controls the sequence in which locations of a memory are accessed during a memory burst access operation wherein the burst access sequence is determined by an order in which a burst access starting address is incremented. Toggle increment logic (201B) for incrementing a starting address in a toggle sequence is included in the computer system. An input bus (106) receives a burst access request and a burst access starting address indicating a first memory location to be accessed in response to the burst access request from a device in the computer system. Additional logic (117) determines whether the device requires a linear increment sequence or a toggle increment sequence for the burst access. Control logic (213) controls the toggle increment logic (201B) to increment the starting address in a linear sequence in response to determining that the device requires a linear increment sequence.

REPLACEMENT SHEET

02 SEP 1996