METHOD AND STRUCTURE FOR CALIBRATING SCATTEROMETRY-BASED METROLOGY TOOL USED TO MEASURE DIMENSIONS OF FEATURES ON A SEMICONDUCTOR DEVICE

TECHNICAL FIELD

This invention relates generally to semiconductor fabrication technology, and, more particularly, to a method and a structure for calibrating a scatterometry-based metrology tool used to measure dimensions of features on a semiconductor device.

BACKGROUND ART

WO-A-02/13232 discloses a method for measurement of critical dimensions by irradiating a test pattern on a surface of a substrate with X-rays. In one embodiment, a collimator is used to collimate the irradiating beam. The collimator comprises a grating of ridges having a pitch equal to the pitch of ridges in the test pattern. When the X-ray beam from the collimator is incident on the test pattern, interference occurs, and the interference pattern can be measured by a detector whilst the collimator and test pattern are translated relative to each other.

There is a constant drive within the semiconductor industry to increase the operating speed of integrated circuit devices, *e.g.*, microprocessors, memory devices, and the like. This drive is fueled by consumer demands for computers and electronic devices that operate at increasingly greater speeds. This demand for increased speed has resulted in a continual reduction in the size of semiconductor devices, *e.g.*, transistors. That is, many components of a typical field effect transistor (FET), *e.g.*, channel length, junction depths, gate insulation thickness, and the like, are reduced. For example, all other things being equal, the smaller the channel length of the transistor, the faster the transistor will operate. Thus, there is a constant drive to reduce the size, or scale, of the components of a typical transistor to increase the overall speed of the transistor, as well as integrated circuit devices incorporating such transistors.

By way of background, an illustrative field effect transistor 10, as shown in Figure 1, may be formed above a surface 11A of a semiconducting substrate or wafer

11 comprised of doped-silicon. In the process of forming integrated circuit devices, millions of transistors, such as the illustrative transistor 10 depicted in Figure 1, are formed above a semiconducting substrate. The substrate 11 may be doped with either N-type or P-type dopant materials, for example. The transistor 10 may have a doped polycrystalline silicon (polysilicon) gate electrode 14 formed above a gate insulation layer 16. The gate electrode 14 and the gate insulation layer 16 may be separated from doped source/drain regions 22 of the transistor 10 by a dielectric sidewall spacer 20. The source/drain regions 22 for the transistor 10 may be formed by performing one or more ion implantation processes to introduce dopant atoms, *e.g.*, arsenic or phosphorous for NMOS devices, boron for PMOS devices, into the substrate 11. Shallow trench isolation regions 18 may be provided to isolate the transistor 10 electrically from neighboring semiconductor devices, such as other transistors (not shown). Additionally, although not depicted in Figure 1, a typical integrated circuit device is comprised of a plurality of conductive interconnections, such as conductive lines and conductive contacts or vias, positioned in multiple layers of insulating material formed above the substrate. These conductive interconnections allow electrical signals to propagate between the transistors formed above the substrate.

During the course of fabricating such integrated circuit devices, a variety of features, *e.g.*, gate electrodes, conductive lines, openings in layers of insulating material, etc., are formed to very precisely controlled dimensions. Such dimensions are sometimes referred to as the critical dimension (CD) of the feature. It is very important in modern semiconductor processing that features be formed as accurately as possible due to the reduced size of those features in such modern devices. The gate electrode 14 has a critical dimension 12, *ie.*, the width of the gate electrode 14, that approximately corresponds to the channel length 13 of the device when the transistor 10 is operational. Gate electrodes 14 may now be patterned to a width 12 that is approximately 180 nm, and further reductions are planned in the future, *e.g.*, 120 nm. Since the width 12 of the gate electrode 14 corresponds approximately to the channel length 13 of the transistor 10 when it is operational, even slight varia-

tions in the critical dimension 12 of the gate electrode 14 as fabricated may adversely affect device performance. Moreover, at a given level of a wafer, features, *e.g.*, gate electrodes, may be formed to a variety of different critical dimensions. Additionally, gate electrodes and/or shallow trench isolation structures at a given level may have differing critical dimensions.

Given the importance of forming features to very precise dimensions, semiconductor manufacturers typically measure the critical dimension of the resulting features to insure that manufacturing operations are producing features with dimensions that are within a previously determined acceptable range. Scatterometry-based metrology tools may be employed in determining the various dimensions. However, in situations where features having a variety of different critical dimensions must be measured, it is important that the metrology data obtained while measuring these structures be accurate, and that the scatterometry tool can be accurately calibrated as part of the overall metrology process.

The present invention is directed to a method and device that may solve, or at least reduce, some or all of the aforementioned problems.

DISCLOSURE OF INVENTION

The present invention is generally directed to a method and a structure for calibrating a scatterometry-based metrology tool used to measure dimensions of features on semiconductor devices. In one illustrative embodiment, the method comprises measuring a critical dimension of at least one production feature formed above a wafer using a scatterometry tool, measuring at least one of a plurality of grating structures formed above the wafer using the scatterometry tool, each of the grating structures having a different critical dimension, and correcting the measured critical dimension of the at least one production feature based upon the measurement of the at least one grating structure.

In another illustrative embodiment, the method comprises forming a plurality of production features above a wafer, forming a plurality of grating structures above the wafer, each of the grating structures comprised of a plurality of features each having a target critical dimension that thereby defines a critical dimension of the grating structure, each of the grating structures having a different critical dimension, measuring a critical dimension of at least one of the production features using a scatterometry tool, measuring at least one of the grating structures using the scatterometry tool to determine a measured critical dimension of at least one feature of the at least one grating structure, and correcting the measured critical dimension of the at least one production feature based upon a comparison between the measured critical dimension of the at least one feature on the at least one grating structure and the target critical dimension of the feature on the at least one grating structure.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which:

Figure 1 is a cross-sectional view of an illustrative prior art transistor;

Figure 2 is a plan view of an illustrative wafer depicting several production die and a plurality of grating structures formed above said wafer;

Figure 3 is an enlarged view of an illustrative array of grating structures that may be employed with the present invention; and

Figures 4A-4B depict one illustrative embodiment of an illustrative grating structure that may be employed with the present invention.

MODE (S) FOR CARRYING OUT THE INVENTION

Illustrative embodiments of the invention are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual embodiment, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure.

The present invention will now be described with reference to the attached figures. Although the various regions and structures of a semiconductor device are depicted in the drawings as having very precise, sharp configurations and profiles, those skilled in the art recognize that, in reality, these regions and structures are not as precise as indicated in the drawings. Additionally, the relative sizes of the various features and doped regions depicted in the drawings may be exaggerated or reduced as compared to the size of those features or regions on fabricated devices. Nevertheless, the attached drawings are included to describe and explain illustrative examples of the present invention. The words and phrases used herein should be understood and interpreted to have a meaning consistent with the understanding of those words and phrases by those skilled in the relevant art. No special definition of a term or phrase, i.e., a definition that is different from the ordinary and customary meaning as understood by those skilled in the art, is intended to be implied by consistent usage of the term or phrase herein. To the extent that a term or phrase is intended to have a special meaning, i.e., a meaning other than that understood by skilled artisans, such a special definition will be expressly set forth in the specification in a definitional manner that directly and unequivocally provides the special definition for the term or phrase.

In general, the present invention is directed to a method and a structure for calibrating a scatterometry-based metrology tool used to measure dimensions of features on a semiconductor device. As will be readily apparent to those skilled in the art upon a complete reading of the present application, the present method is applicable to obtaining metrology data for a vast variety of different features formed in integrated circuit devices, e.g., the critical dimension of gate electrode structures, the width of shallow trench isolation regions, the width of conductive lines, etc. Thus, the particular feature measured on a semiconductor device should not be considered a limitation of the present invention unless such limitations are expressly set forth in the appended claims.

As shown in Figure 2, a plurality of production die 42 are formed above a wafer 31. The die 42 define an area of the wafer 31 where production integrated circuit devices, e.g, microprocessors, ASICs, memory devices, etc., will be formed. The size, shape and number of die 42 per wafer 31 depend upon the type of device under construction. For example, several hundred die 42 may be formed above an 8-inch (203.2 mm) diameter wafer 31. The production die 42 are separated from each other by scribe lines 42A. After the fabrication processes are completed, the wafer 31 will be cut along the scribe lines 42A, and the production die 42, containing the integrated circuit device formed thereon, will be packaged and sold.

In fabricating integrated circuit devices, many features are formed above the wafer 31. Such features may include, but are not limited to, shallow trench isolation structures (STIs), gate electrode structures, conductive metal or polysilicon lines, etc. Moreover, such features may be formed at various levels of the completed integrated circuit device. For example, shallow trench isolations and gate electrode structures are formed at the lowest level, *i.e.*, the device level, while conductive metal lines may be formed at multiple levels above the wafer 31. Additionally, at each level, the features constructed at that level may have differing critical dimensions, *e.g.*, the critical dimensions of the gate electrode structures may vary, the STI structures may have a different critical dimension than that of the gate electrode structures formed at the same level, etc. For example, at the device level, shallow trench isolations may be formed that have a width of approximately 250 nm, while gate electrode structures formed at that level may have a critical dimension of approximately 180 nm. Moreover, similar type structures, *e.g.*, conductive lines, at a given level may have differing nominal widths due to a variety of factors, such as physical plot space limitations or design choice.

The present invention is generally directed to various methods and structures that may be used to calibrate scatterometry-based metrology tools used to measure the critical dimension of these various features. As a general statement, such methodologies involve the use of an illustrative array 61 (see Figures 2 and 3) comprised of a plurality of grating structures 60A-E formed above the wafer 31. For ease of reference, the grating structures 60A-E may be referred to individually and/or collectively by the reference numeral 60. As will be recognized by those skilled in the art after a complete reading of the present application, the size, shape, number, location and orientation of the grating structures 60 may be varied depending upon the context in which the invention is employed and on the features to be measured. Moreover, although the illustrative grating structures 60A-E are depicted in a linear array, they may be oriented in a different manner, or individually dispersed around the surface of the wafer 31 in a random manner. The grating structures 60 may be formed in the scribe lines 42A of the wafer 31. Lastly, more than one such array 61 may be formed at a given level of the device, and such multiple arrays 61 may be useful in calibrating a scatterometry tool for measuring features having different nominal feature sizes. For example, a first such array may be adapted for calibrating a scatterometry tool for measurements at a first nominal range, *e.g.*, 220-280 nm, while the second such array may be adapted for calibrating such a scatterometry tool to measure dimensions in the range of 110-70 nm.

Figure 3 depicts an illustrative array 61 comprised of the illustrative grating structures 60A-E. Each of the grating structures 60A-E is comprised of a plurality of features 38. The features 38 on each of the grating structures 60A-E have different critical dimensions. As set forth previously, the size, shape, and configuration of the grating structures 60A-E may be varied depending upon the features to be measured using a scatterometry tool. The grating structures 60 may be comprised of any type of features 38, *e.g.*, metal lines, STI structures, gate electrode structures, etc. In the case where it is known that a plurality of features will be formed above the wafer 32 to a nominal critical dimension of 100 nm, the grating structures 60A-E may be comprised of features that have critical dimensions that vary about this nominal value by a known amount, *i.e.*, a fixed offset. For example, in one illustrative embodiment depicted in Figure 3, where the nominal critical dimension of the feature is 100 nm, *e.g.*, gate electrode structures, the array 61 may be comprised of five grating structures 60A-E, each of which is comprised of features having critical dimensions of, respectively, 110 nm, 100 nm, 90 nm, 80 nm and 70 nm. That is, the critical dimension of each grating structure 60A-E is defined by the size of the features 38 that comprise the grating structure 60A-E. The particular size of the critical dimension of the features 38 comprising the grating structure 60A-E and the incremental difference in the critical dimension of the features 38 comprising

the grating structure 60 may vary. In the depicted embodiment in Figure 3, the grating structures 60A-E have a dimensional offset of 10 nm from one grating structure to the next.

One illustrative grating structure 60, depicted in Figures 4A-4B, is comprised of a plurality of gate electrode structures 38A. The gate electrode structures 38A comprising the grating structure 60 have a thickness 65 and sidewalls 62 disposed at an angle 63 (relative to a line normal to the surface 43 of the substrate). The gate electrode structures 38A have a critical dimension 52. The thickness 65, the sidewall angle 63, the pitch 64 of the gate electrode structures 38A, and the critical dimension 52 of the gate electrode structures 38A may be varied as a matter of design choice. The grating structure 60 may be formed in regions having, for example, approximate dimensions of 100 μm x 120 μm, and it may be comprised of approximately 150-200 gate electrode structures 38A (depending upon the selected pitch). Of course, the features that comprise the grating structures 60A-E will vary depending upon the features to be measured.

Each of the grating structures 60A-E, or the array 61 comprising the grating structures 60, may be formed as a separate test structure that is formed in an area defined by a scribe line 42A of a wafer 31. The features that are part of the grating structure 60 may be formed at the same time that other similar features are being formed for production devices formed on the wafer 31. That is, a pattern for the grating structures 60A-E may be formed in a reticle that will be used in the process of forming production integrated circuit devices within the die 42. Alternatively, a separate reticle may be used to form the features that comprise the grating structures 60A-E.

Typically, the critical dimension 52 of the features 38 comprising the various grating structures 60A-E will be such that at least some of the plurality of grating structures 60A-E will be comprised of features 38 having a critical dimension that is comparable to the intended or nominal critical dimension of features to be formed in manufacturing production devices. That is, the group of grating structures 60A-E will provide a range of critical dimensions of features 38 that may be formed on an integrated circuit device, at least for a given type of feature.

In one illustrative embodiment, the array 61 may be comprised of five grating structures 60A-E. In this embodiment, the first of the grating structures, *e.g.*, 60A, may have features 38 that are a fixed increment above a nominal feature size, while the second grating structure 60B is comprised of features 38 at the approximate nominal feature size, and grating structures 60C-D are comprised of features 38 that are successively smaller than the nominal feature size. For example, for a nominal feature size of 250 nm, *e.g.*, for metal lines, the array 61 may be comprised of grating structures 60A-E having feature sizes of, respectively, 260 nm, 250 nm, 240 nm, 230 nm and 220 nm. Of course, this illustrative array pattern may be varied, *e.g.*, the array 61 may be comprised of grating structures 60A-E having feature sizes of, respectively, 280 nm, 275 nm, 250 nm, 235 nm and 220 nm. Thus, the particular pattern or arrangement of the array 61, as well as the incremental difference in the feature sizes of each grating structure 60A-E, may be varied as a matter of design choice.

Through use of the present invention, scatterometry-based metrology tools may be accurately and reliably calibrated to enhance the accuracy of the critical metrology data obtained by such tools. For example, due to the complexity of modern semiconductor processing tools, there will be variations in the size, *e.g.*, critical dimension, of features formed on a wafer. While scatterometry tools may be accurately calibrated to a known nominal value, in measuring feature sizes that vary from this nominal value, undesirable errors may be introduced into the measurement process. That is, if a scatterometry tool is calibrated to measure critical dimensions having a target value of 100 nm, unwanted errors may be introduced in the measurement process when the scatterometry-based tool is used to measure critical dimensions above or below this value by a significant amount. The present

invention provides a structure and various methods that may be useful in calibrating such a tool to thereby eliminate or at least reduce the effects of such errors.

By way of example only, assuming that the feature to be measured has a nominal critical dimension of 100 nm, a scatterometry-based tool may measure many of the features to find that the critical dimension varies from 98-101 nm. However, some of the features may also initially be measured to have a critical dimension of, for example, 93 nm. At that time, the scatterometry-based tool may be calibrated using the array 61 of grating structures 60A-E disclosed herein. More particularly, the scatterometry tool may be used to measure one of the grating structures 60A-E having the closest target feature size to that of the measured dimension. In this case, the scatterometry-based tool may be used to measure the grating structure 60C having a known or target feature size of 90 nm. Based upon the measurement of the grating structure 60C, the scatterometry tool may be calibrated. That is, if, in measuring the grating structure 60C (of a known value of 90 nm), the tool data indicates a value of 91, then the tool may be calibrated based upon this data by multiplying the measurement data for the measured feature by a correction factor based upon the measurement data of the grating structure 60C. That is, a measured value of 93 nm would be properly calibrated to be 93 nm $\times$ (90/91) = 91.98 nm. While such errors in measurement may be very small in absolute terms, in the context of forming integrated circuit devices to the dimensions of modern devices, it may be critically important to accurately determine the size or critical dimension of the resulting features and to determine the efficiency of the processes used to manufacture such devices.

A variety of scatterometry tools 74 may be used with the present invention, *e.g.*, so-called 2θ-type systems and lens-type scatterometry tools. The scatterometry tool 74 may use white light, or some other wavelength or combination of wavelengths, depending on the specific implementation. Typically, the scatterometry tool 74 will generate an incident beam that has a wide spectral composition and wherein the intensity of the light changes slowly in comparison to changes in wavelength. The angle of incidence of the light may also vary, depending on the specific implementation. The optical characteristic traces generated by the scatterometry tool 74 may be based upon a comparison of light intensity to wavelength (for white light, fixed angle type scatterometry tools) or a comparison of intensity to incident angle (for angle resolved systems that use a single light source). Additionally, the light source 73 and the detector 75 may be arranged in a concentric circle configuration, with the light source 73 illuminating the grating structures 60A-E from a perpendicular orientation, *e.g.*, a reflectometer. The intensity of the reflected light may be measured as s- and p- polarization over either multiple angles or at multiple wavelengths.

In general, the scatterometry tool 74 (see Figure 4A) includes optical hardware, such as an ellipsometer or reflectometer, and a data processing unit loaded with a scatterometry software application for processing data collected by the optical hardware. For example, the optical hardware may include a Model OP5230 or OP5240 with a spectroscopic ellipsometer offered by Thermawave, Inc. of Fremont, California. The data processing unit may comprise a profile application server manufactured by Timbre Technologies, a fully owned subsidiary of Tokyo Electron America, Inc. of Austin, Texas and distributed by Thermawave, Inc.

Portions of the invention and corresponding detailed description are presented in terms of software, or algorithms and symbolic representations of operations on data bits within a computer memory. These descriptions and representations are the ones by which those of ordinary skill in the art effectively convey the substance of their work to others of ordinary skill in the art. An algorithm, as the term is used here, and as it is used generally, is conceived to be a self-consistent sequence of steps leading to a desired result. The steps are

those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of optical, electrical, or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, or the like.

It should be understood, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise, or as is apparent from the discussion, terms such as "processing" or "computing" or "calculating" or "determining" or "displaying" or the like, refer to the actions and processes of a computer system, or similar electronic computing device, that manipulates and transforms data represented as physical, electronic quantities within the computer system's registers and memories into other data similarly represented as physical quantities within the computer system memories or registers or other such information storage, transmission or display devices.

The present invention is generally directed to a method and a structure for calibrating a scatterometry-based metrology tool used to measure dimensions of features on a semiconductor device. In one illustrative embodiment, the method comprises measuring a critical dimension of at least one production feature formed above a wafer using a scatterometry tool, measuring at least one of a plurality of grating structures formed above the wafer using the scatterometry tool, each of the grating structures having a different critical dimension, and correcting the measured critical dimension of the at least one production feature based upon the measurement of the at least one grating structure.

In another illustrative embodiment, the method comprises forming a plurality of production features above a wafer, forming a plurality of grating structures above the wafer, each of the grating structures comprised of a plurality of features each having a target critical dimension that thereby defines a critical dimension of the grating structure, each of the grating structures having a different critical dimension, measuring a critical dimension of at least one of the production features using a scatterometry tool, measuring at least one of the grating structures using the scatterometry tool to determine a measured critical dimension of at least one feature of the at least one grating structure, and correcting the measured critical dimension of the at least one production feature based upon a comparison between the measured critical dimension of the at least one feature on the at least one grating structure and the target critical dimension of the feature on the at least one grating structure.

Through use of the present invention, better metrology data may be obtained in the course of manufacturing integrated circuit devices. The present invention may also be useful in determining the efficiency of various processes performed in manufacturing integrated circuit devices. In general, the present invention may result in improving device performance and increasing production yields.

The particular embodiments disclosed above are illustrative only, as the invention may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. For example, the process steps set forth above may be performed in a different order. Furthermore, no limitations are intended to the details of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered or modified and all such variations are considered within the scope and spirit of the invention. Accordingly, the protection sought herein is as set forth in the claims below.

CLAIMS:

1. A method for calibrating a scatterometry tool, the method comprising:

measuring a critical dimension of at least one production feature formed above a wafer (31) using said scatterometry tool (74);

measuring at least one of a plurality of grating structures (60A-E) formed above said wafer (31) using said scatterometry tool (74), each of said grating structures (60A-E) having a different critical dimension; and

determining a correction factor based upon said measurement of said at least one grating structure (60A-E), wherein said scatterometry tool (74) applies said correction factor to said measured critical dimension of said at least one production feature in determining the critical dimension of said at least one production feature.

2. The method as claimed in claim 1, wherein measuring a critical dimension of at least one production feature formed above a wafer (31) using a scatterometry tool (74) comprises measuring a critical dimension of at least one production feature formed above a wafer (31) using a scatterometry tool (74), said production feature comprised of at least one of a shallow trench isolation, a gate electrode structure and a conductive line.

3. The method as claimed in claim 1 or claim 2, wherein measuring at least one of a plurality of grating structures (60A-E) formed above said wafer (31) using said scatterometry tool (74), each of said grating structures (60A-E) having a different critical dimension, comprises measuring at least one of a plurality of grating structures (60A-E) formed above said wafer (31) using said scatterometry tool (74), each of said grating structures (60A-E) having a different critical dimension, a first of said plurality of grating structures (60A-E) having a critical dimension of a first size, at least one of said plurality of grating structures (60A-E) having a critical dimension of a second size, said second size being greater than said first size, the remainder of said plurality of grating structures (60A-E) having a critical dimension that is less than said first size.

4. The method as claimed in claim 1, 2 or 3, wherein measuring at least one of a plurality of grating structures (60A-E) formed above said wafer (31) using said scatterometry tool (74), each of said grating structures (60A-E) having a different critical dimension, comprises measuring at least one of a plurality of grating structures (60A-E) formed above said wafer (31) using said scatterometry tool (74), each of said grating structures (60A-E) having a different critical dimension, said critical dimensions of said grating structures (60A-E) varying from one another by a fixed increment.

5. The method as claimed in claim 1, 2, 3 or 4, wherein measuring at least one of a plurality of grating structures (60A-E) formed above said wafer (31) using said scatterometry tool (74), each of said grating structures (60A-E) having a different critical dimension, comprises measuring at least one of five grating structures (60A-E) formed above said wafer (31) using said scatterometry tool (74), each of said grating structures (60A-E) having a different critical dimension.

6. The method as claimed in claim 1, wherein measuring at least one of a plurality of grating structures (60A-E) formed above said wafer (31) using said scatterometry tool (74), each of said grating structures (60A-E) having a different critical dimension, comprises measuring at least one of a plurality of grating structures (60A-E) formed above said wafer (31) using said scatterometry tool (74), each of said grating structures (60A-E) having a different critical dimension, said critical dimension of each of said grating structures (60A-E) being defined by a critical dimension of features (38A) that comprise said grating structure (60A-E).

7. A semiconductor fabrication method comprising:

forming a plurality of production features above a wafer (31);

forming a plurality of grating structures (60A-E) above said wafer (31), each of said grating structures (60A-E) comprised of a plurality of features (38A) each having a target critical dimension that thereby defines a critical dimension of said

grating structure (60A-E), each of said grating structures (60A-E) having a different critical dimension; and

performing the method as claimed in claim 1 using at least one (38A) of said production features and at least one of said plurality of grating structures (60A-E);

wherein said correction factor is determined based upon a comparison between said measured critical dimension of said at least one feature (38A) on said at least one grating structure (60A-E) and said target critical dimension of said feature on said at least one grating structure (60A-E).

8. The method as claimed in claim 7, wherein forming a plurality of production features above a wafer (31) comprises forming a plurality of production features above a wafer (31), said production features comprised of at least one of a shallow trench isolation, a gate electrode structure and a conductive line.

9. The method as claimed in claim 7 or claim 8, wherein each of said grating structures (60A-E) are comprised of a plurality of at least one of a shallow trench isolation, a gate electrode structure and a conductive line.

10. The method as claimed in claim 7, 8 or 9, wherein said grating structures (60A-E) have a different critical dimension that varies by a fixed increment.

11. The method as claimed in claim 7, 8, 9 or 10, wherein measuring a critical dimension of at least one production feature formed above a wafer (31) using a scatterometry tool (74) comprises measuring a critical dimension of at least one production feature formed above a wafer (31) using a scatterometry tool (74), said production feature comprised of at least one of a shallow trench isolation, a gate electrode structure and a conductive line.

12. The method as claimed in any one of claims 7 to 11, wherein a first of said plurality of grating structures (60A-E) has a critical dimension of a first size, at least one of said plurality of grating structures (60A-E) has a critical dimension of a second

size, said second size being greater than said first size, the remainder of said plurality of grating structures (60A-E) having a critical dimension that is less than said first size.

13. The method as claimed in any one of claims 7 to 12, wherein forming a plurality of grating structures (60A-E) above said wafer (31) comprises forming at least five grating structures (60A-E) above said wafer (31).