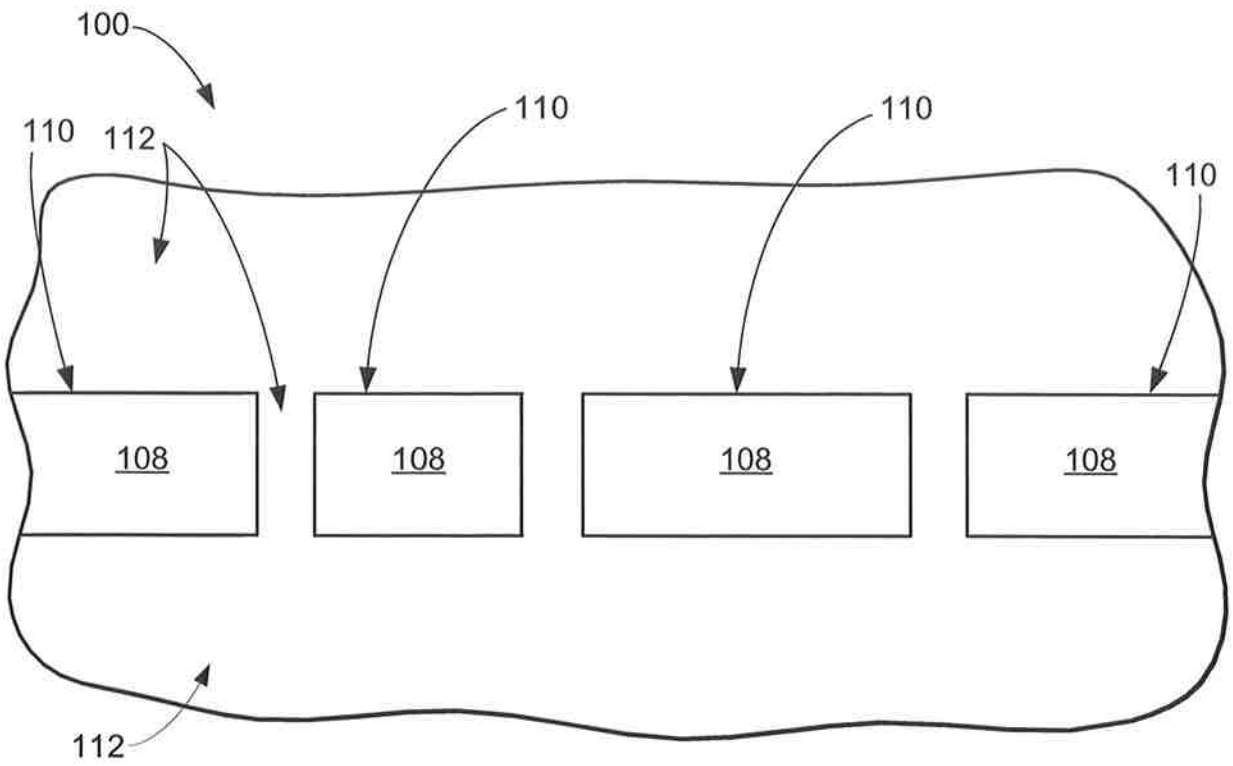

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FIG. 1B

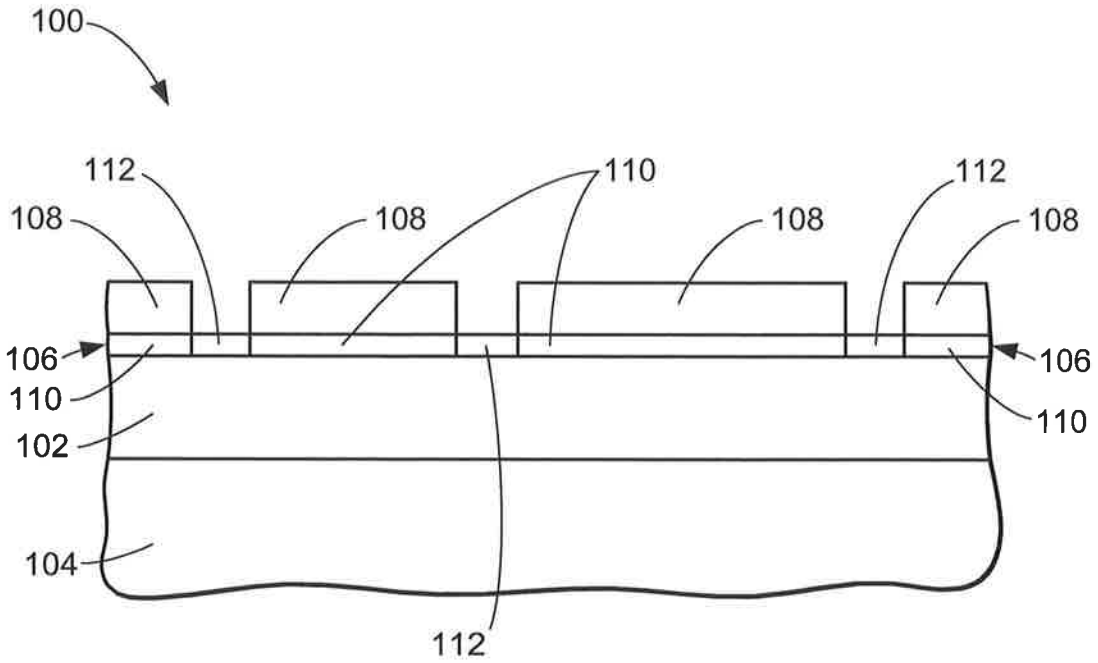

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FIG. 1A

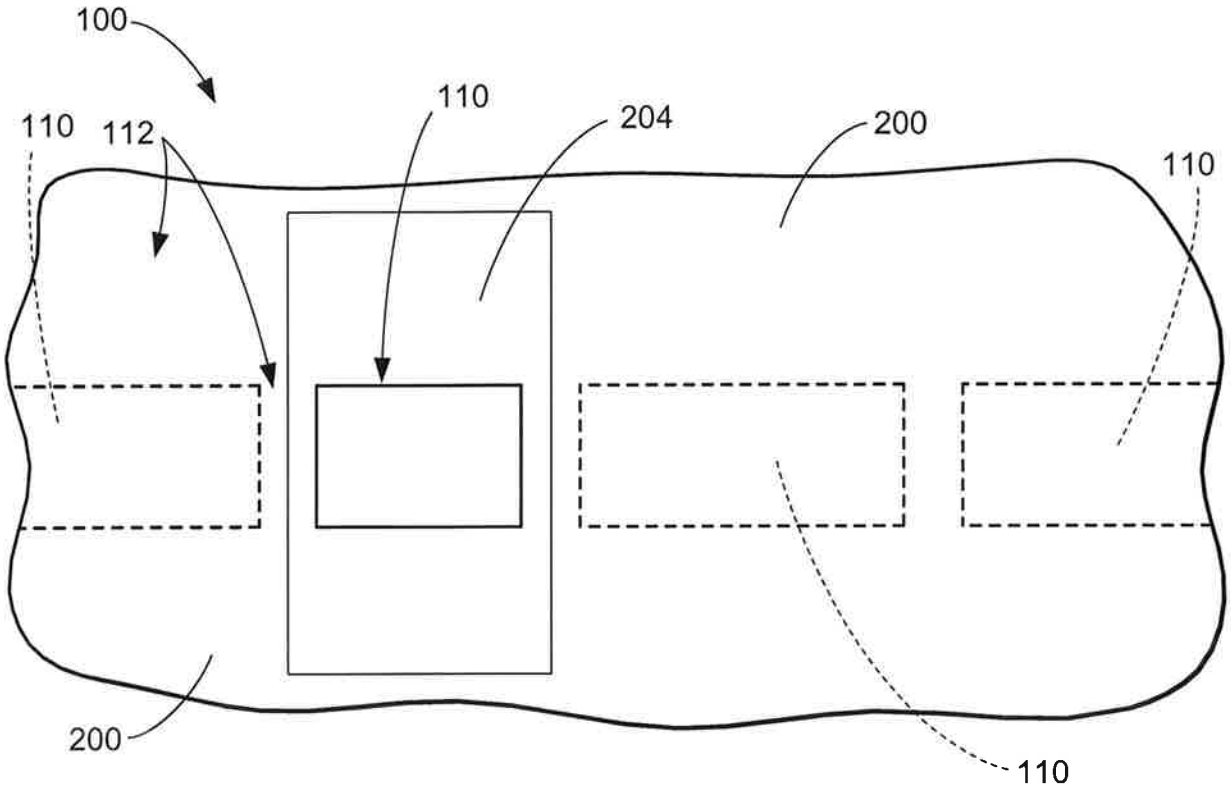

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FIG. 2B

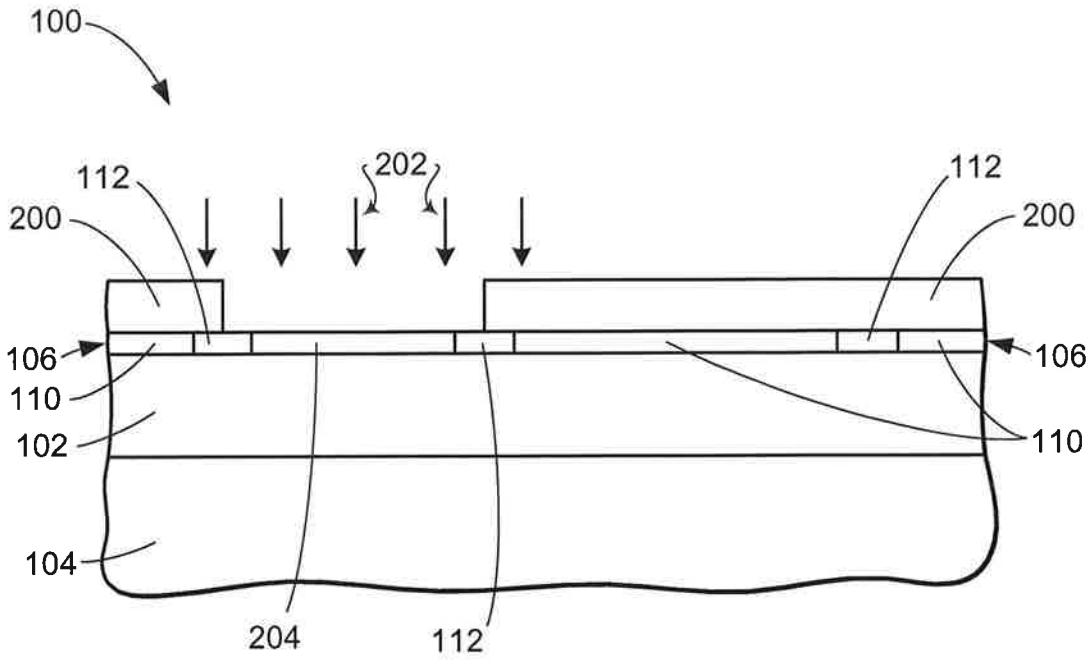

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FIG. 2A

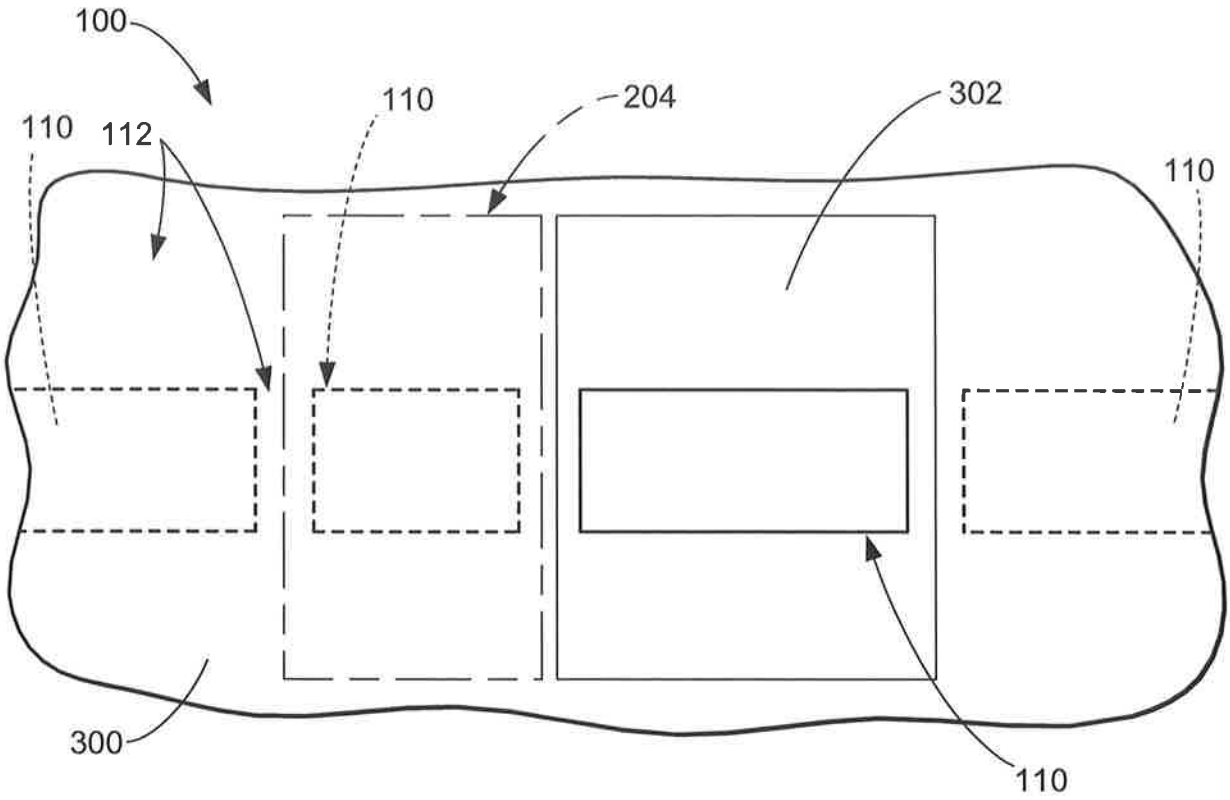

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FIG. 3B

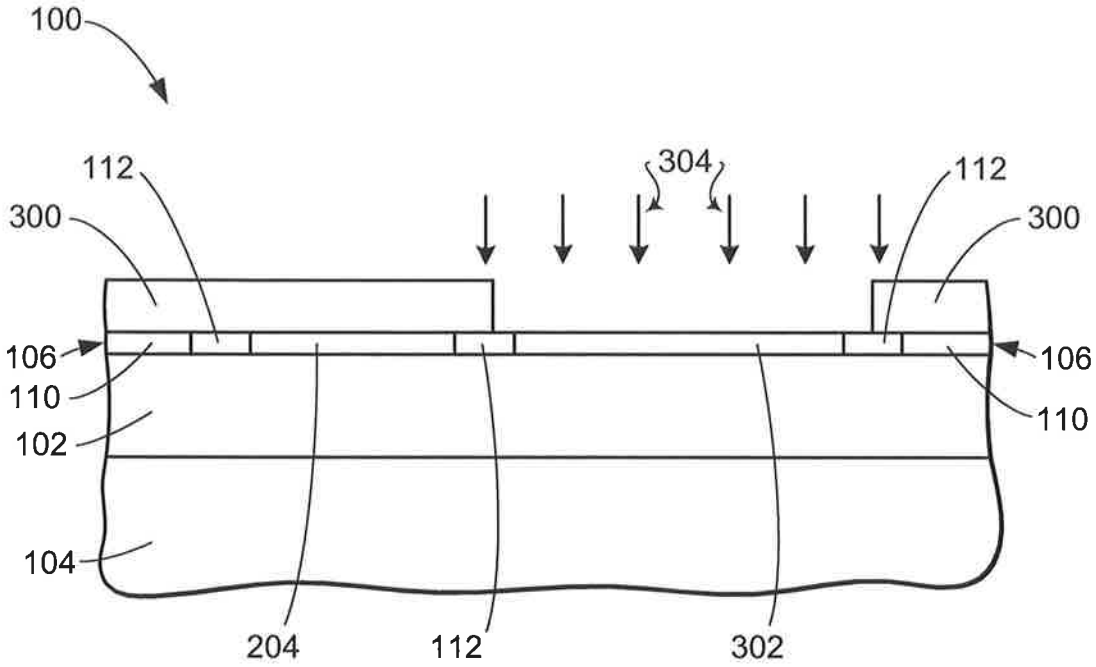

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FIG. 3A

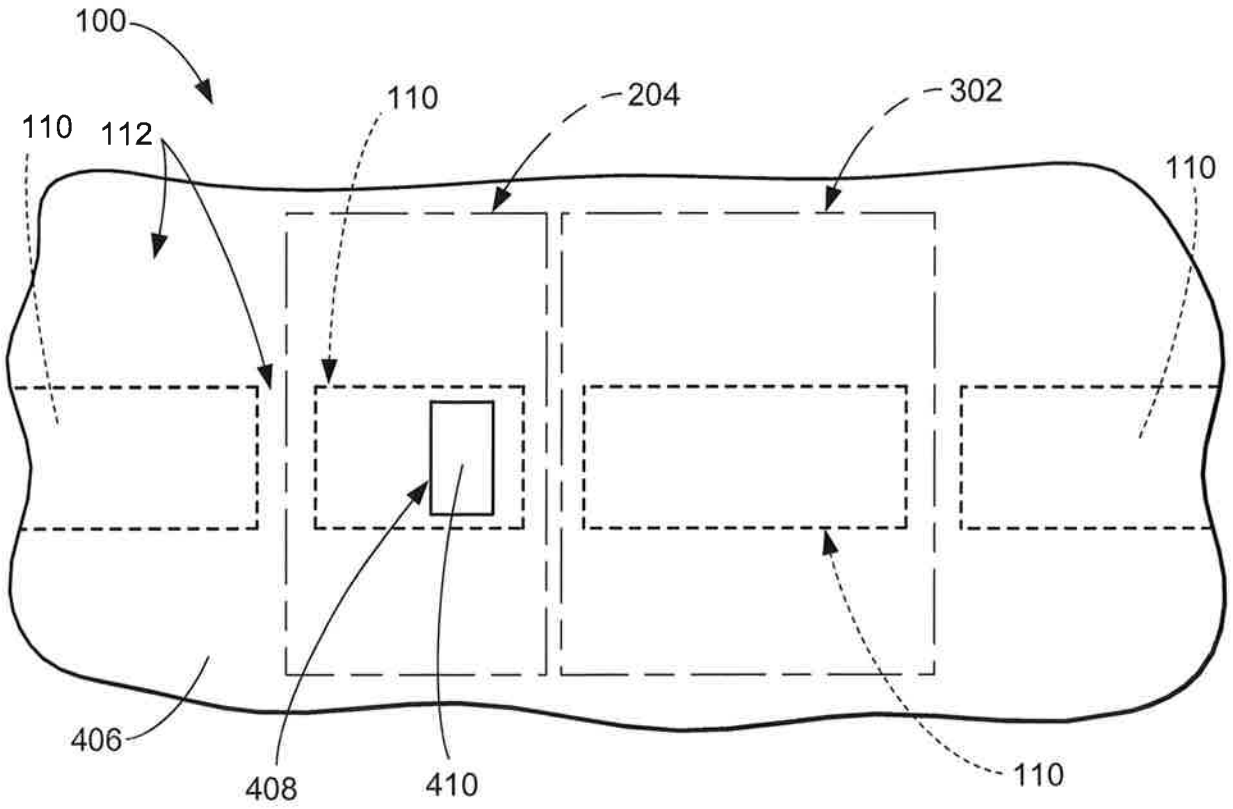

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FIG. 4B

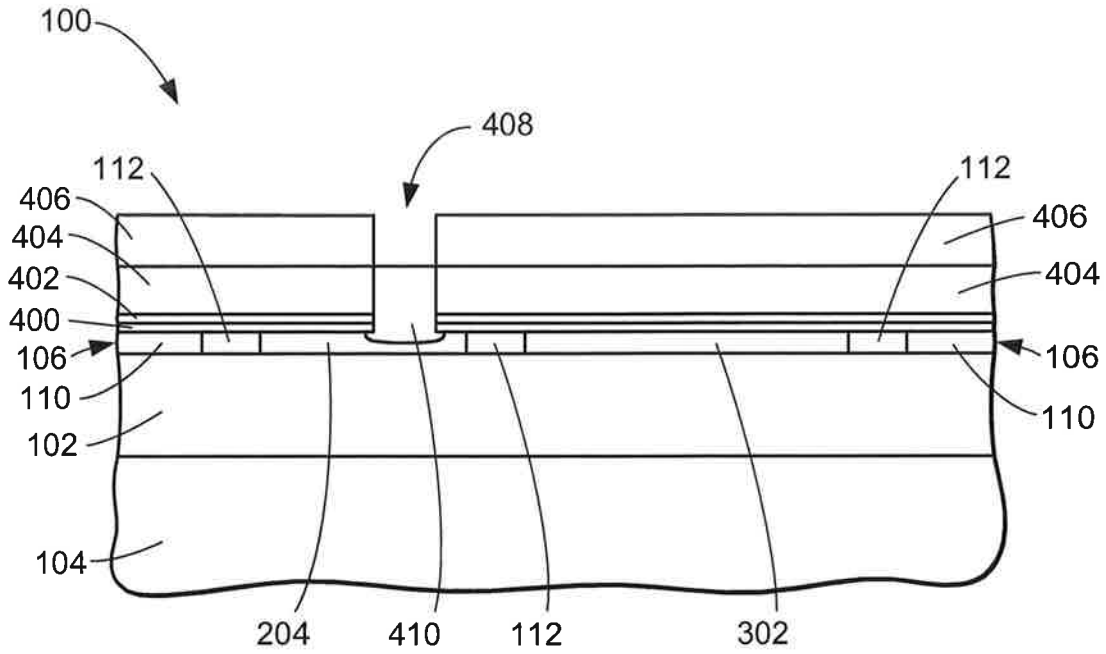

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FIG. 4A

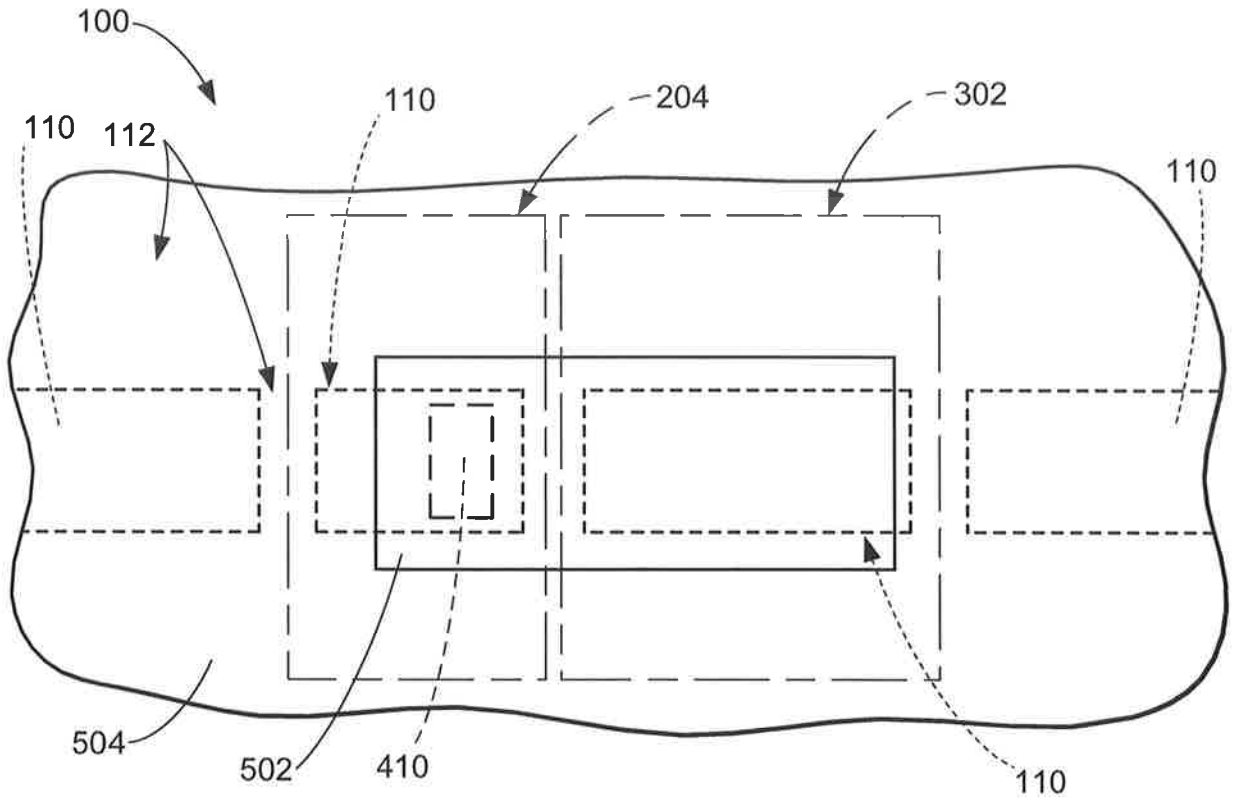

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FIG. 5B

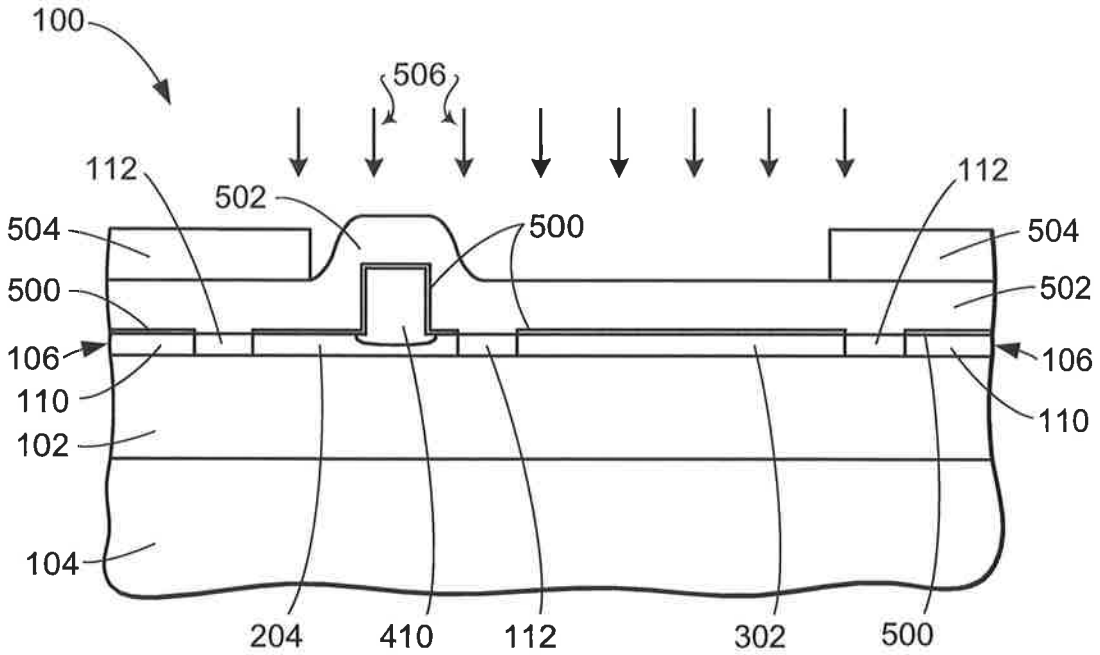

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FIG. 5A

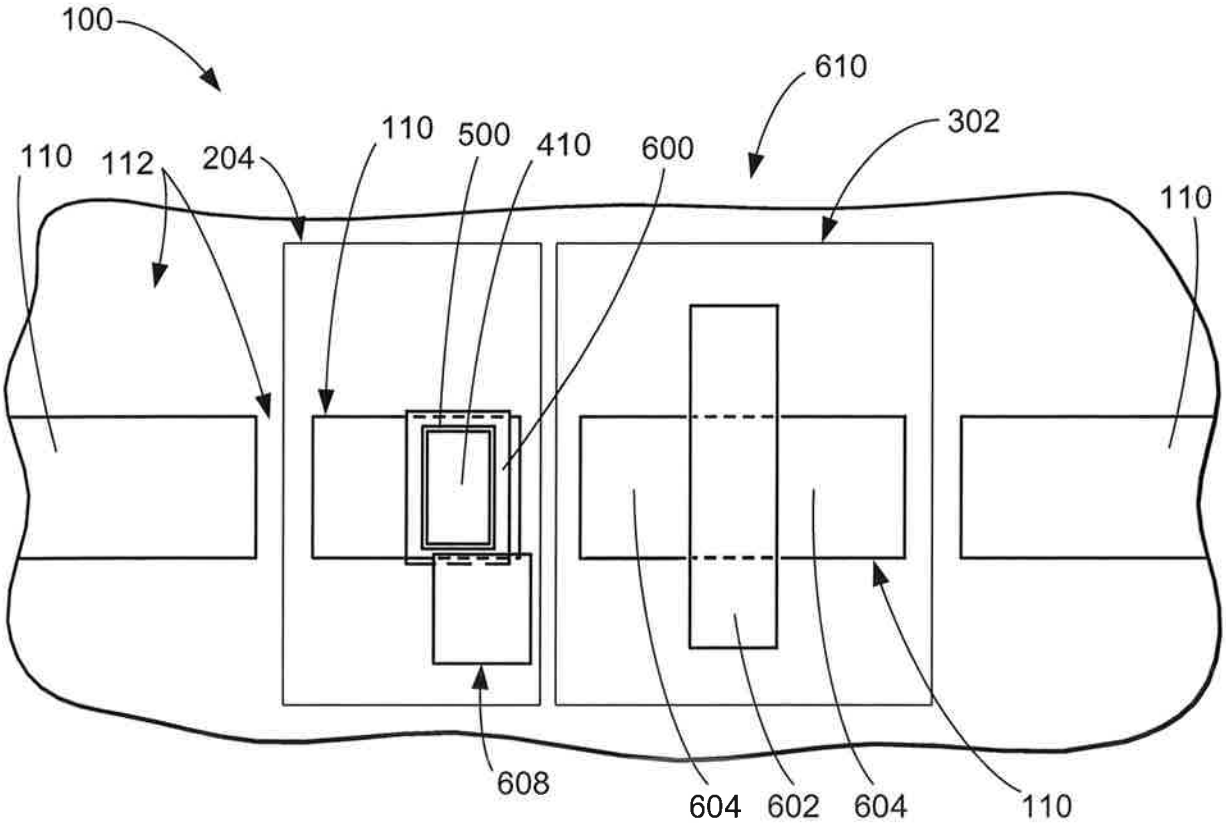

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FIG. 6B

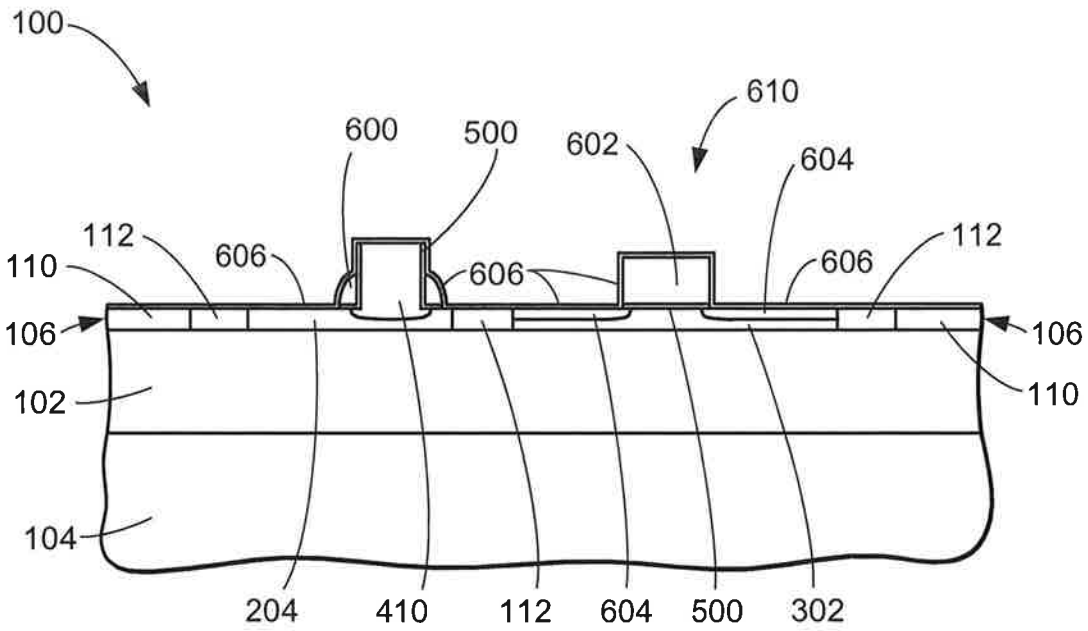

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FIG. 6A

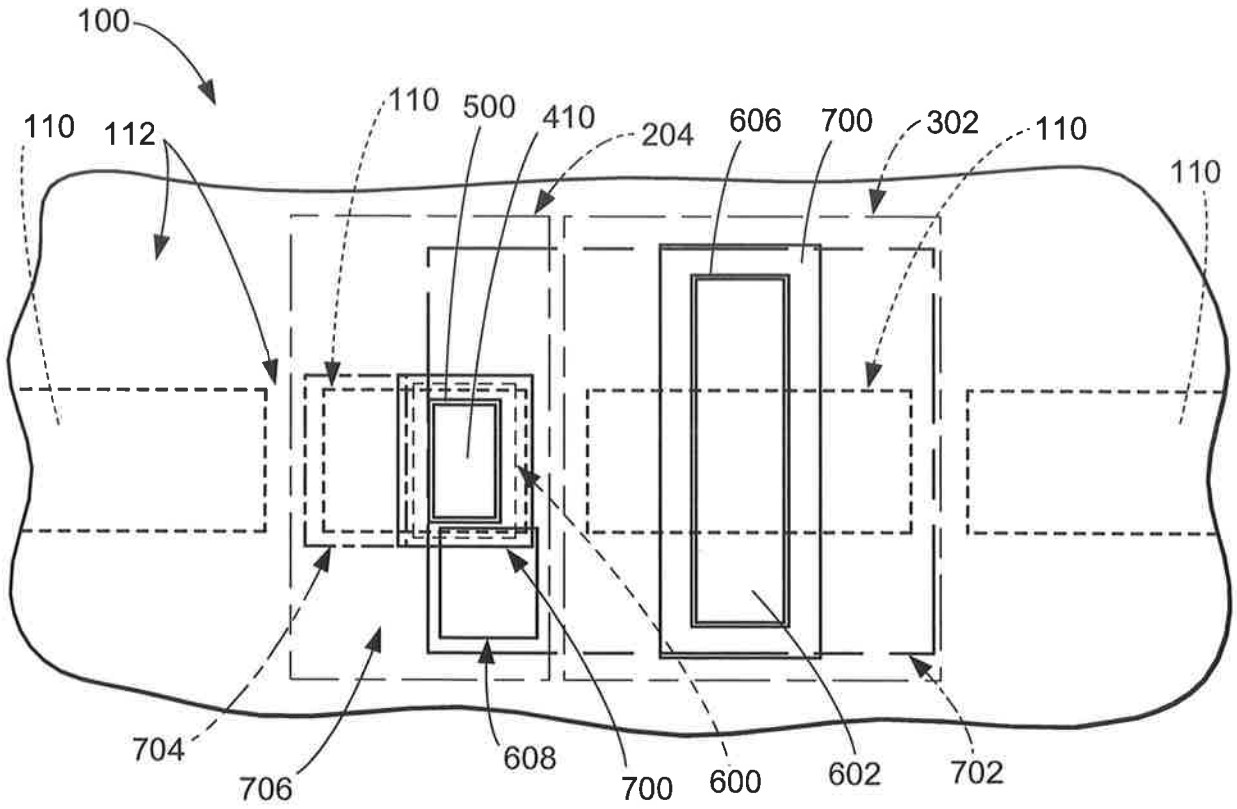

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FIG. 7B

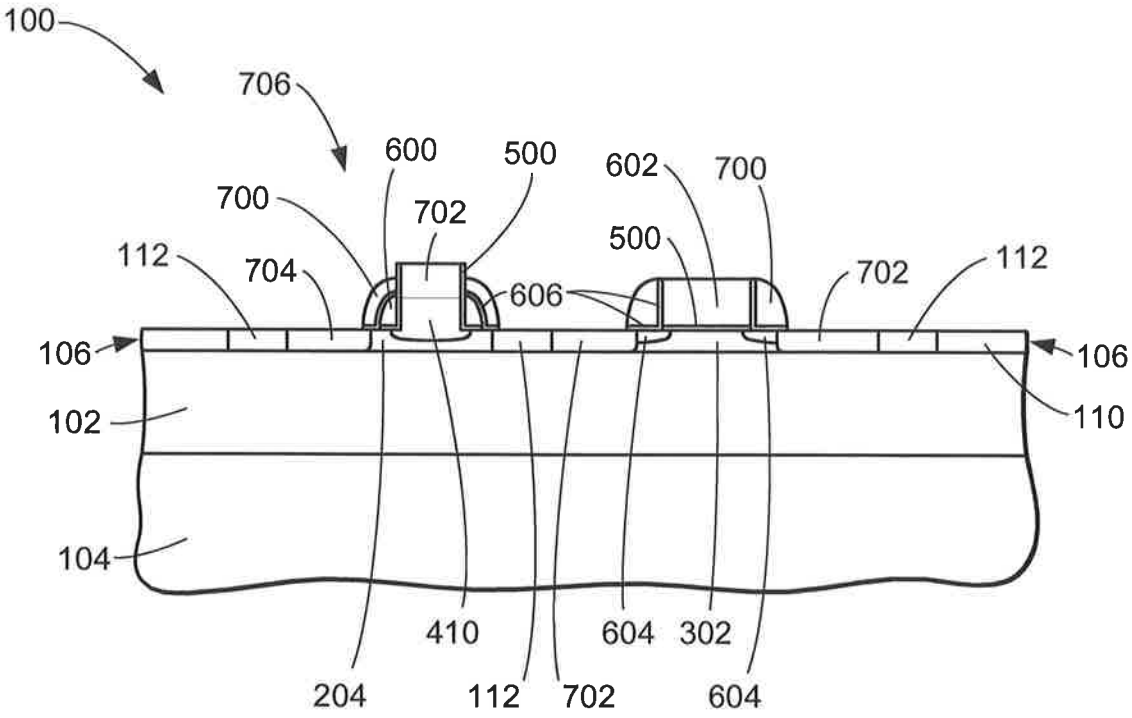

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FIG. 7A

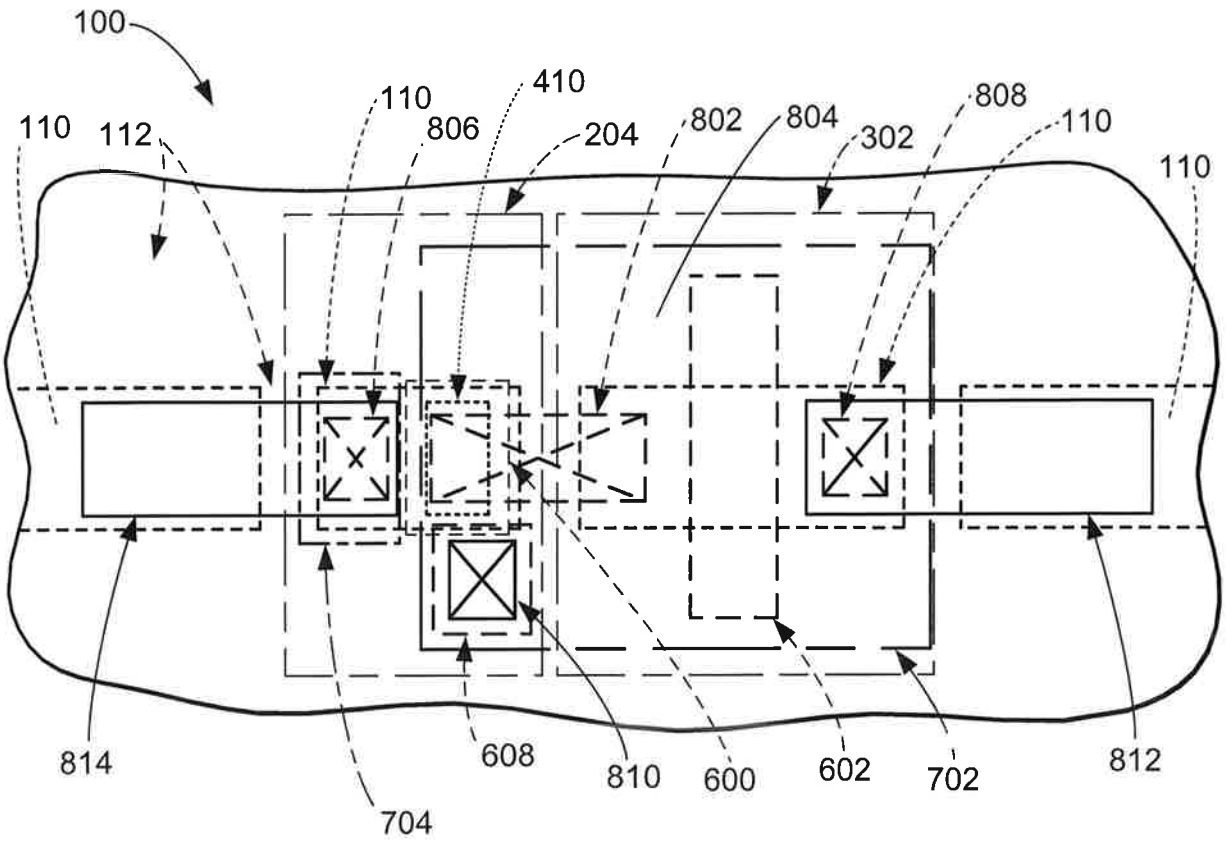

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FIG. 8B

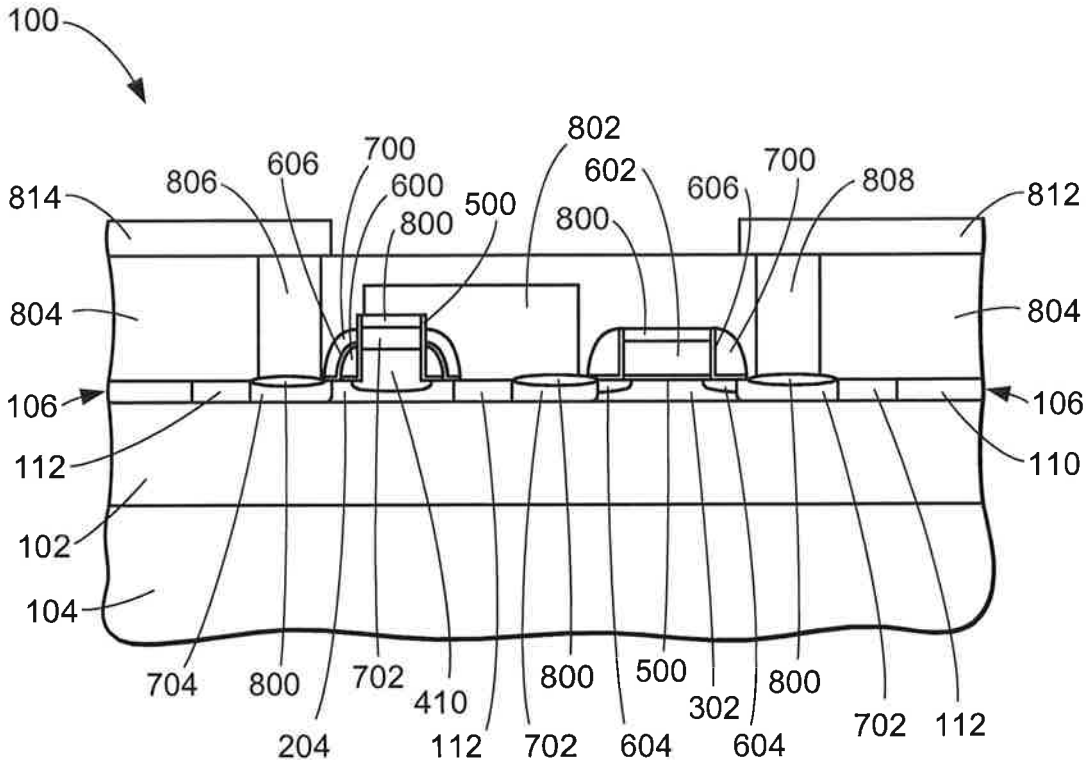

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FIG. 8A

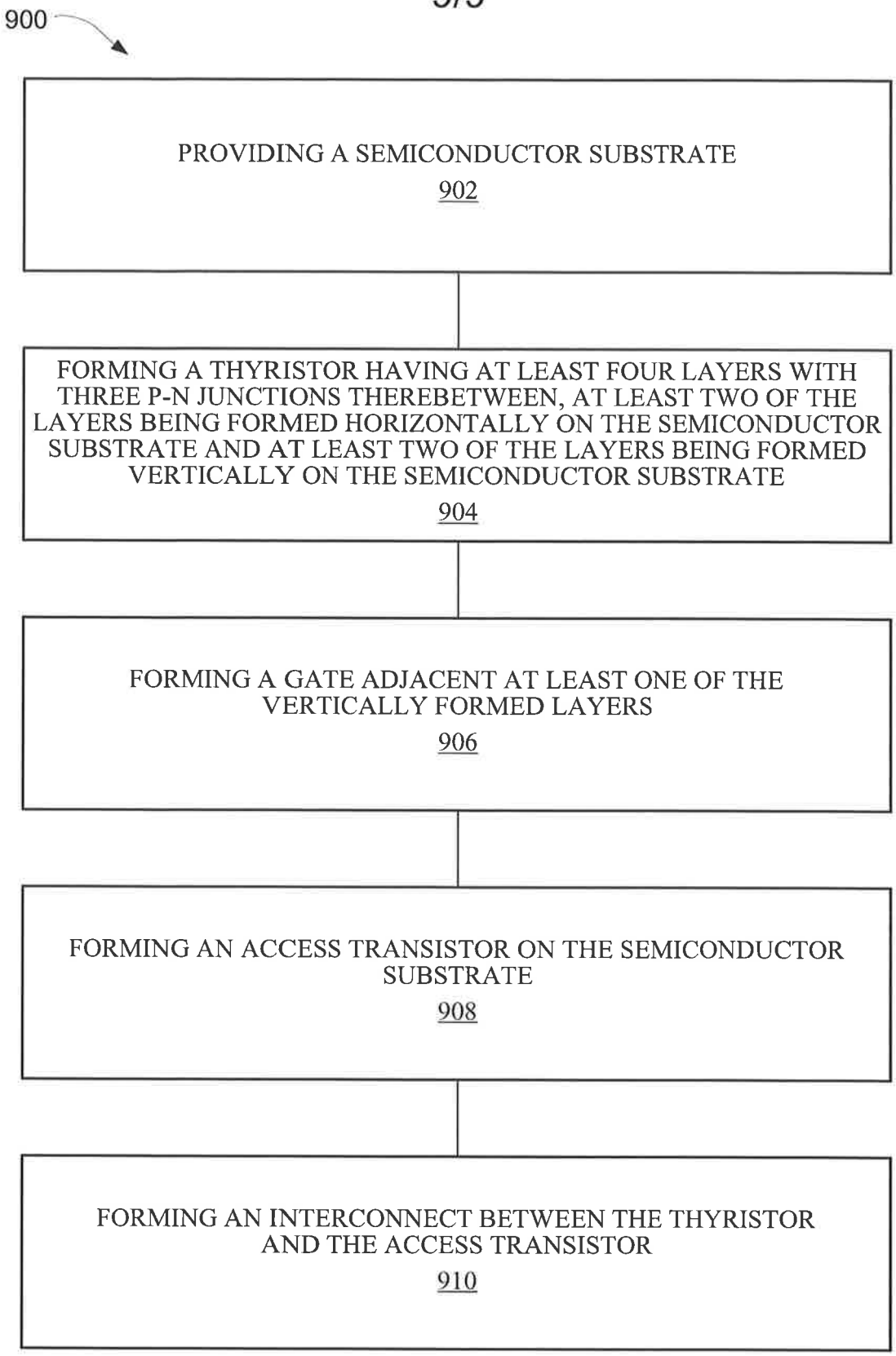

900
PROVIDING A SEMICONDUCTOR SUBSTRATE
902
FORMING A THYRISTOR HAVING AT LEAST FOUR LAYERS WITH THREE P-N JUNCTIONS THEREBETWEEN, AT LEAST TWO OF THE LAYERS BEING FORMED HORIZONTALLY ON THE SEMICONDUCTOR SUBSTRATE AND AT LEAST TWO OF THE LAYERS BEING FORMED VERTICALLY ON THE SEMICONDUCTOR SUBSTRATE
904
FORMING A GATE ADJACENT AT LEAST ONE OF THE VERTICALLY FORMED LAYERS
906
FORMING AN ACCESS TRANSISTOR ON THE SEMICONDUCTOR SUBSTRATE
908
FORMING AN INTERCONNECT BETWEEN THE THYRISTOR AND THE ACCESS TRANSISTOR
910

FIG. 9