Device Separation Structure and Semiconductor Device Improved in Wiring Structure

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to a semiconductor circuit device such as memory, photoelectric converting device, signal processing device, etc. to be mounted on various electronic instruments, particularly to a metal wiring structure and a semiconductor device improved in device separation structure.

Related Background Art

Conventionally, device separation in semiconductor device has been constituted as shown in Fig. 1. In the Fig. 1, the symbol 1 is metal wiring, 2, 3 are device regions where transistor, FET, resistance, condenser, photosensor, etc. are formed, and electrical insulation thereof is effected by the device separation region, namely the Si substrate 4 doped with an impurity or the Si layer 5 doped with the same impurity. The potentials of the device separation regions of 4, 5 are fixed by the metal wiring 1 or 6.

For example, the device separation region of a solid image pick-up device is constituted as shown in

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Fig. 2. In the Figure, the symbol 4 is a P type substrate, 5' an n^+ buried layer, 2 an n^- epitaxial growth layer (hereinafter epitaxial growth is written as epi), 5 an n^+ layer. The above n^- epi layer 2 is a photoelectric converting region, and the n^+ buried layer 5' and the n^+ layer 5 are device regions.

The n^- epi layer 2 is maintained at a certain positive potential through the n^+ buried layer 5' and the n^+ layer 5. By the build-in electrical field through junction between the n^- epi layer 2 and the n^+ layer 7, the electrons formed by photoirradiation are absorbed in the n^+ buried layer 2 and the n^+ layer 7, and the positive holes cannot be diffused to the confined adjacent picture elements, whereby cross-talk can be prevented.

However, prior art examples had the technical tasks as follows.

(1) There was an impedance of about some ten to some hundred $\Omega/\square$. For this reason, current flowed into the region 5, and when the potential is elevated, parasitic transistor turned on between the device regions 2 and 3, whereby latch-up or unstable actuation of function was caused to occur.

(2) On account of the impedance in the region 5, cross-talk in the device regions 2 and 3 was generated to cause unstable actuation.

Particularly in the case of a solid image

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pick-up device,

(3) The positive holes having acquired thermally high energy will be diffused to the adjacent picture elements.

(4) Since the device separation region is also a semiconductor, carriers will be generated when light is irradiated.

(5) The width of the n^+-Si device separation cannot be made narrow in process to obstruct reduction of picture element, whereby higher resolving power of solid image pick-up device has been obstructed.

On the other hand, as the metal wiring structure in a highly integrated semiconductor device, for example, there has been known one having an interlayer insulating film 52 comprising silicon oxide, etc. formed on the surface of a semiconductor substrate 51 comprising silicon and a metal wiring layer 53 comprising Al, Al-Si, etc. formed on the interlayer insulating film 52 as shown in Fig. 2A.

In the semiconductor device equipped with the metal wiring of such structure, the sectional area of wiring has been increased by enlargement of the width dimensions of the respective wirings, thereby ensuring necessary current tolerant capacities for the respective wirings, and therefore the flat area of wiring will be increased and improvement of wiring

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without making greater the device size is limited.

For this reason, for improvement of wiring density, for example, a semiconductor device of a wiring structure having the respective wirings laminated in multiple layers as shown in Fig. 2B has been known.

In this semiconductor device, two layers of metal wiring are laminated through an insulating film.

In the following, the outline of the process for preparing the semiconductor device shown in 2B is described.

First, after formation of various necessary functional devices such as bipolar transistor, MOS transistor, MOS diode, etc. on a part of the surface of the semiconductor substrate 1, on the remaining surface of the semiconductor substrate 51 is formed a first interlayer insulating film 52 comprising PSG (Phospho silicate glass), etc. according to the normal pressure CVD method with a thickness of 0.5 to 1.0 μm, and the first interlayer insulating film 52 is applied with annealing.

Next, patterning by use of a resist is applied on the first interlayer insulating film 52 as described above to form openings 52a for taking out electrodes of various functional devices. Subsequently, according to the sputtering method,

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after deposition of a wiring material comprising, for example, Al-Si according to the sputtering method on the surface of the first interlayer insulating film 52 and internally of the openings 52a, the first wiring layer 53 is formed by patterning by use of a resist.

Next, on the first wiring layer 53 and the first interlayer insulating film 52 are formed a second interlayer insulating film 54 comprising PSG with a thickness of about 0.5 to 1.0 μm according to the normal pressure CVD method, openings 54a for connecting the first wiring layer and the upper wiring layer as described below to a part of the second interlayer insulating film 54 corresponding to the upper portion of the first wiring layer 53 are formed.

Next, on the second insulating film 54 and internally of the openings 54a, a wiring comprising, for example, Al-Si is deposited, followed by formation of the second wiring layer 55 for connecting the second wiring layer 55 for connecting the first wiring layer 52 through the portion of the openings 54a by patterning.

Next, on the second interlayer insulating film 54 and the second wiring layer 55, a passivation film 6 can be formed with a thickness of 0.5 to 1.0 μm according to the plasma CVD method to prepare a

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semiconductor device with a metal double layer wiring structure shown in Fig. 2B.

In the semiconductor device having a multi-layer wiring structure of such constitution, a wiring with wiring density by far higher than the semiconductor device with the monolayer wiring structure shown 2A can be realized.

However, in the semiconductor device having a multi-layer wiring structure as described above, since an interlayer insulating film is provided between the wiring at the lower part and the wiring at the upper part, the surface stepped difference due to the wiring portion will become greater as the number of the lamination is more, whereby the degree of freedom in design in the wiring structure is regulated because of movement of the position (migration) of the wiring portion relative to the semiconductor substrate at the wiring portion or the shape of the contact hole necessary for connection between the respective insulating layers. Thus, also in this case, improvement of wiring density is limited and it has been difficult to enhance wiring density more than a certain level.

Further, in a semiconductor device with a multi-layer structure, surface unevenness becomes greater as the layer is upper, and therefore slippage in alignment becomes greater during mask registration

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in patterning when laminating further wiring, whereby wiring could not be formed with good precision at the predetermined position relative to the semiconductor substrate, thus involving the problem with respect to reliability of wiring.

SUMMARY OF THE INVENTION

A primary object of the present invention is to provide a semiconductor device having a wiring structure more excellent than in the prior art.

Another primary object of the present invention is to provide a semiconductor device having more excellent device separation function than in the prior art.

First, an object of the present invention is to provide a semiconductor device having a device separation structure with a device region being formed on a substrate doped with an impurity, a device separation region doped with the same impurity as in the above substrate formed in the device region and a metal wiring formed on the surface of the above device region or on the back of the above substrate, wherein an aluminum deposited layer extending in the longitudinal direction connected to the above metal wiring is formed within the above device separation region.

Another object of the present invention is to

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provide a semiconductor device which can reduce the impedance of the device separation region of semiconductor device, prevent generation of latch-up or cross-talk and give stability in actuation.

Still another object of the present invention is to provide a semiconductor device equipped with a wiring structure which can ensure necessary current tolerable quantity even if the wiring flat area may be small.

Still another object of the present invention is to provide a semiconductor device comprising a device region formed on a substrate, and also a first device separation region formed doped with an impurity formed between these substrate and device region, with the respective ends being connected to the both ends of the above-mentioned first device separation region, and the respective other ends exposed on the surface of the above-mentioned device regions, thus forming a trench metal layer of aluminum or composed mainly of aluminum.

Still another object of the present invention is to provide a semiconductor device comprising a device region formed on an insulating substrate, having a trench metal layer of aluminum or composed mainly of aluminum which becomes the device separation region extending in the longitudinal direction with its one end being in contact with the

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above-mentioned insulating substrate and its other end being formed exposed on the surface of the above-mentioned device region.

Still another object of the present invention is to provide semiconductor device which removed cross-talk between the picture elements and enables higher densification of picture elements by using a trench metal layer constituted by selective growth deposition of aluminum or a metal composed mainly of aluminum within the trench for forming the device separation layer.

Still another object of the present invention is to provide a semiconductor device which can also reduce the lay-out, because the trench metal layer can be used as the wiring line.

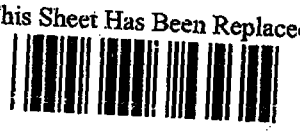
Still another object of the present invention is to provide a semiconductor device comprising a metal wiring layer for connecting at least two functional devices to the inner portion of a semiconductor substrate having at least functional devices as mentioned above.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A, 1B, 2A, 2B are constitutional views for illustration of the semiconductor device of the prior art.

Fig. 3 is a constitutional view of the

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pertinent portion of the semiconductor device showing a first example of the present invention.

Fig. 4 is a constitutional view of the pertinent portion of the semiconductor portion showing a second example of the present invention.

Fig. 5 is a constitutional view of the pertinent portion of the semiconductor portion of the semiconductor device applied to the present invention.

Fig. 6A is a constitutional view of the semiconductor device applied to the present invention, Fig. 6B is a circuit diagram of the same device.

Figs. 7A to 7D are diagrams of the steps for preparing the semiconductor device applied to the present invention.

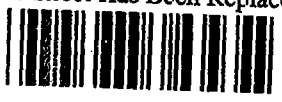
Fig. 8 is a constitutional view of the pertinent portion of the semiconductor device showing a third example of the present invention.

Fig. 9 is a constitutional view of the semiconductor device showing a fourth example of the present invention.

Figs. 10A and 10B are schematic views for illustration of the logic circuit according to the present invention.

Fig. 11 is an upper view showing the logic circuit according to the present invention.

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Fig. 12 is a schematic sectional view showing the wiring structure intended to apply a positive potential.

Fig. 13 is a schematic sectional view showing the wiring structure intended to apply a negative potential.

Fig. 14 is a schematic sectional view showing an example of a multi-layer wiring structure in the semiconductor device of the present invention.

Figs. 15A to 15C are schematic views for illustration of the preparation method of the wiring structure in Fig. 14.

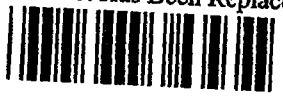
Figs. 16, 17 are schematic view showing an example of the film forming device to be used for practicing the film forming method suitable for formation of the wiring layer in the semiconductor device according to the present invention.

Fig. 18 is a schematic plan constitutional view of the device shown in Figs. 16, 17.

Fig. 19 is a schematic constitutional view with the movement order shown by arrowheads in Fig. 18.

Figs. 20A to 20D are schematic view for illustration of the film forming method suitable for formation of the wiring layer in the semiconductor device according to the present invention.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

One preferred embodiment of the present invention has a longitudinally lengthy buried region comprising a metal in the device separation region.

When the predetermined region which is a part of the semiconductor substrate and the longitudinally lengthy buried region of a metal are electrically connected, the following embodiment is taken.

For example, when the metal is electrically connected to a predetermined region only at bottom, the whole side wall should be preferably coated with an insulating film.

On the other hand, when the metal is insulated from a part of the side groove or bottom of the groove, only said part is coated with an insulating film.

Example 1

Fig. 3 is a drawing representing best the specific feature of the first example of the present invention, in which the symbol is the device separation wiring formed in the longitudinal direction within the device separation region 5 as described below according to the Al-CVD method as described below, 2 the first device region, 3 the second device region, 4 the Si substrate doped with an impurity, 5 the device separation region doped with an impurity of the same type as in the substrate

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4.

As shown in the drawing, by deposition the device separation wiring 1 deeply in the longitudinal direction with an aspect ratio of 1.0 or more, preferably 2.0 or more, optimally 3.0 or more, the impedance of the device region 5 can be reduced without bringing about increase of chip area. By reduction of impedance, the following effects can be obtained:

(1) Prevention of latch-up;

(2) Improvement for functional lowering due to mutual interference between devices (reduction of cross-talk).

Next, the process for preparing a semiconductor device having the device separation structure with the above constitution is described.

i) On a mono-electroconductive semiconductor substrate, for example, a P-type Si substrate 4, an n-type epi-layers 2, 3 are formed by epitaxial growth as the layer having the impurity of the reverse conduction type to the substrate 4.

ii) Next, after formation of the oxidized film to 0.5 to 1.0 μm on a surface of above-mentioned epi-layers 2, 3 by thermal oxidation, impurities (e.g. P type) with the reverse conduction type to the epi-layers 2, 3 are formed on the device separation region 5 by patterning by ion injection with the

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above-mentioned oxidized film as the mask. The diffusion layer is made so as to reach the subbing semiconductor substrate 4.

iii) Next, after the oxidized films on the surfaces of the epi-layers are removed, again oxidized films with a thickness of 100 to 1000 Å are formed. Then, the above-mentioned device separation region 5 is internally opened by regist patterning, and the oxidized film and the epi-layer are etched in two steps with the resist as the mask to form grooves. In this case, the depth of the groove is made to reach the subbing semiconductor substrate 4. After completion of etching, the resist is removed.

iv) Next, by use of DMAH and hydrogen as the Al-CVD method as described above, Al is buried in the grooves provided within the epi-layers 2, 3. Here, the material to be buried within the grooves is not limite to Al, but Al-Si, Al-Ti may be also used as the metal material as described above.

Example 2

Fig. 4 shows a drawing representing best the specific feature of the second example, wherein the symbol 1 is the device separation wiring of the buried type with a large aspect ratio, 2 the first device region, 3 the second device region, 4 the Si substrate doped with an impurity, 5 the device

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separation Si doped with the impurity of the same type as in 4, and 6 the back metal wiring.

By fixing of the potential in the device separation region 5 with the device separation wiring 1 and the back metal wiring 6, no wiring from the chip upper surface will be required to result in reduction of chip area.

Next, the process for preparing the semiconductor device having the device separation structure having the above-mentioned structure is described.

The steps i) - ii) are practiced in the same manner as in Example 1, and hence description thereof is omitted. iii) Next, after formation of an oxidized film on the back surface of the semiconductor substrate 4 by thermal oxidation, patterning is effected so as to form openings only on the back surface of the semiconductor substrate 4 immediately below the above device separation region 5.

Then, continuously to the oxidized film from the back surface of the semiconductor substrate 4, the semiconductor substrate 4 is etched to provide grooves on the back surface of the semiconductor substrate 4. The depth of the grooves is made to extend through the semiconductor substrate 4 until reaching the above-mentioned diffusion layer 5 for

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device separation. iv) Next, as the Al-CVD method, Al is deposited selectively at the groove portions similarly as in Example 1 to bury Al within the grooves. Then, according to the sputtering method of the non-selective mode, an Al film is formed on the whole back surface of the semiconductor substrate 4.

Example 3

Next, the semiconductor functional devices formed in the device region 2 or 3 is described by referring to Fig. 5 and Fig. 6. The semiconductor functional device is characterized by forming a device wiring 12 with a large aspect ratio for fixing the back gate of the MOS type transistor (P well region 10 of nMOS, and n-epi or n-well region 11 of pMOS) at any desired potential in the P-well region 10 the n-epi or n-well region in the longitudinal direction according to the Al-CVD method as described above.

Example 4

Fig. 6A is a sectional constitutional view of another semiconductor functional device, and Fig. 6B is the circuit diagram of the same device. The device is characterized by forming the device separation wiring 12 for reducing the resistance in the back gate when the P-well 10 which is the back gate of the MOS type transistor and the n-epi or n-well 11 are at the same potential as the source region (or drain

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region) in the source (or drain) region 13 according to the Al-CVD method as described above.

In the MOS type transistor of the prior art, the resistance of the back gate has been a cause for latch-up or lowering in function. Also, since the device region and the wiring region have been increased in order to reduce this problem, increase of layout area has been brought about.

In contrast, in the above-mentioned device, as shown in Fig. 5 and Fig. 6A, by depositing the device wiring 12 deeply in the longitudinal direction according to the Al-CVD method, the resistance of the back gate can be reduced with smaller wiring area to ameliorate latch-up or lowering in function which has been the problem in the prior art. Particularly, in the logical circuit (e.g. invertor) as shown in Fig. 6, the wiring structure can be made as shown in the figure in the region where the power source and the source (or drain) are at the same potential, whereby less wiring area is required and the problems of the prior art can be improved.

Next, the process for preparing the device shown in Fig. 5 is described by referring to Fig. 7A to Fig. 7D.

First, according to the known C-MOS preparation technique, working is practiced to the state immediately before formation of contact holes

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(Fig. 7A).

Next, according to the photolithography by use of a resist, a resist image corresponding to the openings to be formed of about 0.8 μm at the P-well portion of n-MOS, the n-epi or n-well portion 11 of P-MOS (Fig. 7B).

Next, by use of the CHF_3-C_2F_6 type dry etching, openings 22 extending through the two layers of the interlayer insulation layer 20 and the field oxidized film 21 are formed. Then, without removal of the resit, the silicon substrate is etched vertically to about 1 μm by the Cl_2-$CBrF_3$ type dry etching.

Next, by use of the Al-CVD method as described in Example 1, aluminum 12 is buried to the upper surface of the interlayer insulation film. The total amount buried is made 2.5 μm as the total with the silicon substrate groove being 1 μm, the field oxidized film 21 being 8000 Å, and the interlayer insulation layer 20 being 7000 Å. (Fig. 7C).

Employing subsequently known techniques contact opening formation, aluminum wiring formation, etc. can be practice to complete the sample.

Preparation of the example shown in Fig. 6 can be also practiced according to the same procedure as in Fig. 5. The difference is only that the

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opening formation site becomes the source (or drain) portion of the MOS transistor, and the interlayer insulation layer-gate oxidized film is extended through instead of extending through of the interlayer insulation layer-field oxidized film during opening formation.

As described above, by depositing Al in the longitudinal direction by use of the Al-CVD method within the device separation region, reduction of chip area can be effected as compared with the case when obtaining the same effect without use thereof, whereby Al wiring portion can be made smaller, with the result that the production cost can be made lower.

Example 5

Fig. 8 is a drawing showing best the specific feature of the present example of the present invention, in which the symbol 4 is a P substrate, 5' an n^+ buried layer, 2 an n^- epi-layer, and 1 a trench metal layer formed according to the CVD method. The above trench metal layer 1 has its one end exposed on the above n^- epi-layer surface 2 with other end being connected to the above n^+ buried layer 5'.

The n^- epi-layer 2 is a photoelectric converting region (called device region or activation region), and the n^+ buried region 5' and the trench metal layer 1 are device separation regions. The

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trench metal layer 1 also a wiring line.

The n^- epi-layer 2 is maintained at a certain potential through the n^+ buried layer 5' and the trench metal layer 1.

In the above-mentioned structure, the electrons formed by photoirradiation are absorbed primarily into the n^+ buried layer 5' through the built-in electrical by the junction of the n^+ buried layer 5' and the n^- epi-layer 2. The positive holes are closed within the picture elements by the built-in electrical field.

The positive holes which tend to be diffused to the adjacent picture elements will be all absorbed in the trench metal layer 1, and therefore there can be no cross-talk between picture elements.

The device separation region 1 is formed by forming the trench (groove) by etching, and then depositing aluminum or a metal composed mainly of aluminum on the groove according to the selective CVD method as described above, whereby the device separation region width can be reduced as compared with the prior art, enabling higher densification of picture elements.

The trench metal layer 1 has a low resistance and therefore can be also utilized as the wiring line, whereby reduction of the layer is rendered possible.

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Next, a process for preparing the device separation structure semiconductor device of the above constitution is described,

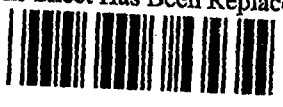
i) On a monoconduction type semiconductor, for example a P type Si substrate 4 are formed grooves with wide width shallowly on a part thereof. In the grooves, n^+ buried layer 5' containing impurities of the opposite conduction type to the substrate 4 according to the epitaxial growth by use of as mask.

ii) On the substrate 4 having the n^+ buried layer 5' formed as described above, an n^- epi-layer 2 which becomes the photoelectric converting region is formed by epitaxial growth.

iii) Next, after formation of oxide flms with a thickness of 0.5 to 1.0 μm on the surface of the above n^- epi-layer 2 by thermal oxidation, opening are formed internally of the above n^- epi-layer at the both ends of the above-mentioned n^+ buried layer by resist patterning, followed by etching with the resist as the ask to form a trench. In this case, the depth of the trench is made the depth which reached the subbing n^+ buried layer 5'. After completion of etching, the resist was removed.

iv) Next, by use of the Al-CVD method as described below using DMAH and hydrogen as the selective CVD method, the substrate surface

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temperature was maintained at 270 °C, and Al is buried in the trench provided within the n^- epi-layer. Here, the material to be buried in the trench is not limited to Al, but Al-Si, Al-Ti, etc. may be also employed as the metal material.

Example 6

Fig. 9 is an example in which the present invention is applied to a semiconductor device having an insulating substrate. 1 is a trench metal layer, 4' an insulation substrate and 2 a semiconductor substrate layer.

The above semiconductor layer 2 is a photoelectric converting region, and the trench metal layer 1 is a device separation region and a wiring line. By the trench metal layer 1, it becomes possible to obtain a semiconductor with high density without cross-talk.

Next, a process for preparing a device separation structure semiconductor structure of the above constitution is described.

i) On an insulation substrate 4' comprising sapphire, a semiconductor layer 2 comprising a photoelectric converting region (device region) is formed by epitaxial growth.

ii) Next, after formation of an oxidized film to 0.5 to 1.0 μm on the surface of the above semiconductor layer 2 by thermal oxidation, opening

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are formed internally the above semiconductor layer by resist patterning, and etching effected with the resist as the mask to form a trench. In this case, the depth of the trench is made the depth which reaches the subbing insulating substrate 4'. After completion of etching, the resist is removed.

iii) Next, by use of DMAH and hydrogen as the selective CVD method as described above, the substrate surface temperature is maintained at 270 °C, and aluminum is buried in the trench provided within the semiconductor layer 6. Here, as the metal material, aluminum is not limitative, but Al-Si, Al-Ti, etc. may be also used as mentioned above.

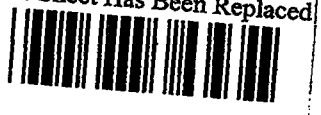
As described above, by use of the trench metal layer as the device separation region, it becomes possible to obtain a semiconductor device with high picture element density and reduced chip size without cross-talk between the picture elements.

Another preferred embodiment of the present invention has a part of the metal wiring for connecting a plurality of devices formed not on the insulating film on the semiconductor substrate but within the groove formed on the semiconductor substrate.

Example 7

Fig. 10A is a circuit diagram showing a part of the logic circuit of the CMOS constitution, and

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Fig. 10B a schematic view showing the lay-out thereof.

Thus, the power source line Vcc and the earthline GND are commonly arranged for the respective cells. In these lines, reduction of the impedance, avoidance of erroneous actuation and further avoidance of lowering in reliability by migration, etc. are particularly demanded.

Hence, by use of buried wirings in these lines, in addition to functional aspect, improvements in physical aspect such as reduction of occupied area, reduction of stepped difference, etc. can be effected.

Similarly, the buried wiring has also the effect even by use of the clock-line for transmitting the clock signals. In this case, after formation of the groove for forming such wiring in the semiconductor substrate, the whole inner surface of the groove is covered with an insulating layer. And, by depositing a semiconductor material or an electroconductive material within the groove, a subbing layer for selective deposition of a metal is formed. And, by burying a metal within the groove, the semiconductor device of the present embodiment is formed.

Fig. 11 is a schematic view for illustrating in more detail Fig. 10B, and 63 is the same invertor

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as the CMOS in Fig. 6.

Here, the line Vcc and the line GND are both buried wirings connected to the source region and the well region of the two MOSFET's, forming the common line for the both adjacent cells 61, 62.

a is the polycrystalline gate electrode which becomes the input of the invertor, out is the drain wiring which becomes the output of the invertor. In this example, as different from the prior art, the power source lines Vcc and the earthline GND are wirings of the lower layers than the gate electrode a.

In the semiconductor device of the present embodiment, since the metal wiring layer is provided within the substrate, a predetermined current tolerant capacity can be ensured by making larger the depth dimension without increasing the plan area of the metal wiring layer, and also the unevenness of the device surface can be inhibited minimum, whereby the relative movement of the wiring layer relative to the substrate can be removed to improve the precision of the formation position of the wiring layer.

Example 8

Fig. 12 and Fig. 13 are both Figures representing the characteristic portions of the wiring structures in the semiconductor devices of the present invention. Here, Fig. 12 shows the wiring

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structure constituted for the purpose of applying a positive voltage as the power source line, and Fig. 13 the wiring structure constituted for the purpose of applying a negative voltage as the earth line. These wiring structures are the embodiments of the present invention in that they are constituted on the basis of the technical thought of the present invention except that the kinds of the materials for forming the respective portions are different concerning the application method of voltage. Therefore, the constitution of the former and the preparation method thereof are described before description of the constitution and the preparation method thereof in difference from the former.

In Fig. 12, the symbol 710 is a P⁻ type semiconductor substrate comprising, for example, silicon, etc. On the surface of the substrate 710 is formed a groove 711 by conventional means such as etching, etc., and the inner surface excluding the bottom surface of the groove 711 and the surface of the substrate 710 is formed an insulation layer 712 comprising oxidized silicon, etc. formed by the thermal oxidation method or the CVD method, etc. continuously. From the bottom surface of the groove 711 to internally of the substrate 710 as described above, if necessary, an N^+ type diffusion layer 713 is provided, which is formed by thermal diffusion as

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the semiconductor region doped with an impurity of the opposite type to the conduction type of the semiconductor such as silicon forming the substrate 710.

Internally of such groove 711, a metal wiring layer 714 comprising a metal such as Al, etc. is provided. The metal wiring layer 714 may be also formed by use of a conventional method such as bias sputtering, etc., but preferably it can be also formed by use of the Al-CVD method as described below. The Al-CVD method is a film forming method with good reproducibility which can form a metal film of Al, etc. selectively on the substrate 710, namely the bottom of the groove 711 in this case without formation on the insulation layer 712 comprising silicon oxide.

The wiring film thus formed is used for connection between the predetermined electrode terminals mutually between two functional devices or, if necessary, 3 or more functional devices, to constitute an electrical circuit. For example, it may be used suitably used for connection between two source-drains of MOSFET or collectors of a bipolar transistor, or between MOSFET or a bipolar transistor and a diffusion resistance, between MOSFET or a bipolar transistor and a capacity device, etc.

Next, an example for preparing the wiring

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structure with such constitution is described.

First, as shown in Fig. 12, a P^- type silicon substrate 710 is prepared as the semiconductor substrate.

Subsequently, on the surface of the substrate 710, after application of a patterning by use of a resist, a groove 711 for formation of a wiring layer is formed by application of etching.

Then, an insulation layer 712 with a film thickness of 0.5 to 1.0 μm is formed according to the thermal oxidation method or the CVD method on the surface of the substrate 710 and the inner surface of the groove 711.

Next, after application of a patterning by use of a resist on the whole surface of the substrate 711 excluding the bottom of the groove 711, the oxidized film layer formed on the bottom of the groove 711 is removed by anisotropic etching such as RIE (reactive ion etching) to have the silicon portion of the substrate 710 exposed.

Next, at the silicon exposed portion of the bottom of the groove 711, an impurity of the type opposite to the conduction type of the material for forming the substrate 710 is doped according to the ion injection method of the thermal diffusion method, followed by diffusion to form an N^+ type diffusion layer 713.

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Subsequently, on the N^+ type diffusion layer 713, according to a conventional film forming method such as sputtering or the Al-CVD method, a metal wiring layer 714 comprising Al, etc. is formed. The metal wiring layer 714 should be desirably formed so that its upper may be coplanar with the upper surface of the insulation layer 712 formed on the surface of the substrate 710 around the groove 711 in accomplishing surface flattening of the semiconductor device. In such metal wiring layer 714, electrical separation is effected from the P^- type silicon substrate 710 through the insulation layer 712 as the insulation film formed on the inner surface of the groove 711 and the N+ type diffusion layer 713 as the P-N separation layer formed on the bottom of the groove 711.

According to the selective Al-CVD method as described above, the Al film is deposited selectively on the N^+ type diffusion layer 713 comprising silicon as described above, but not on the insulation layer 712 comprising silicon oxide. Therefore, by use of the selective Al-CVD method, there is the advantage that no patterning with resist, etc. as required in the case of a conventional film forming method such as sputtering, etc. need be applied. Also, the depth dimension of the groove 711 as described above is relatively longer than the width dimension, and even

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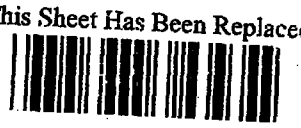
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in the case when the width dimension itself is short, there is the advantage that an Al film of good quality can be formed from the bottom of the groove 711. Therefore, it is sufficiently applicable to a fine structure with an aspect ratio of 1.0 or more as a matter of course, even 1.5 or more, further 2.0 or more. Further, because an Al film of good quality can be also formed internally of a deep groove 711 easily, the current tolerance of the metal wiring layer 714 can be easily increased by enlarging the depth dimension without enlarging the width dimension of the metal wiring layer 714.

Next, the wiring structure shown in Fig. 13 is described. In Fig. 13, the same portions as the constitution in Fig. 12 are affixed with the same symbols for brevity of the description.

In Fig. 13, the symbol 720 is an N^- type semiconductor substrate comprising, for example, silicon, as the substrate. On the surface of the substrate 720 is formed a groove 711 by conventional means such as ethcing, etc. and on the inner surface excluding the bottom internally of the groove and the surface of the substrate 720 is formed continuously an insulation film 712 comprising silicon oxide, etc. according to the thermal oxidation method or the CVD method. Internally of the substrate of the substrate 720 from the bottom of the groove 711 as described

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above, an impurity of the conduction type opposite to that of the semiconductor such as silicon, etc. for forming the substrate 720 to provide a P^+ type diffusion layer 21 as the semiconductor region formed by thermal diffusion.

Internally of such groove 711, a metal wiring layer 714 comprising a metal such as Al, etc. is provided. In such metal wiring layer 714, electrical separation is effected from the N^- type silicon substrate 720 through the insulation layer 712 as the insulation film formed on the inner surface of the groove 711 and the P-N separation layer formed on the bottom of the groove 711. Therefore, substantially no leak current from the metal wiring layer 714 to the substrate will occur.

The wiring structure of the present invention with such constitution can be utilized for all functional devices, namely field effect transistors, bipolar transistors, diffusion resistances, etc.

Fig. 14 is an example of the wiring structure of the present invention, which is a schematic sectional view showing a wiring structure of two metal layers.

In Fig. 14, the symbol 730 is an N^- type semiconductor substrate comprising, for example, silicon. On the surface of the substrate 730 is formed a groove 731 according to conventional means

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such as etching, etc., and on the inner surface excluding the bottom internally of the groove 731 and on the surface of the substrate 730 are formed continuously an oxidized film layer 732 comprising silicoin oxide, etc. according to the thermal oxidation method or the CVD method. From the bottom of the groove 731 as described above to internally of the substrate 730 is doped an impurity of the conduction type opposite to that of the semiconductor such as silicon, etc. forming the substrate 730 to provide a P^+ diffusion layer 733 formed by thermal diffusion.

Internally of such groove 731, a first wiring layer 734 comprising, for example, Al, etc. is formed according to the selective Al-CVD method as described below. The first metal wiring layer 734 has its upper surface coplanar with the surface of the substrate 730.

On a part of the oxidized film layer 732 as desc ibed above, openings 735 for taking out the electrode of the semiconductor device reaching the surface of the substrate 730 are formed.

On the surface of the oxidized film layer 732 together with the inner portion of the openings 735 and the inner portion of the groove 731 at upper portion of the first metal wiring layer 734, a second metal wiring layer 736 comprising a metal such as Al,

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etc. is formed. A passivation film 737 comprising, for example, silicon nitride, etc. is formed on the second metal wiring layer 736 and the oxidized film 732.

Referring next to Fig. 15A to Fig. 15C, a method for preparing a semiconductor device having the wiring structure with the constitution shown in Fig. 3.

First, as shown in Fig. 14A, an N^- type silicon substrate 730 is prepared.

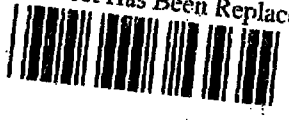
Next, after application of a patterning by use of a resist on the surface of the substrate 730, a groove 731 for formation of a first metal wiring layer is formed.

Next, an oxidized film layer 732 with a film thickness of about 0.5 to 1.0 μm is formed on the surface of the substrate 730 the inner surface of the groove 731 according to the thermal oxidation method.

Next, after application of a patterning by use of a resist on the whole surface of the substrate 730 excluding the bottom of the groove 731, the oxidized film layer formed on the groove 731 is removed by anisotropic etching of RIE (reactive ion etching) to have the silicon portion of the substrate 730 exposed.

Next, the silicon exposed portion at the bottom of the groove 731 is doped with B as the

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impurity of the conduction type opposite to that of the material for forming the substrate 730 according to the ion injection method, followed by diffusion to form a P^+ diffusion layer 733.

Next, on the P^+ type diffusion layer 733 is formed a first metal wiring layer 734 comprising Al, etc. according to the selective Al-CVD method as described above. The first metal wiring layer 734 is formed so that its upper surface became coplanar with the upper surface of the substrate 730 around the groove 731. The first metal wiring layer 734 is separated electrically from the N^- type silicon substrate 730 through the oxidized film layer 732 as the insulation film formed on the inner surface of the groove 731 and the P^+ type diffusion layer 733 as the P-N separation layer formed on the bottom of the groove 731. And, it is confirmed that there is substantially no leak of current from the first wiring layer 734 to the substrate 730.

Next, after application of a patterning by use of a resist on the surface of the oxidized film layer 732, openings 735 for taking out the electrode of the semiconductor device reaching the surface of the substrate 730 are formed in a part of the oxidized film layer 732 (Fig. 15B).

Next, internally of the openings 735 and internally of the groove 731 at the upper portion of

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the first metal wiring layer 734 is formed by depositing a second metal wiring lower layer 736a comprising Al utilizing DMAH and hydrogen as the Al-CVD method at a substrate surface temperature of 270 °C. The second method wiring lower layer 736a is formed so that its surface may be coplanar with the upper surface of the oxidized film layer 732. Next, on the respective upper surfaces of the second metal wiring lower layer 736a and at the predetermined positions on the surface of the oxidized film layer 732 are formed the upper second metal wiring layer 736b comprising Al according to the sputtering method (see Fig. 15C).

Further, on the second metal wiring layer 736 and the oxidized film layer 732, a passivation film 737 comprising silicon nitride with a film thickness of about 0.5 to 1.0 μm is formed according to the plasma CVD method to obtain a semiconductor device equipped with the metal double layer wiring structure as shown in Fig. 14.

Also in the semiconductor device with such constitution, the first metal wiring layer 734 provided internally of the N^- type silicon substrate 730 is separated from the N^- type silicon substrate 730 through the oxidized film layer 732 as the insulation film on the inner surface of the groove 731 and the P^+ type diffusion layer 733 as the P-N

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separation layer at the bottom of the groove 731, and there will be substantially no leak current from the first metal wiring layer 734 to the substrate 730. In the first metal wiring layer 734, the desired current tolerance can be ensured by enlarging the depth dimension without enlarging its flat area. Also, since the unevenness of the surface of the semiconductor device can be inhibited minimum, there is no relative movement of the first metal wiring layer 734 to the substrate 730 to effect improvement of the precision of the formation position of the first metal wiring layer 734, and also the number of the multiple layers of wiring can be increased within the range of a limited thickness of the device. Further, since no interlayer insulation film is required between the first metal wiring layer and the second metal wiring layer, the surface stepped difference can be reduced in the case of providing wiring layers of the third metal wiring layer et seq, whereby reliability of the wiring layers of the third layer et seq can be improved.

As described above, according to the present invention, a wiring structure capable of ensuring necessary current tolerance can even with a small wiring flat area and also capable of being formed at a high positional precision can be obtained.

The film forming method suitable for the

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present invention is to form a deposited film by the surface reaction on an electron-donative substrate by use of a gas of an alkylaluminum hydride and hydrogen gas (hereinafter called the Al-CVD method).

Particularly, by use of monomethylaluminum hydride (MMAH) as the starting gas or dimethylaluminum hydride (DMAH) as the starting gas, and H_2 gas as the reaction gas, and heating the substrate surface under the mixture of these gases, an Al film of good quality can be deposited. Here, during the selective deposition of Al, it is preferable to maintain the surface temperature at the decomposition temperature of the alkylaluminum hydride or higher and less than 450 °C, more preferably 260 °C to 440 °C.

As the method for heating the substrate to the above-mentioned temperature range, there are direct heating and indirect heating. Particularly, by maintaining the substrate at the above-mentioned temperature by direct heating, an Al film of good quality can be formed at high deposition speed. For example, when the substrate surface temperature during Al film formation is made 260 °C to 440 °C which is more preferable temperature range, a film of good quality can be obtained at higher deposition speed of 300 Å to 5000 Å/min. which is higher than in the case of resistance heating. As such direct

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heating method (substrate itself is heated by direct transmission of the energy from the heating means to the substrate), for example, lamp heating by means of halogen lamp, xenon lamp, etc. may be included. As the method for indirect heating, there is resistance heating, by which heating can be performed by use of a heat-generating body, etc. provided at the substrate supporting member for supporting the substrate to form deposited film arranged in the space for formation of the deposited film.

By applying the CVD method to the substrate having the electron-donative surface portion and the non-electron donative surface portion co-present thereon, a single crystal of Al is formed under good selectivity only on the electron-donative substrate surface portion. The Al thus formed will have all of excellent characteristics desirable for the electrode/wiring material. That is, reduction of generation probability of hillock, reduction of generation probability of alloy spike will be accomplished.

This may be considered to be due to the fact that substantially no or extremely small formation of alloy spike, etc. on account of the eutectic reaction with the subbing silicon, etc. is seen, because Al of good quality can be formed on the surface comprising a semiconductor or an electro-conductive

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member as the electron-donative surface, and also the Al is excellent in crystallinity. And, when employed for the electrode of a semiconductor device, an effect surpassing the concept of the Al electrode which has been contemplated in the prior art, and could not be even expected in the prior art can be obtained.

Having described above about the fact that the Al deposited on an electron-donative surface, for example, within the opening with the semiconductor substrate surface exposed becomes to have a single crystalline structure, according to the Al-CVD method, a metal film composed mainly of Al as described below can be also selectively deposited, and its film quality also exhibits excellent characteristics.

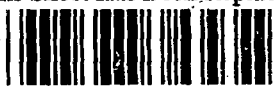
For example, in addition to a gas of an alkylaluminum hydride and hydrogen,

a gas containing Si atoms such as SiH_4, Si_2H_6, Si_3H_8, $Si(CH_3)_4$, $SiCl_4$, SiH_2Cl_2, $SiHCl_3$, or the like.

a gas containing Ti atoms such as $TiCl_4$, $TiBr_4$, $Ti(CH_3)_4$, etc.,

a gas containing Cu atoms such as copper bisacetylacetonate $Cu(C_5H_7O_2)$, copper bisdipivaloylmethanite $Cu(C_{11}H_{19}O_2)_2$, copper bishexafluoroacetylacetonate $Cu(C_5HF_6O_2)_2$, etc.

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may be introduced in a suitable combination to form a gas mixture atmosphere, thereby forming an electrode by selective deposition of an electroconductive material such as Al-Si, Al-Ti, Al-Cu, Al-Si-Ti, Al-Si-Cu, etc.

The Al-CVD method as described above is a film forming method excellent in selectivity, and also the surface characteristic of the film formed has good surface characteristic. Hence, by application of a non-selective film forming method to the next deposition step, Al or a metal film composed mainly of Al can be also formed on the Al film selectively deposited as described above and SiO_2, etc. as the insulating film, whereby a suitable metal film having high useability for general purpose as the wiring of semiconductor device can be obtained.

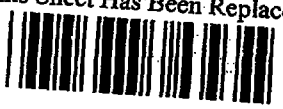
Specific examples of such metal film include the following. There may be included combinations of Al, Al-Si, Al-Ti, Al-Cu, Al-Si-Ti, Al-Si-Cu, etc. deposited selectively with Al, Al-Si, Al-Ti, Al-Cu, Al-Si-Ti, Al-Si-Cu, etc.

As the film forming method for non-selective deposition, there are other CVD methods than the Al-CVD method as described above, the sputtering method, etc.

(Film Forming Apparatus)

Next, a suitable film forming apparatus for

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forming the electrode according to the present invention is described.

Fig. 16 to Fig. 18 show schematically a sequential metal film forming apparatus suitable for applying the film forming method as described above.

The sequential metal film forming apparatus, as shown in Fig. 16, is constituted of loadlock chamber 311 connected mutually communicated under shielding from outer air through the gate valves 310a to 310f, a CVD reaction chamber 312 as the first film forming chamber, an Rf etcing chamber 313, a sputtering chamber 314 as the second film forming chamber and a loadlock chamber 315, and the respective chambers are constituted reducible in pressure by evacuation with the evacuation systems 316a to 316e. Here, the above loadlock chamber 311 is a chamber for replacing the substrate atmosphere before deposition treatment with H_2 atmosphere after evacuation in order to improve the throughput characteristic. The next CVD reaction chamber 312 is a chamber for selective deposition on the substrate according to the Al-CVD method as described above under normal pressure or reduced pressure, in which a substrate holder 318 having a heat-generating member 317 which can heat the substrate to be formed to a range of 200 °C to 450 °C is provided internally, and starting gases such as alkylaluminum

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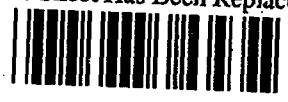


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hydride bubbled and gasified in the bubbler 319-1 are introduced into the chamber through the starting gas introducing line 319 for CVD, and also hydrogen gas as the reactive gas is introduced through the gasline 319'. The next Rf etching chamber 313 is a chamber for carrying out cleaning of the substrate surface after selective deposition (etching) under Ar atmosphere, and internally thereof are provided at least a substrate holder 320 capable of heating the substrate to a range of 100 °C to 250 °C and an electrode line for Rf etching 321, and also an Ar gas feeding line 322 is connected. The next sputtering chamber 314 is a chamber for depositing non-selectively a metal film by sputtering under Ar atmosphere on the substrate surface, and internally thereof are provided a substrate holder 323 heated within a range of 200 °C to 250 °C and a target electrode 324 for mounting a sputter target material 324a, and also an Ar gas feeding line 325 is connected. The final loadlock chamber 315 is a control chamber before taking out the substrate after completion of the metal film deposition into the outer air, and constituted so that the atmosphere may be replaced with N_2.

Fig. 17 shows another constitutional example of a sequential metal film forming apparatus suitable for applying the film forming method as described

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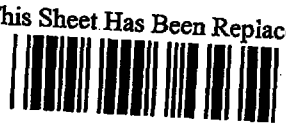
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above, and the same portions as described above in Fig. 16 are made the same symbols. The difference of the apparatus in Fig. 17 from that in Fig. 16 resides in that a halogen lamp 330 is provided as the direct heating means and the substrate surface can be directly heated, and for that purpose, the substrate holder 312 is provided with a nail 331 for holding the substrate under suspended state.

By heating directly the substrate surface with such constitution, the deposition speed can be further improved as described above.

The sequential metal film forming apparatus with the above constitution, as shown in Fig. 18, is substantially equivalent to one with the structure having the above loadlock chamber 311, the CVD reaction chamber 312, the Rf etching chamber 313, the sputtering chamber 314, the loadlock chamber 315 connected mutually to one another with the conveying chamber 326 as the relay chamber. With this constitution, the loadlock chamber 311 functions also as the loadlock chamber 315. In the above conveying chamber 326, as shown in the Figure, an arm 327 as the conveying means reversibly rotatable in the AA direction and stretchable in the BB direction is provided, and with the arm 327, as shown in the arrowhead in Fig. 19, the substrate can be moved following the steps successively from the loadlock

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chamber 311 to the CVD chamber 312, the Rf etching chamber 313, the sputtering chamber 314, the loadlock chamber 315 without exposure to outer air.

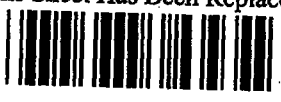
(Film Forming Procedure)

The film forming procedure for forming the electrode and wiring according to the present invention is described.

Fig. 20 is a schematic perspective view for illustration of the film forming procedure for formation of the electrode and wiring according to the present invention.

First, the outline is described. A semiconductor substrate having openings formed on an insulating film is prepared, which substrate is arranged in a film forming chamber, and its surface is maintained at, for example, 260 °C to 450 °C to deposit selectively Al at the portion where the semiconductor is exposed according to the hot CVD method in a mixed atmosphere of DMAH as the alkylaluminum hydride and hydrogen gas. Of course, as described above, a metal film composed mainly of Al such as Al-Si, etc. may be also deposited selectively by introducing a gas containing Si atoms, etc. Next, on the Al selectively deposited by the sputtering method and the insulating film, Al or a metal film composed mainly of Al is non-selectively formed. Then, by patterning of the metal film

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non-selectively deposited to a desired wiring shape, electrodes and wirings can be formed.

Referring next to Fig. 17 to Fig. 20, description is made in more detail. First, a substrate is prepared. As the substrate, for example, a single crystalline Si wafer having an insulating film provided with openings with respective apertures provided thereon is prepared.

Fig 20A is a schematic view showing a part of the substrate. Here, 401 is a single crystalline silicon substrate as a conductive substrate, 402 a thermally oxidized silicon film as the insulating film (layer). 403 and 404 are openings (exposed portions), having apertures different from each other. 410 is the groove bottom with Si exposed.

The procedure for forming Al film which becomes the electrode as the first wiring layer on the substrate is as follows with Fig. 20.

First, the substrate as described above is arranged in the loadlock chamber 311. Hydrogen is introduced into the loadlock chamber 311 to make it under hydrogen atmosphere. And, the reaction chamber 312 is internally evacuated to approximately 1×10^{-8} Torr by the evacuation system 316b. However, Al film can be formed even if the vacuum degree within the reaction chamber 312 may be worse than 1×10^{-8} Torr.

And, the gas of DMAH bubbled from the gas

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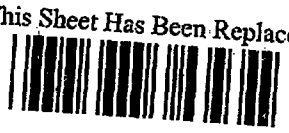
line 319 is fed. For the carrier gas for the DMAH line, H_2 is employed.

The second gas line 319' is for H_2 as the reaction gas, and by flowing H_2 through the second gas line 319' and controlling the opening degree of the slow leak valve not shown to adjust the pressure within the reaction chamber 312 to a predetermined value. A typical pressure in this case is preferably about 1.5 Torr. Through the DMAH line, DMAH is introduced into the reaction tube. The total pressure is made about 1.5 Torr, and the DMAH pressure 5.0×10^{-3} Torr. Then, current is passed to the halogen lamp 330 to heat directly the wafer. Thus, Al is selectively deposited.

After elapse of a predetermined deposition time, feeding of DMAH is once stopped. The predetermined deposition time of the Al film deposited in this process is the time until the thickness of the Al film on the Si (single crystalline silicon substrate 1) becomes equal to the film thickness of the SiO_2 (thermally oxidized silicon film 2), and can be determined previously by experimentation.

The temperature of the substrate surface by direct heating at this time is made about 270 °C. According to the steps up to this stage, the Al film 405 is selectively deposited within the openings and

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the grooves as shown in Fig. 20B.

All of the steps as described above are referred to as the first film forming step for formation of electrode within contact hole.

After the above first film forming step, the CVD reaction chamber 312 is evacuated until reaching a vacuum degree of 5×10^{-3} Torr or lower by the evacuation system 316b. At the same time, the Rf etching chamber 313 is evacuated to 5×10^{-6} Torr or lower. After confirmation that the both chambers have reached the above vacuum degree, the gate valve 310c is opened, the substrate moved from the CVD reaction chamber 312 to the Rf etching chamber 313 by the conveying means, and the gate valve 310c closed. The substrate is conveyed to the Rf etching chamber 313, and the Rf etching chamber 313 is evacuated by means of the evacuation system 316c until reaching a vacuum degree of 10^{-6} Torr or lower. Then, argon is fed through the argon feeding line 322 for Rf etching, and the Rf etching chamber 131 maintained under an argon atmosphere of 10^{-1} to 10^{-3} Torr. The substrate holder 320 of Rf etching is maintained at about 200 °C, Rf power of 100 W supplied to the electrode for Rf ethcing 321 for about 60 seconds, and discharging of argon is caused to occur within the Rf etching chamber 313 for about 60 seconds. By doing so, the surface of the

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substrate can be etched with argon ions to remove unnecessary surface layer of the CVD deposited film. The etching depth in this case is made about 100 Å in terms of the oxide. Here, surface etching of the CVD deposited film is effected in the Rf etching chamber, but since the surface layer of the CVD film of the substrate conveyed through vacuum contains no oxygen, etc., no Rf etching may be effected. In that case, the Rf etching chamber 313 function as the temperature changing chamber for effecting temperature change within a short time, when the temperatures in the CVD reaction chamber 12 and the sputtering chamber 314 are greatly different.

In the Rf etching chamber 313, after completion of Rf etching, flowing of argon is stopped, and the argon within the Rf etching chamber 313 is evacuated. After the Rf etching chamber 313 is evacuated to 5×10^{-6} Torr and the sputtering chamber 314 to 5×10^{-6} Torr or lower, the gate valve 310d is opened. Then, the substrate is moved from the Rf etching chamber 313 to the sputtering chamber 314 by means of a conveying means, followed by closing of the gate valve 310d.

After the substrate is conveyed to the sputtering chamber 314, the sputtering chamber 314 is made under an argon atmosphere of 10^{-1} to 10^{-3} Torr similarly as in the Rf etching chamber 313, and the

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temperature of the substrate holder 323 for mounting the substrate set to about 200 to 250 °C. And discharging of argon is effected at a DC power of 5 to 10 KW to cut a target material such as Al or Al-Si (Si: 0.5 %) and effect film formation of a metal such as Al, Al-Si, etc. at a deposition speed of about 10000 Å/min. on the substrate. This step is a non-selective deposition step. This is called the second film forming step for formation of the wiring to be connected to the electrode.

After formation of a metal film of about 5000 Å, flowing of argon and application of DC power are stopped. After evacuation of the loadlock chamber 311 to 5×10^{-3} Torr or lower, the gate valve 310e is opened and the substrate moved. After the gate valve 310e is closed, N_2 gas is permitted to flow into the loadlock chamber 311 until reaching atmospheric pressure, the gate valve 310f opened and the substrate taken out of the apparatus.

According to the second Al film deposition step as described above, the Al film 406 can be formed on the SiO_2 film 402.

And, by patterning the Al film 406 as shown in Fig. 20D, a wiring with a desired shape can be obtained.

(Experimental Examples)

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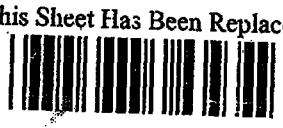
above-described Al-CVD method is and how good of the quality the Al film deposited within the openings is are described based on the experimental results.

First, as the substrate, a plurality of N-type single crystalline silicon wafers were prepared, which are thermally oxidized on the surface to form SiO_2 of 8000 Å, and have various openings with various apertures from 0.25 μm x 0.25 μm square to 100 μm x 100 μm square patterned to have the subbing Si single crystal exposed (Sample 1-1).

These are subjected to formation of Al films according to the Al-CVD method under the conditions as described below. Under the common conditions by use of DMAH as the starting gas, and hydrogen as the reaction gas, a total pressure of 1.5 Torr, a DMAH partial presure of 5.0×10^{-3} Torr, the power amount passed through the halogen lamp is adjusted and the substrate surface temperature set within the range of 200 °C to 490 °C to form films.

The results are shown in Table 1.

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Table 1

	200	230	250	260	270	280	300	350	400	440	450	460	470	480	490
Substrate surface temperature(°C)															
Deposition speed (Å/min)		1000 - 1500						3000 - 5000							
Line defect of Si				Not recognized											
Carbon content				Not detected											
Resistivity (Ω μcm)		2.7 - 3.3						2.8 - 3.4							
Reflectance (%)		85 - 95						90 - 95					- 60		
Hillock density of 1 μm or more		$1 - 10^2$						0 - 10					$10 - 10^4$		
Spike generation (destruction probability of 0.15 μm junction)		0											0 - 30		

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As can be seen from Table 1, at a substrate surface temperature by direct heating of 260 °C or higher, Al is deposited selectively at a high deposition speed of 3000 to 5000 Å/min. within the openings.

When the characteristics of the Al film within the openings at substrate surface temperature range of 260 °C to 440 °C are examined, they are found to be excellent such that no carbon is contained, with resistivity being 2.8 to 3.4 μΩcm, reflectance 90 to 95 %, hillock density of 1 μm or higher 0 to 10 and substantially no spike generation (destruction probability of 0.15 μm junction).

In contrast, at substrate surface temperatures of 200 °C to 250 °C, the film is found to be considerably good as compared with the prior art although the film quality is slightly worse as compared with the case of 260 °C to 440 °C, but the deposition speed is 1000 to 1500 Å/min., which can never be said to be sufficiently high.

When the substrate surface temperature becomes 450 °C or higher, the characteristics of the Al film with the openings are lowered with the reflectance becoming 60 % or less, hillock density of 1 μm or more 10 to 10^4 cm^{-2}, alloy spike generation 0 to 30 %.

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the method as described above can be used openings such as contact hole or thru-hole.

That is, it can be also preferably applied to the contact hole/thru-hole structure comprising the material as described below.

On the Sample 1-1 as described above, an Al film is formed on a substrate (sample) as described below under the same conditions as when the Al film is formed.

On a single crystalline silicon as the first substrate surface material is formed a silicon oxide film according to the CVD method as the second substrate surface material, and patterning effected according to the photolithographic steps to have the single crystalline silicon surface partially exposed.

The film thickness of the thermally oxidized SiO_2 film has a film thickness of 8000 Å, the exposed portion of the single crystalline silicon a size of 0.25 μm x 0.25 μm to 100 μm x 100 μm. Thus, Sample 1-2 is prepared (hereinafter such samples are represented as "CVD SiO_2 (hereinafter abbreviated as SiO_2)/single crystalline silicon").

Sample 1-3 is boron doped oxide film formed by normal pressure CVD (hereinafter abbreviated as BSG)/single crystalline silicon,

Sample 1-4 phosphorus doped oxide film formed by normal pressure CVD (hereinafter abbreviated as

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PSG)/single crystalline silicon,

Sample 1-5 phosphorus and boron doped oxide film formed by normal pressure CVD (hereinafter abbreviated as BSPG)/single crystalline silicon,

Sample 1-6 nitride film formed by plasma CVD (hereinafter abbreviates as P-SIN)/single crystalline silicon,

Sample 1-7 hot nitride film (hereinafter abbreviated as T-SiN)/single crystalline silicon,

Sample 1-8 nitride film formed by low pressure CVD (hereinafter abbreviated as LP-SiN)/ single crystalline silicon,

Sample 1-9 nitride film formed by means of an ECR apparatus (hereinafter abbreviated as ECR-SiN)/ single crystalline silicon.

Further, according to all combinations of the first substrate surface materials (18 kinds) and the second substrate surface materials (9 kinds), Samnples 1-11 to 1-179 (note: Sample Nos. 1-10, 20, 30, 40, 50, 60, 70, 80, 90, 100, 110, 120, 130, 140, 150, 160, 170 are lacking) are prepared. As the first substrate surface material, single crystalline silicion (single crystalline Si), polycrystalline silicon (polycrystalline Si), amorphous silicon (amorphous Si), tungsten (W), molybdenum (Mo), tantalum (Ta), tungsten silicide (WSi), titanium silicide (TiSi), aluminum (Al), aluminum silicon

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(Al-Si), titanium aluminum (Al-Ti), titanium nitride (Ti-N), copper (Cu), aluminum silicon copper (Al-Si-Cu), aluminum palladium (Al-Pd), titanium (Ti), molybdenum silicide (Mo-Si), tantalum silicide (Ta-Si) are employed. As the second substrate surface material, T-SiO_2, SiO_2, BSG, PSG, BPSG, P-SiN, T-SiN, LP-SiN, ECR-SiN are employed. For all of the samples as described above, good Al films comparable with the Sample 1-1 could be formed.

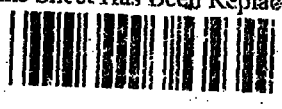
Next, on the substrate having Al deposited selectively as described above, Al is deposited non-selectively according to the sputtering method as described above, followed by patterning.

As the result, the Al film formed according to the sputtering method, and the Al film selectively selected within the openings are found to be under the contact state with both electrically and mechanically high durability due to good surface characteristic of the Al film.

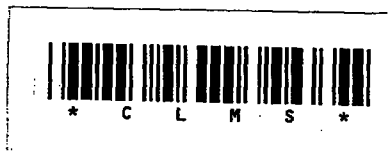
(Experimental Examples)

Samples of semiconductor device are trially made according to the methods as described in Examples 1 to 8, and as the result of experimentation, good characteristics as expected can be obtained.

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WHAT IS CLAIMED IS:

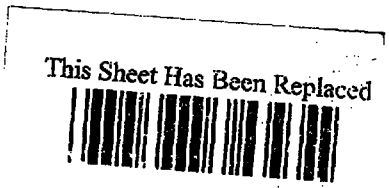
1. A semiconductor device having a device region and a device separation region formed on a semiconductor substrate doped with impurities, and the device separation region having a metal wiring formed on the surface of said device region or the back surface of said substrate,

characterized in that an aluminum region extending in the longitudinal direction connected to said metal wiring is formed within said device separation region.

2. A semiconductor device having device separation region, which device having a device region and a metal region composed mainly of aluminum which becomes the device separation region extending out in the longitudinal direction formed on an insulating substrate, one end of the metal region being in contact with said insulating substrate and the other end with the surface exposed.

3. A semiconductor device according to Claim 1, wherein said semiconductor device is a solid image pick up device.

4. A semiconductor device, comprising a semiconductor substrate having at least two



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functional devices, and having a buried metal wiring layer for connecting said at least two functional devices provided internally of said semiconductor substrate.

5. A semiconductor device according to Claim 4, wherein further at least one metal wiring layer is laminated on said metal wiring layer.

6. A semiconductor device according to Claim 4, wherein the metal wiring layer provided within said semiconductor substrate is formed of a single crystalline aluminum.

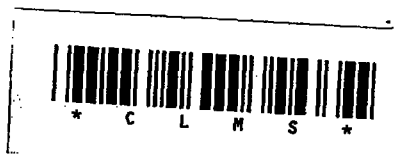
7. A semiconductor device according to Claim 6, wherein said semiconductor substrate and the metal wiring layer provided within said substrate are electrically separated with a layer region of the conduction type opposite to that of said substrate.

8. A semiconductor device according to Claim 4, wherein said semiconductor device includes a logic circuit.

9. A semiconductor device according to Claim 2, wherein said semiconductor device is a solid image pick up device.

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10. A semiconductor device according to Claim 5, wherein the metal wiring layer provided within said semiconductor substrate is formed of a single crystalline aluminum.

11. A semiconductor device, comprising a plurality of active regions each separated one from the other by a device separation region, which device is characterised in that:

each device separation region is provided with a metal or metallic filling.

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ABSTRACT

DEVICE SEPARATION STRUCTURE AND SEMICONDUCTOR DEVICE IMPROVED IN WIRING STRUCTURE

A semiconductor device has a device region, and a device separation region formed on a semiconductor substrate doped with impurities. And, the device separation region has a metal wiring formed on the surface of the device region or the back surface of the substrate. An aluminum region extending in the longitudinal direction connected to the metal wiring is formed within the device separation region.

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FIG. 1A
PRIOR ART

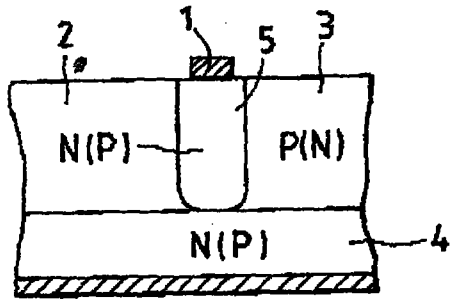


FIG. 1B
PRIOR ART

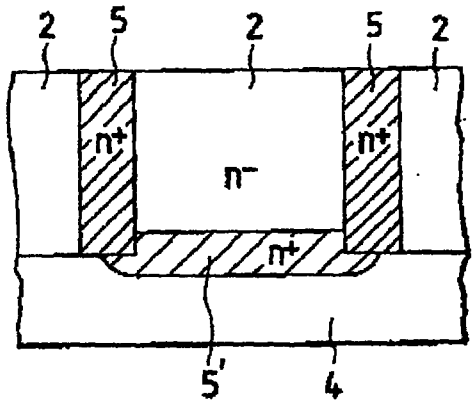


FIG. 2A
PRIOR ART

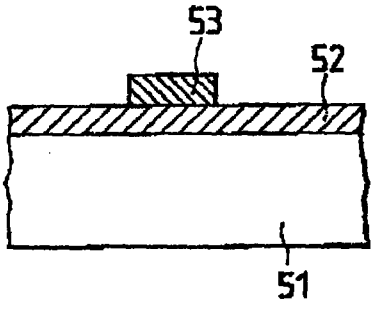
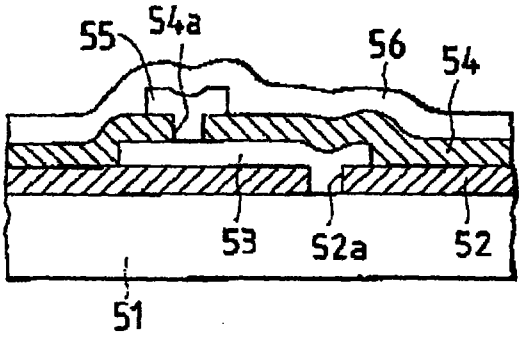


FIG. 2B
PRIOR ART



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FIG. 3

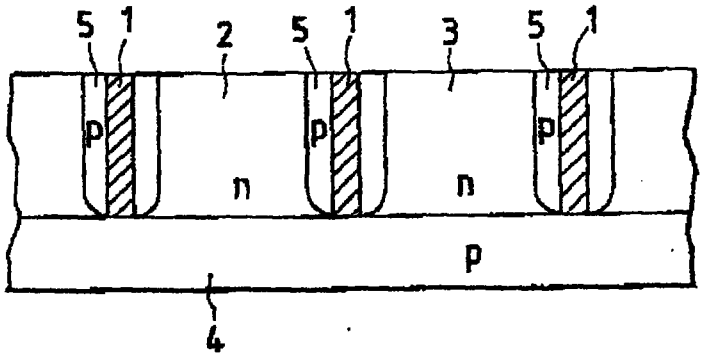


FIG. 4

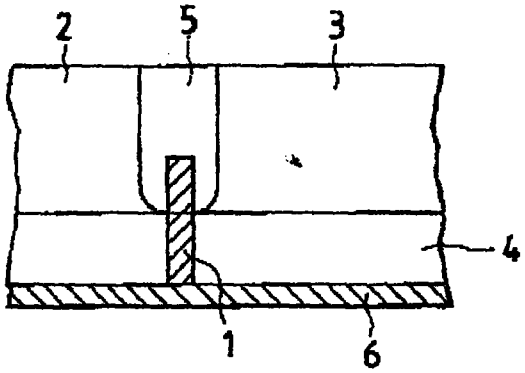
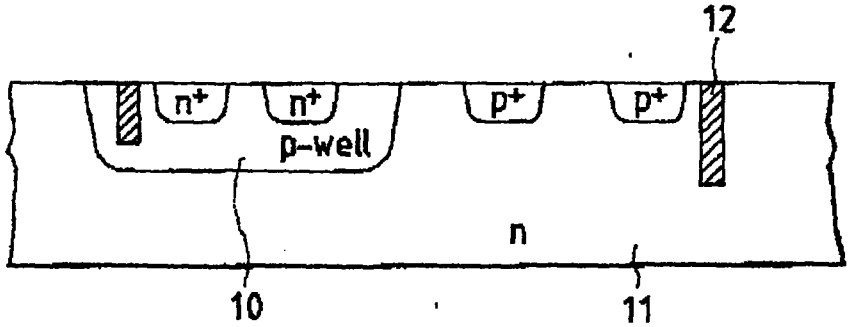


FIG. 5



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FIG. 6A

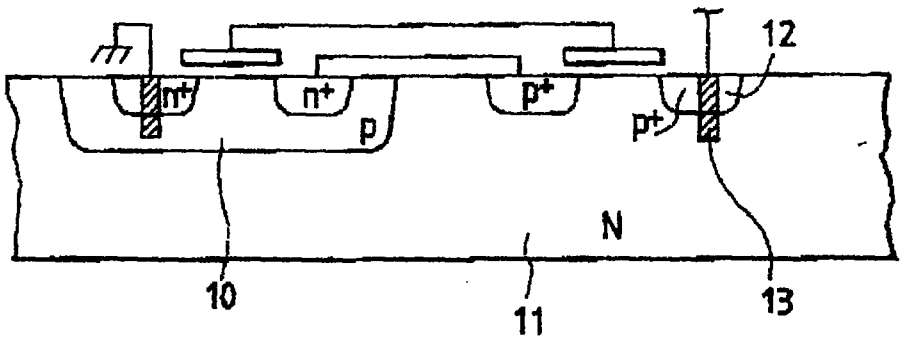
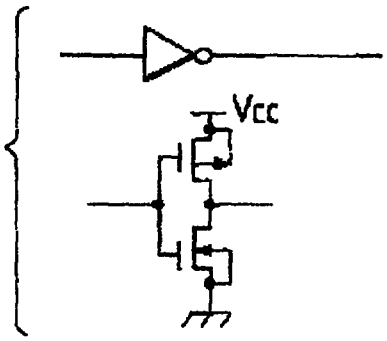


FIG. 6B



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FIG. 7A

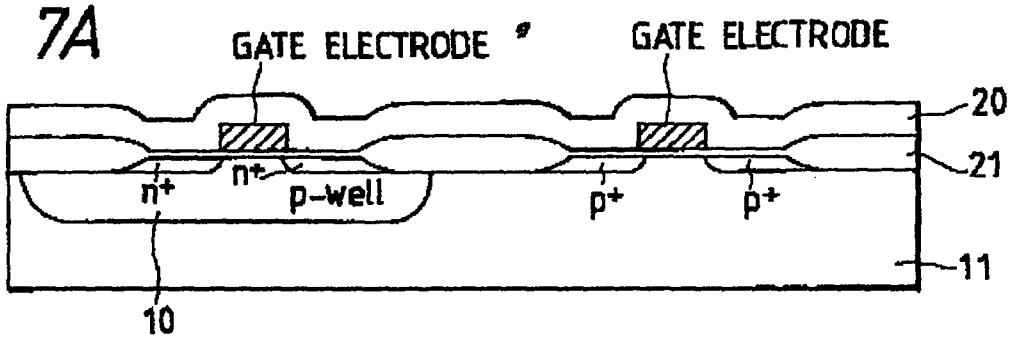


FIG. 7B

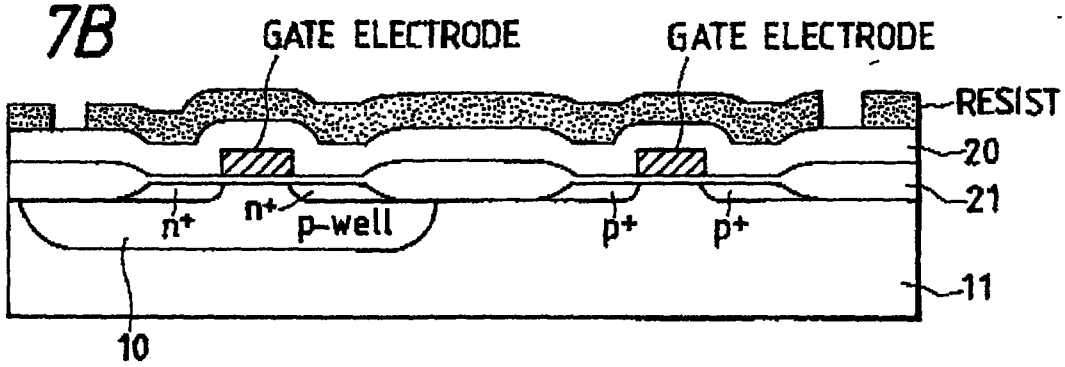


FIG. 7C

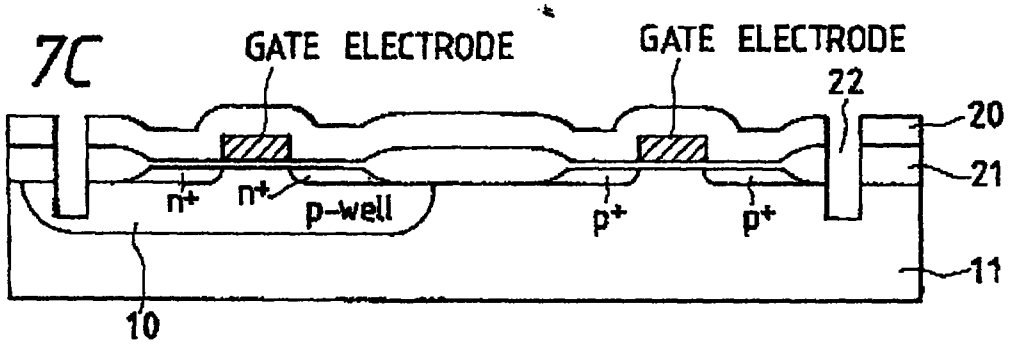
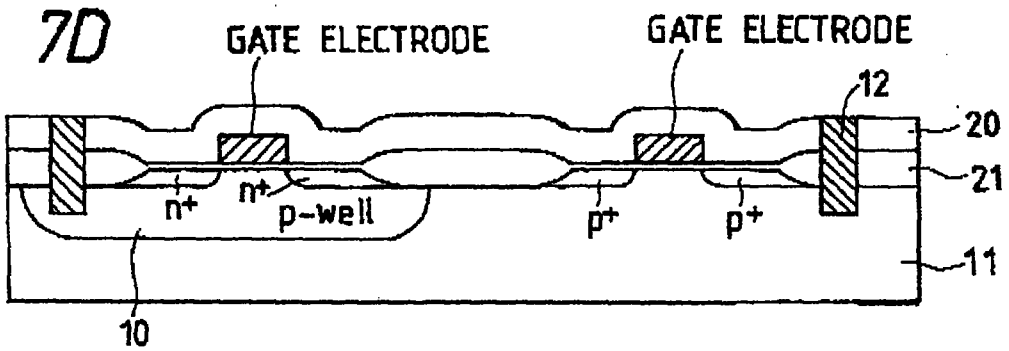
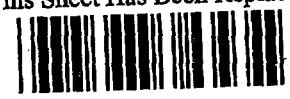


FIG. 7D



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FIG. 8

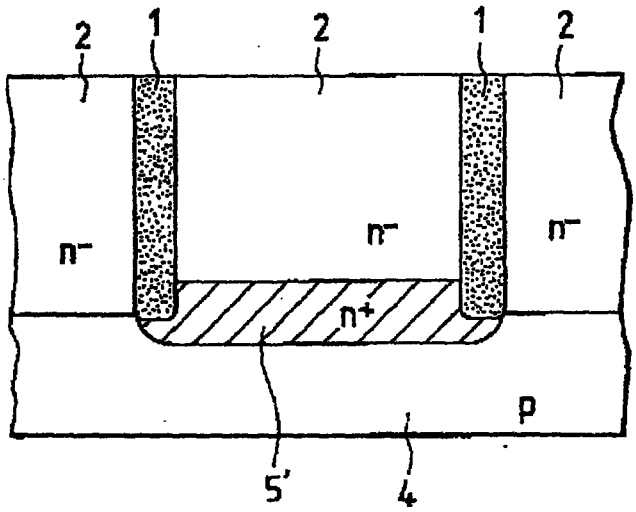
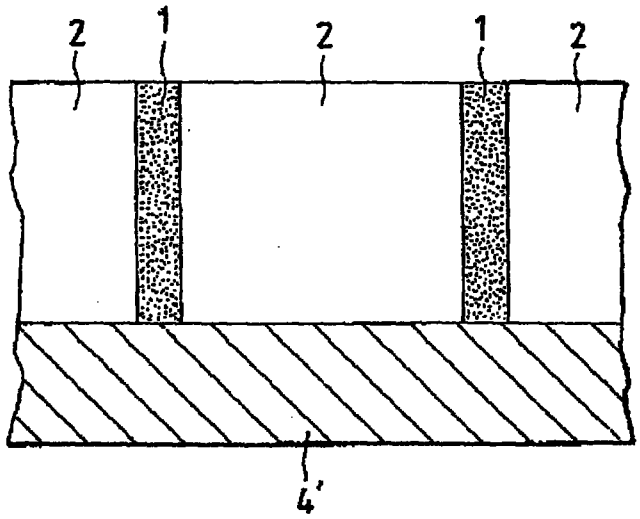


FIG. 9



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FIG. 10A

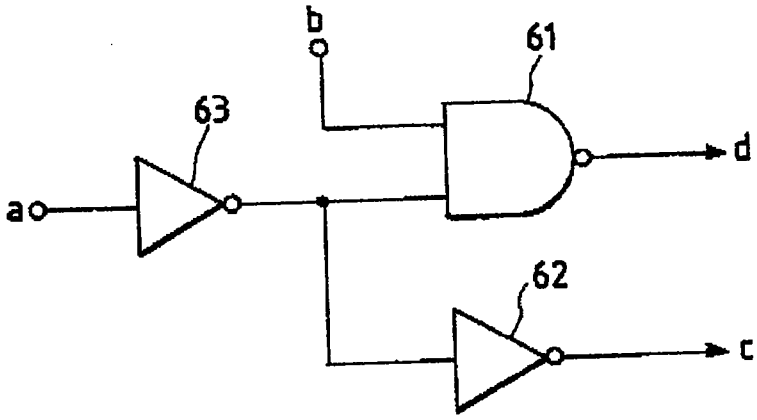
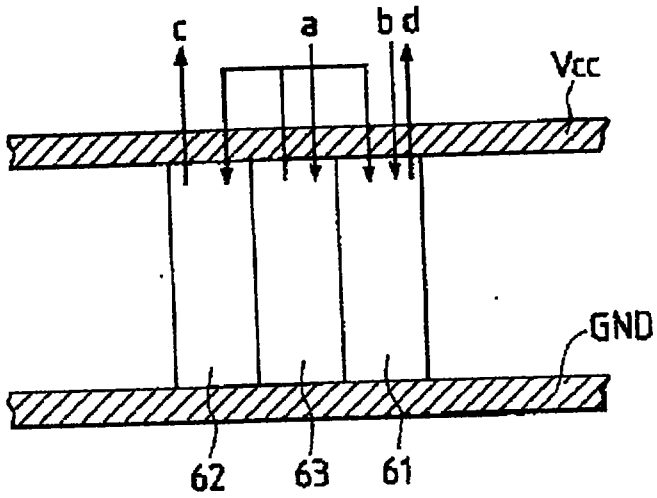


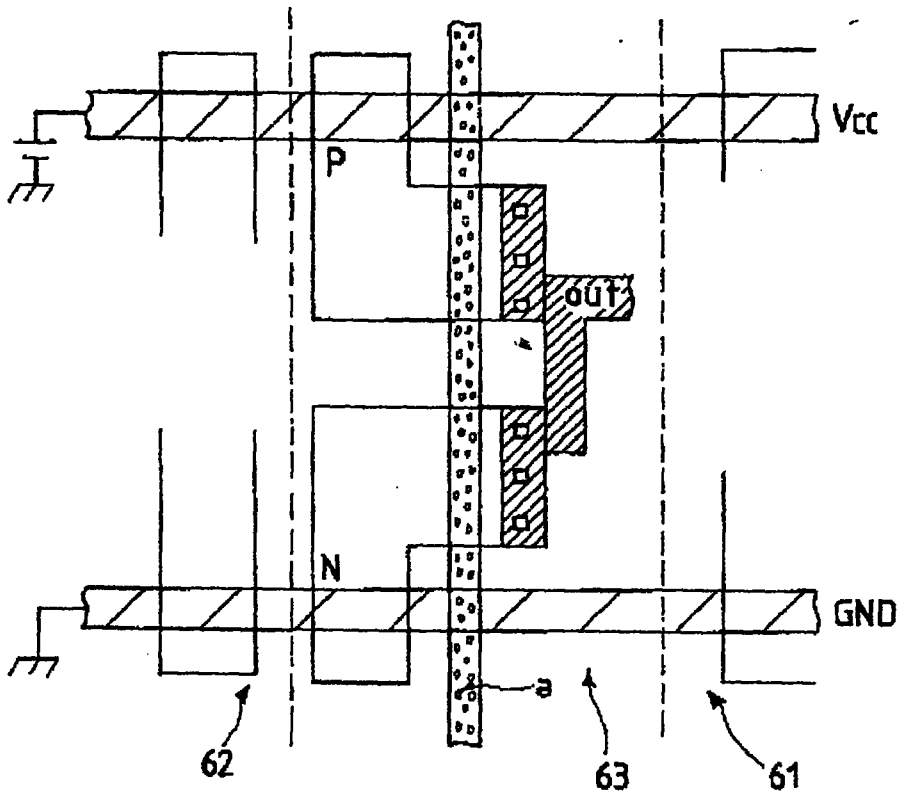
FIG. 10B



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FIG. 11



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FIG. 12

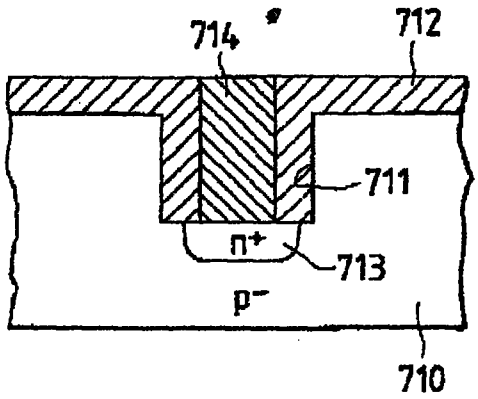


FIG. 13

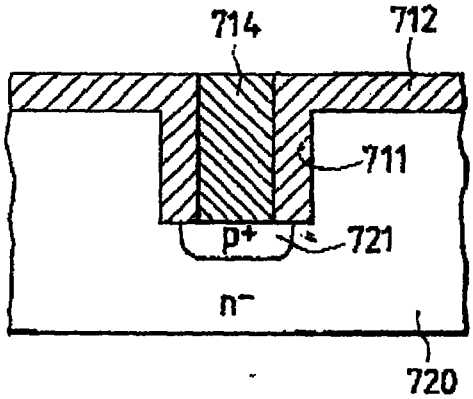
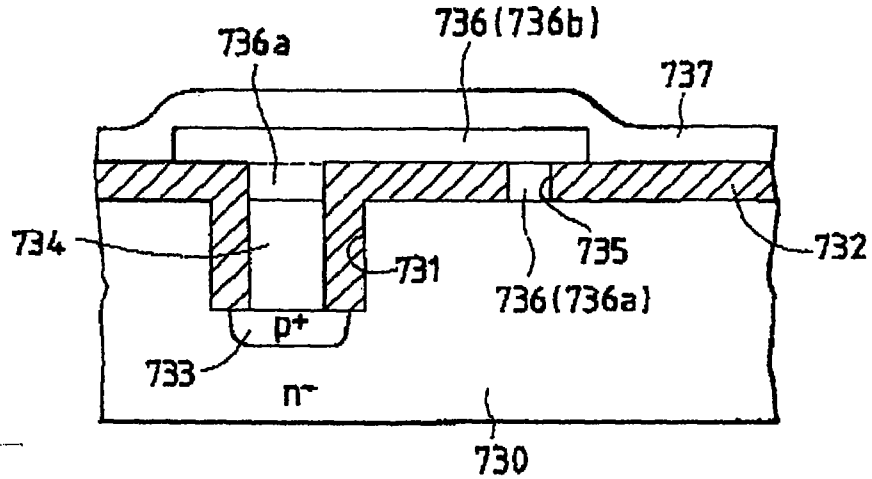


FIG. 14



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FIG. 15A

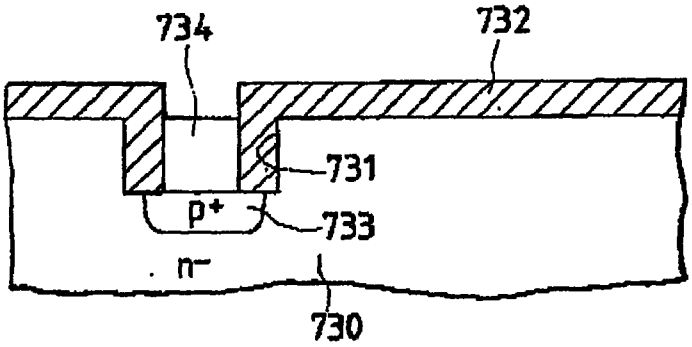


FIG. 15B

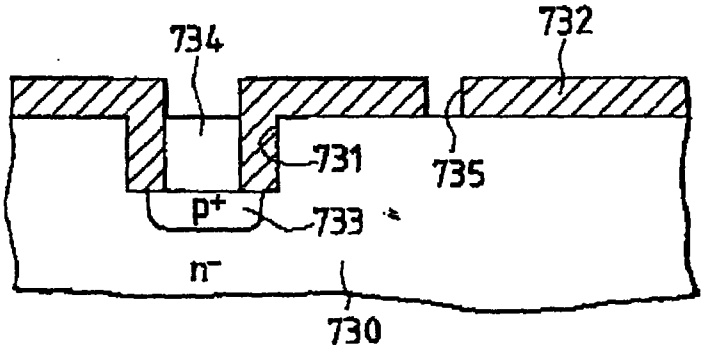
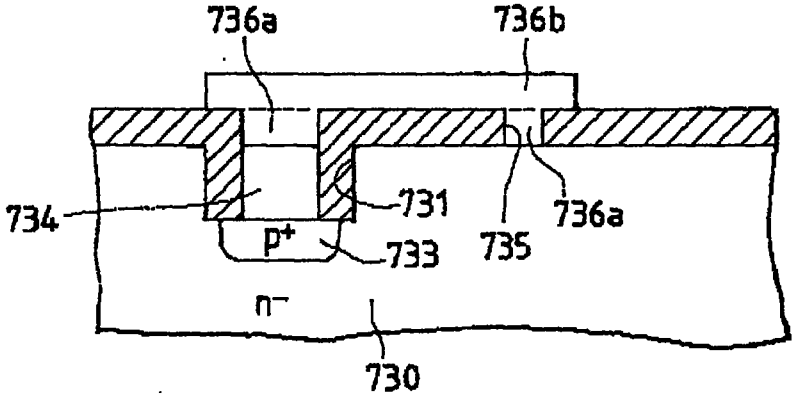


FIG. 15C



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FIG. 16

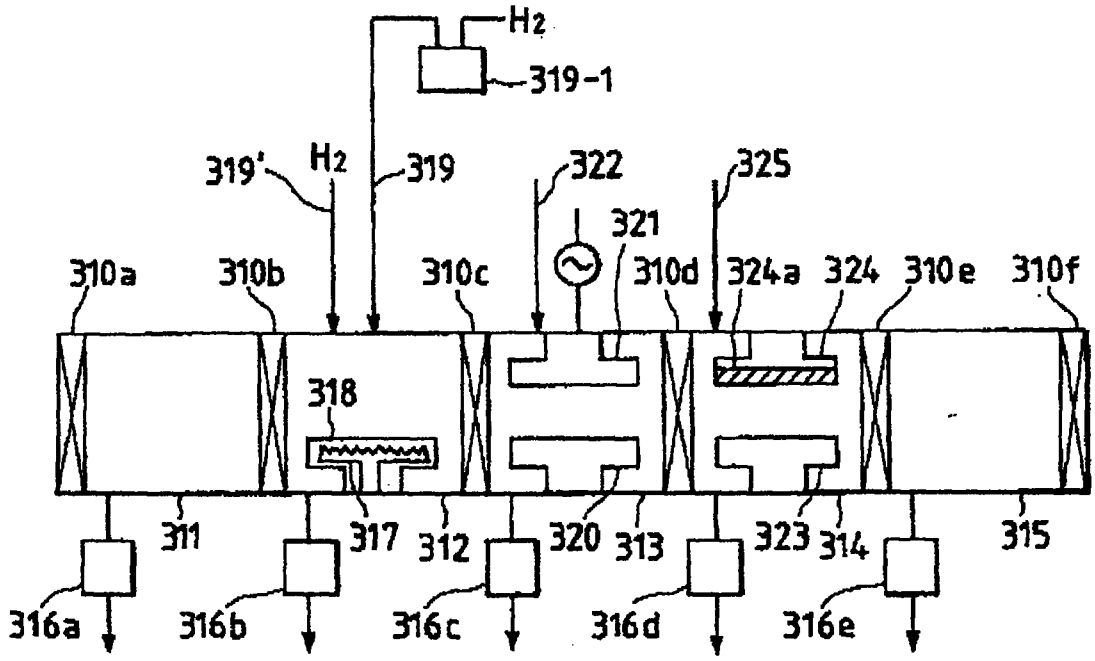
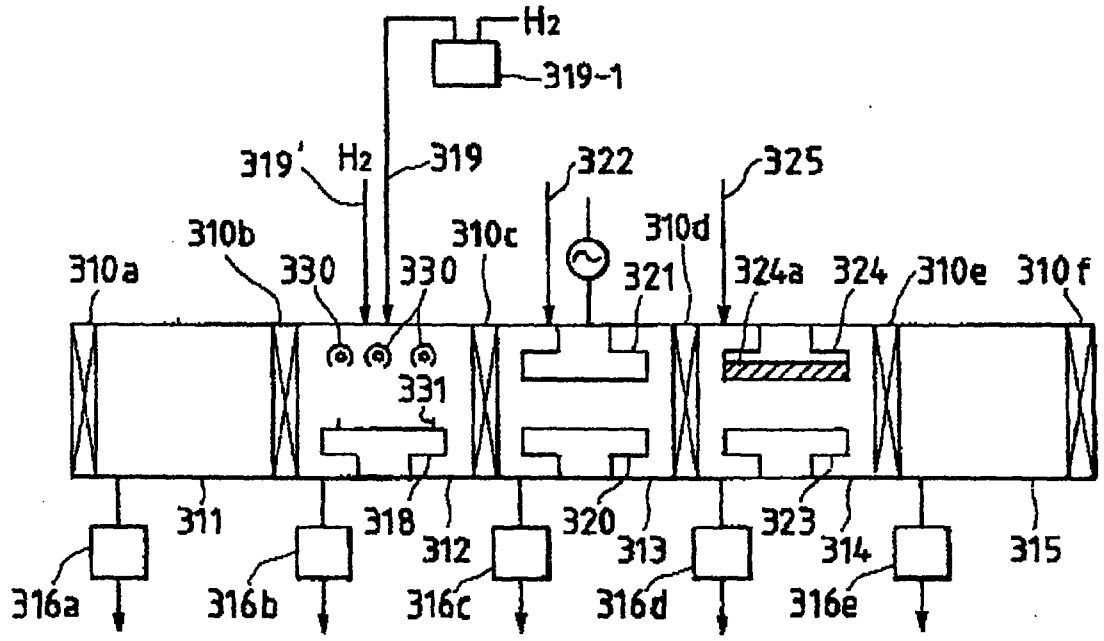


FIG. 17



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FIG. 18

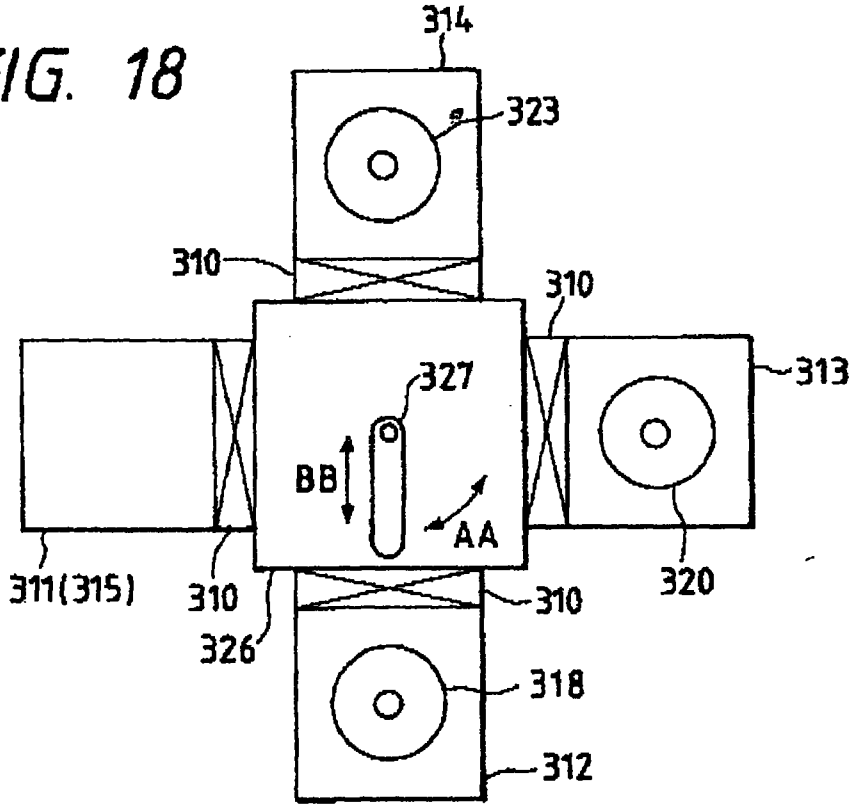
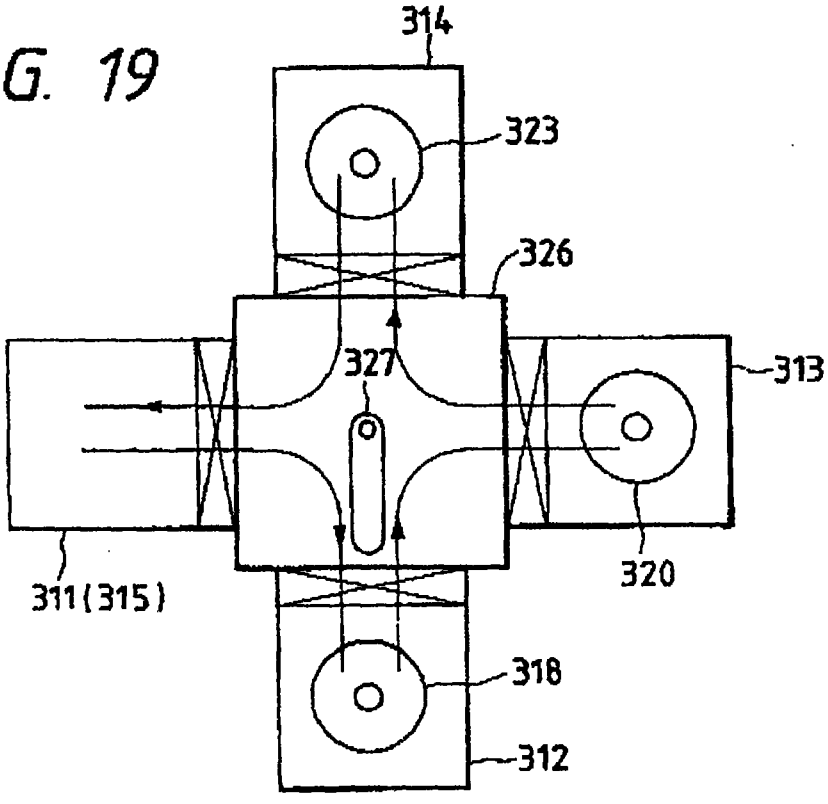


FIG. 19



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FIG. 20A

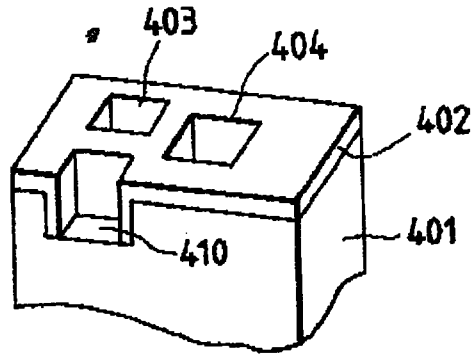


FIG. 20B

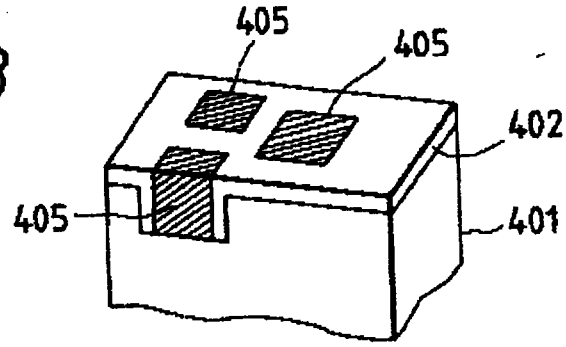


FIG. 20C

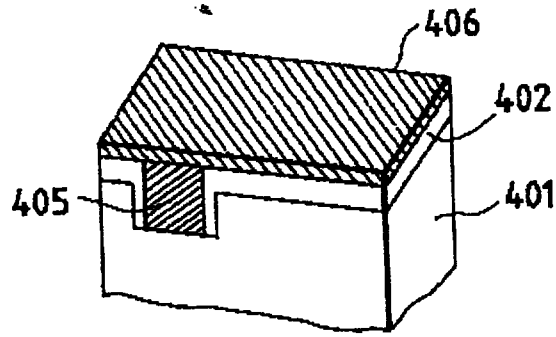
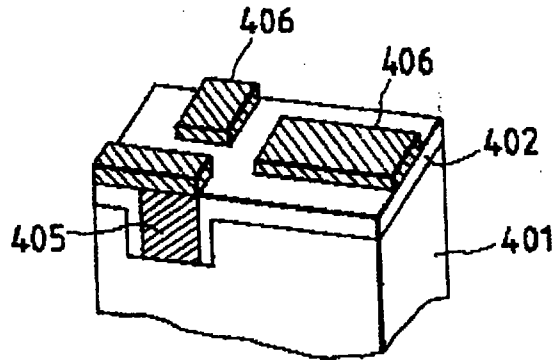


FIG. 20D



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Device Separation Structure and Semiconductor Device Improved in Wiring Structure

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to a semiconductor circuit device such as memory, photoelectric converting device, signal processing device, etc. to be mounted on various electronic instruments, particularly to a metal wiring structure and a semiconductor device improved in device separation structure.

Related Background Art

Conventionally, device separation in semiconductor device has been constituted as shown in Fig. 1. In the Fig. 1, the symbol 1 is metal wiring, 2, 3 are device regions where transistor, FET, resistance, condenser, photosensor, etc. are formed, and electrical insulation thereof is effected by the device separation region, namely the Si substrate 4 doped with an impurity or the Si layer 5 doped with the same impurity. The potentials of the device separation regions of 4, 5 are fixed by the metal wiring 1 or 6.

For example, the device separation region of a solid image pick-up device is constituted as shown in

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19 NOV 1996

Fig. 2. In the Figure, the symbol 4 is a P type substrate, 5' an n^+ buried layer, 2 an n^- epitaxial growth layer (hereinafter epitaxial growth is written as epi), 5 an n^+ layer. The above n^- epi layer 2 is a photoelectric converting region, and the n^+ buried layer 5' and the n^+ layer 5 are device regions.

The n^- epi layer 2 is maintained at a certain positive potential through the n^+ buried layer 5' and the n^+ layer 5. By the build-in electrical field through junction between the n^- epi layer 2 and the n^+ layer 7, the electrons formed by photoirradiation are absorbed in the n^+ buried layer 2 and the n^+ layer 7, and the positive holes cannot be diffused to the confined adjacent picture elements, whereby cross-talk can be prevented.

However, prior art examples had the technical tasks as follows.

(1) There was an impedance of about some ten to some hundred $\Omega/\square$. For this reason, current flowed into the region 5, and when the potential is elevated, parasitic transistor turned on between the device regions 2 and 3, whereby latch-up or unstable actuation of function was caused to occur.

(2) On account of the impedance in the region 5, cross-talk in the device regions 2 and 3 was generated to cause unstable actuation.

Particularly in the case of a solid image

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pick-up device,

(3) The positive holes having acquired thermally high energy will be diffused to the adjacent picture elements.

(4) Since the device separation region is also a semiconductor, carriers will be generated when light is irradiated.

(5) The width of the n^+-Si device separation cannot be made narrow in process to obstruct reduction of picture element, whereby higher resolving power of solid image pick-up device has been obstructed.

On the other hand, as the metal wiring structure in a highly integrated semiconductor device, for example, there has been known one having an interlayer insulating film 52 comprising silicon oxide, etc. formed on the surface of a semiconductor substrate 51 comprising silicon and a metal wiring layer 53 comprising Al, Al-Si, etc. formed on the interlayer insulating film 52 as shown in Fig. 2A.

In the semiconductor device equipped with the metal wiring of such structure, the sectional area of wiring has been increased by enlargement of the width dimensions of the respective wirings, thereby ensuring necessary current tolerant capacities for the respective wirings, and therefore the flat area of wiring will be increased and improvement of wiring

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without making greater the device size is limited.

For this reason, for improvement of wiring density, for example, a semiconductor device of a wiring structure having the respective wirings laminated in multiple layers as shown in Fig. 2B has been known.

In this semiconductor device, two layers of metal wiring are laminated through an insulating film.

In the following, the outline of the process for preparing the semiconductor device shown in 2B is described.

First, after formation of various necessary functional devices such as bipolar transistor, MOS transistor, MOS diode, etc. on a part of the surface of the semiconductor substrate 1, on the remaining surface of the semiconductor substrate 51 is formed a first interlayer insulating film 52 comprising PSG (Phospho silicate glass), etc. according to the normal pressure CVD method with a thickness of 0.5 to 1.0 μm, and the first interlayer insulating film 52 is applied with annealing.

Next, patterning by use of a resist is applied on the first interlayer insulating film 52 as described above to form openings 52a for taking out electrodes of various functional devices. Subsequently, according to the sputtering method,

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after deposition of a wiring material comprising, for example, Al-Si according to the sputtering method on the surface of the first interlayer insulating film 52 and internally of the openings 52a, the first wiring layer 53 is formed by patterning by use of a resist.

Next, on the first wiring layer 53 and the first interlayer insulating film 52 are formed a second interlayer insulating film 54 comprising PSG with a thickness of about 0.5 to 1.0 μm according to the normal pressure CVD method, openings 54a for connecting the first wiring layer and the upper wiring layer as described below to a part of the second interlayer insulating film 54 corresponding to the upper portion of the first wiring layer 53 are formed.

Next, on the second insulating film 54 and internally of the openings 54a, a wiring comprising, for example, Al-Si is deposited, followed by formation of the second wiring layer 55 for connecting the second wiring layer 55 for connecting the first wiring layer 52 through the portion of the openings 54a by patterning.

Next, on the second interlayer insulating film 54 and the second wiring layer 55, a passivation film 6 can be formed with a thickness of 0.5 to 1.0 μm according to the plasma CVD method to prepare a

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semiconductor device with a metal double layer wiring structure shown in Fig. 2B.

In the semiconductor device having a multi-layer wiring structure of such constitution, a wiring with wiring density by far higher than the semiconductor device with the monolayer wiring structure shown 2A can be realized.

However, in the semiconductor device having a multi-layer wiring structure as described above, since an interlayer insulating film is provided between the wiring at the lower part and the wiring at the upper part, the surface stepped difference due to the wiring portion will become greater as the number of the lamination is more, whereby the degree of freedom in design in the wiring structure is regulated because of movement of the position (migration) of the wiring portion relative to the semiconductor substrate at the wiring portion or the shape of the contact hole necessary for connection between the respective insulating layers. Thus, also in this case, improvement of wiring density is limited and it has been difficult to enhance wiring density more than a certain level.

Further, in a semiconductor device with a multi-layer structure, surface unevenness becomes greater as the layer is upper, and therefore slippage in alignment becomes greater during mask registration

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in patterning when laminating further wiring, whereby wiring could not be formed with good precision at the predetermined position relative to the semiconductor substrate, thus involving the problem with respect to reliability of wiring.

SUMMARY OF THE INVENTION

A primary object of the present invention is to provide a semiconductor device having a wiring structure more excellent than in the prior art.

Another primary object of the present invention is to provide a semiconductor device having more excellent device separation function than in the prior art.

First, an object of the present invention is to provide a semiconductor device having a device separation structure with a device region being formed on a substrate doped with an impurity, a device separation region doped with the same impurity as in the above substrate formed in the device region and a metal wiring formed on the surface of the above device region or on the back of the above substrate, wherein an aluminum deposited layer extending in the longitudinal direction connected to the above metal wiring is formed within the above device separation region.

Another object of the present invention is to

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provide a semiconductor device which can reduce the impedance of the device separation region of semiconductor device, prevent generation of latch-up or cross-talk and give stability in actuation.

Still another object of the present invention is to provide a semiconductor device equipped with a wiring structure which can ensure necessary current tolerable quantity even if the wiring flat area may be small.

Still another object of the present invention is to provide a semiconductor device comprising a device region formed on a substrate, and also a first device separation region formed doped with an impurity formed between these substrate and device region, with the respective ends being connected to the both ends of the above-mentioned first device separation region, and the respective other ends exposed on the surface of the above-mentioned device regions, thus forming a trench metal layer of aluminum or composed mainly of aluminum.

Still another object of the present invention is to provide a semiconductor device comprising a device region formed on an insulating substrate, having a trench metal layer of aluminum or composed mainly of aluminum which becomes the device separation region extending in the longitudinal direction with its one end being in contact with the

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above-mentioned insulating substrate and its other end being formed exposed on the surface of the above-mentioned device region.

Still another object of the present invention is to provide semiconductor device which removed cross-talk between the picture elements and enables higher densification of picture elements by using a trench metal layer constituted by selective growth deposition of aluminum or a metal composed mainly of aluminum within the trench for forming the device separation layer.

Still another object of the present invention is to provide a semiconductor device which can also reduce the lay-out, because the trench metal layer can be used as the wiring line.

Still another object of the present invention is to provide a semiconductor device comprising a metal wiring layer for connecting at least two functional devices to the inner portion of a semiconductor substrate having at least functional devices as mentioned above.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A, 1B, 2A, 2B are constitutional views for illustration of the semiconductor device of the prior art.

Fig. 3 is a constitutional view of the

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pertinent portion of the semiconductor device showing a first example of the present invention.

Fig. 4 is a constitutional view of the pertinent portion of the semiconductor portion showing a second example of the present invention.

Fig. 5 is a constitutional view of the pertinent portion of the semiconductor portion of the semiconductor device applied to the present invention.

Fig. 6A is a constitutional view of the semiconductor device applied to the present invention, Fig. 6B is a circuit diagram of the same device.

Figs. 7A to 7D are diagrams of the steps for preparing the semiconductor device applied to the present invention.

Fig. 8 is a constitutional view of the pertinent portion of the semiconductor device showing a third example of the present invention.

Fig. 9 is a constitutional view of the semiconductor device showing a fourth example of the present invention.

Figs. 10A and 10B are schematic views for illustration of the logic circuit according to the present invention.

Fig. 11 is an upper view showing the logic circuit according to the present invention.

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Fig. 12 is a schematic sectional view showing the wiring structure intended to apply a positive potential.

Fig. 13 is a schematic sectional view showing the wiring structure intended to apply a negative potential.

Fig. 14 is a schematic sectional view showing an example of a multi-layer wiring structure in the semiconductor device of the present invention.

Figs. 15A to 15C are schematic views for illustration of the preparation method of the wiring structure in Fig. 14.

Figs. 16, 17 are schematic view showing an example of the film forming device to be used for practicing the film forming method suitable for formation of the wiring layer in the semiconductor device according to the present invention.

Fig. 18 is a schematic plan constitutional view of the device shown in Figs. 16, 17.

Fig. 19 is a schematic constitutional view with the movement order shown by arrowheads in Fig. 18.

Figs. 20A to 20D are schematic view for illustration of the film forming method suitable for formation of the wiring layer in the semiconductor device according to the present invention.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

One preferred embodiment of the present invention has a longitudinally lengthy buried region comprising a metal in the device separation region.

When the predetermined region which is a part of the semiconductor substrate and the longitudinally lengthy buried region of a metal are electrically connected, the following embodiment is taken.

For example, when the metal is electrically connected to a predetermined region only at bottom, the whole side wall should be preferably coated with an insulating film.

On the other hand, when the metal is insulated from a part of the side groove or bottom of the groove, only said part is coated with an insulating film.

Example 1

Fig. 3 is a drawing representing best the specific feature of the first example of the present invention, in which the symbol is the device separation wiring formed in the longitudinal direction within the device separation region 5 as described below according to the Al-CVD method as described below, 2 the first device region, 3 the second device region, 4 the Si substrate doped with an impurity, 5 the device separation region doped with an impurity of the same type as in the substrate

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4.

As shown in the drawing, by deposition the device separation wiring 1 deeply in the longitudinal direction with an aspect ratio of 1.0 or more, preferably 2.0 or more, optimally 3.0 or more, the impedance of the device region 5 can be reduced without bringing about increase of chip area. By reduction of impedance, the following effects can be obtained:

(1) Prevention of latch-up;

(2) Improvement for functional lowering due to mutual interference between devices (reduction of cross-talk).

Next, the process for preparing a semiconductor device having the device separation structure with the above constitution is described.

i) On a mono-electroconductive semiconductor substrate, for example, a P-type Si substrate 4, an n-type epi-layers 2, 3 are formed by epitaxial growth as the layer having the impurity of the reverse conduction type to the substrate 4.

ii) Next, after formation of the oxidized film to 0.5 to 1.0 μm on a surface of above-mentioned epi-layers 2, 3 by thermal oxidation, impurities (e.g. P type) with the reverse conduction type to the epi-layers 2, 3 are formed on the device separation region 5 by patterning by ion injection with the

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above-mentioned oxidized film as the mask. The diffusion layer is made so as to reach the subbing semiconductor substrate 4.

iii) Next, after the oxidized films on the surfaces of the epi-layers are removed, again oxidized films with a thickness of 100 to 1000 Å are formed. Then, the above-mentioned device separation region 5 is internally opened by regist patterning, and the oxidized film and the epi-layer are etched in two steps with the resist as the mask to form grooves. In this case, the depth of the groove is made to reach the subbing semiconductor substrate 4. After completion of etching, the resist is removed.

iv) Next, by use of DMAH and hydrogen as the Al-CVD method as described above, Al is buried in the grooves provided within the epi-layers 2, 3. Here, the material to be buried within the grooves is not limite to Al, but Al-Si, Al-Ti may be also used as the metal material as described above.

Example 2

Fig. 4 shows a drawing representing best the specific feature of the second example, wherein the symbol 1 is the device separation wiring of the buried type with a large aspect ratio, 2 the first device region, 3 the second device region, 4 the Si substrate doped with an impurity, 5 the device

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separation Si doped with the impurity of the same type as in 4, and 6 the back metal wiring.

By fixing of the potential in the device separation region 5 with the device separation wiring 1 and the back metal wiring 6, no wiring from the chip upper surface will be required to result in reduction of chip area.

Next, the process for preparing the semiconductor device having the device separation structure having the above-mentioned structure is described.

The steps i) - ii) are practiced in the same manner as in Example 1, and hence description thereof is omitted. iii) Next, after formation of an oxidized film on the back surface of the semiconductor substrate 4 by thermal oxidation, patterning is effected so as to form openings only on the back surface of the semiconductor substrate 4 immediately below the above device separation region 5.

Then, continuously to the oxidized film from the back surface of the semiconductor substrate 4, the semiconductor substrate 4 is etched to provide grooves on the back surface of the semiconductor substrate 4. The depth of the grooves is made to extend through the semiconductor substrate 4 until reaching the above-mentioned diffusion layer 5 for

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device separation. iv) Next, as the Al-CVD method, Al is deposited selectively at the groove portions similarly as in Example 1 to bury Al within the grooves. Then, according to the sputtering method of the non-selective mode, an Al film is formed on the whole back surface of the semiconductor substrate 4.

Example 3

Next, the semiconductor functional devices formed in the device region 2 or 3 is described by referring to Fig. 5 and Fig. 6. The semiconductor functional device is characterized by forming a device wiring 12 with a large aspect ratio for fixing the back gate of the MOS type transistor (P well region 10 of nMOS, and n-epi or n-well region 11 of pMOS) at any desired potential in the P-well region 10 the n-epi or n-well region in the longitudinal direction according to the Al-CVD method as described above.

Example 4

Fig. 6A is a sectional constitutional view of another semiconductor functional device, and Fig. 6B is the circuit diagram of the same device. The device is characterized by forming the device separation wiring 12 for reducing the resistance in the back gate when the P-well 10 which is the back gate of the MOS type transistor and the n-epi or n-well 11 are at the same potential as the source region (or drain

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region) in the source (or drain) region 13 according to the Al-CVD method as described above.

In the MOS type transistor of the prior art, the resistance of the back gate has been a cause for latch-up or lowering in function. Also, since the device region and the wiring region have been increased in order to reduce this problem, increase of layout area has been brought about.

In contrast, in the above-mentioned device, as shown in Fig. 5 and Fig. 6A, by depositing the device wiring 12 deeply in the longitudinal direction according to the Al-CVD method, the resistance of the back gate can be reduced with smaller wiring area to ameliorate latch-up or lowering in function which has been the problem in the prior art. Particularly, in the logical circuit (e.g. invertor) as shown in Fig. 6, the wiring structure can be made as shown in the figure in the region where the power source and the source (or drain) are at the same potential, whereby less wiring area is required and the problems of the prior art can be improved.

Next, the process for preparing the device shown in Fig. 5 is described by referring to Fig. 7A to Fig. 7D.

First, according to the known C-MOS preparation technique, working is practiced to the state immediately before formation of contact holes

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(Fig. 7A).

Next, according to the photolithography by use of a resist, a resist image corresponding to the openings to be formed of about 0.8 μm at the P-well portion of n-MOS, the n-epi or n-well portion 11 of P-MOS (Fig. 7B).

Next, by use of the CHF_3-C_2F_6 type dry etching, openings 22 extending through the two layers of the interlayer insulation layer 20 and the field oxidized film 21 are formed. Then, without removal of the resit, the silicon substrate is etched vertically to about 1 μm by the Cl_2-$CBrF_3$ type dry etching.

Next, by use of the Al-CVD method as described in Example 1, aluminum 12 is buried to the upper surface of the interlayer insulation film. The total amount buried is made 2.5 μm as the total with the silicon substrate groove being 1 μm, the field oxidized film 21 being 8000 Å, and the interlayer insulation layer 20 being 7000 Å. (Fig. 7C).

Employing subsequently known techniques contact opening formation, aluminum wiring formation, etc. can be practice to complete the sample.

Preparation of the example shown in Fig. 6 can be also practiced according to the same procedure as in Fig. 5. The difference is only that the

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opening formation site becomes the source (or drain) portion of the MOS transistor, and the interlayer insulation layer-gate oxidized film is extended through instead of extending through of the interlayer insulation layer-field oxidized film during opening formation.

As described above, by depositing Al in the longitudinal direction by use of the Al-CVD method within the device separation region, reduction of chip area can be effected as compared with the case when obtaining the same effect without use thereof, whereby Al wiring portion can be made smaller, with the result that the production cost can be made lower.

Example 5

Fig. 8 is a drawing showing best the specific feature of the present example of the present invention, in which the symbol 4 is a P substrate, 5' an n^+ buried layer, 2 an n^- epi-layer, and 1 a trench metal layer formed according to the CVD method. The above trench metal layer 1 has its one end exposed on the above n^- epi-layer surface 2 with other end being connected to the above n^+ buried layer 5'.

The n^- epi-layer 2 is a photoelectric converting region (called device region or activation region), and the n^+ buried region 5' and the trench metal layer 1 are device separation regions. The

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trench metal layer 1 also a wiring line.

The n^- epi-layer 2 is maintained at a certain potential through the n^+ buried layer 5' and the trench metal layer 1.

In the above-mentioned structure, the electrons formed by photoirradiation are absorbed primarily into the n^+ buried layer 5' through the built-in electrical by the junction of the n^+ buried layer 5' and the n^- epi-layer 2. The positive holes are closed within the picture elements by the built-in electrical field.

The positive holes which tend to be diffused to the adjacent picture elements will be all absorbed in the trench metal layer 1, and therefore there can be no cross-talk between picture elements.

The device separation region 1 is formed by forming the trench (groove) by etching, and then depositing aluminum or a metal composed mainly of aluminum on the groove according to the selective CVD method as described above, whereby the device separation region width can be reduced as compared with the prior art, enabling higher densification of picture elements.

The trench metal layer 1 has a low resistance and therefore can be also utilized as the wiring line, whereby reduction of the layer is rendered possible.

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Next, a process for preparing the device separation structure semiconductor device of the above constitution is described.

i) On a monoconduction type semiconductor, for example a P type Si substrate 4 are formed grooves with wide width shallowly on a part thereof. In the grooves, n^+ buried layer 5' containing impurities of the opposite conduction type to the substrate 4 according to the epitaxial growth by use of as mask.

ii) On the substrate 4 having the n^+ buried layer 5' formed as described above, an n^- epi-layer 2 which becomes the photoelectric converting region is formed by epitaxial growth.

iii) Next, after formation of oxide flms with a thickness of 0.5 to 1.0 μm on the surface of the above n^- epi-layer 2 by thermal oxidation, opening are formed internally of the above n^- epi-layer at the both ends of the above-mentioned n^+ buried layer by resist patterning, followed by etching with the resist as the ask to form a trench. In this case, the depth of the trench is made the depth which reached the subbing n^+ buried layer 5'. After completion of etching, the resist was removed.

iv) Next, by use of the Al-CVD method as described below using DMAH and hydrogen as the selective CVD method, the substrate surface

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ii) On the substrate 4 having the n^+ buried layer 5' formed as described above, an n^- epi-layer 2 which becomes the photoelectric converting region is formed by epitaxial growth.

iii) Next, after formation of oxide flms with a thickness of 0.5 to 1.0 μm on the surface of the above n^- epi-layer 2 by thermal oxidation, opening are formed internally of the above n^- epi-layer at the both ends of the above-mentioned n^+ buried layer by resist patterning, followed by etching with the resist as the ask to form a trench. In this case, the depth of the trench is made the depth which reached the subbing n^+ buried layer 5'. After completion of etching, the resist was removed.

iv) Next, by use of the Al-CVD method as described below using DMAH and hydrogen as the selective CVD method, the substrate surface

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temperature was maintained at 270 °C, and Al is buried in the trench provided within the n^- epi-layer. Here, the material to be buried in the trench is not limited to Al, but Al-Si, Al-Ti, etc. may be also employed as the metal material.

Example 6

Fig. 9 is an example in which the present invention is applied to a semiconductor device having an insulating substrate. 1 is a trench metal layer, 4' an insulation substrate and 2 a semiconductor substrate layer.

The above semiconductor layer 2 is a photoelectric converting region, and the trench metal layer 1 is a device separation region and a wiring line. By the trench metal layer 1, it becomes possible to obtain a semiconductor with high density without cross-talk.

Next, a process for preparing a device separation structure semiconductor structure of the above constitution is described.

i) On an insulation substrate 4' comprising sapphire, a semiconductor layer 2 comprising a photoelectric converting region (device region) is formed by epitaxial growth.

ii) Next, after formation of an oxidized film to 0.5 to 1.0 μm on the surface of the above semiconductor layer 2 by thermal oxidation, opening

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are formed internally the above semiconductor layer by resist patterning, and etching effected with the resist as the mask to form a trench. In this case, the depth of the trench is made the depth which reaches the subbing insulating substrate 4'. After completion of etching, the resist is removed.

iii) Next, by use of DMAH and hydrogen as the selective CVD method as described above, the substrate surface temperature is maintained at 270 °C, and aluminum is buried in the trench provided within the semiconductor layer 6. Here, as the metal material, aluminum is not limitative, but Al-Si, Al-Ti, etc. may be also used as mentioned above.

As described above, by use of the trench metal layer as the device separation region, it becomes possible to obtain a semiconductor device with high picture element density and reduced chip size without cross-talk between the picture elements.

Another preferred embodiment of the present invention has a part of the metal wiring for connecting a plurality of devices formed not on the insulating film on the semiconductor substrate but within the groove formed on the semiconductor substrate.

Example 7

Fig. 10A is a circuit diagram showing a part of the logic circuit of the CMOS constitution, and

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Fig. 10B a schematic view showing the lay-out thereof.

Thus, the power source line Vcc and the earthline GND are commonly arranged for the respective cells. In these lines, reduction of the impedance, avoidance of erroneous actuation and further avoidance of lowering in reliability by migration, etc. are particularly demanded.

Hence, by use of buried wirings in these lines, in addition to functional aspect, improvements in physical aspect such as reduction of occupied area, reduction of stepped difference, etc. can be effected.

Similarly, the buried wiring has also the effect even by use of the clock-line for transmitting the clock signals. In this case, after formation of the groove for forming such wiring in the semiconductor substrate, the whole inner surface of the groove is covered with an insulating layer. And, by depositing a semiconductor material or an electroconductive material within the groove, a subbing layer for selective deposition of a metal is formed. And, by burying a metal within the groove, the semiconductor device of the present embodiment is formed.

Fig. 11 is a schematic view for illustrating in more detail Fig. 10B, and 63 is the same invertor

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as the CMOS in Fig. 6.

Here, the line Vcc and the line GND are both buried wirings connected to the source region and the well region of the two MOSFET's, forming the common line for the both adjacent cells 61, 62.

a is the polycrystalline gate electrode which becomes the input of the invertor, out is the drain wiring which becomes the output of the invertor. In this example, as different from the prior art, the power source lines Vcc and the earthline GND are wirings of the lower layers than the gate electrode a.

In the semiconductor device of the present embodiment, since the metal wiring layer is provided within the substrate, a predetermined current tolerant capacity can be ensured by making larger the depth dimension without increasing the plan area of the metal wiring layer, and also the unevenness of the device surface can be inhibited minimum, whereby the relative movement of the wiring layer relative to the substrate can be removed to improve the precision of the formation position of the wiring layer.

Example 8

Fig. 12 and Fig. 13 are both Figures representing the characteristic portions of the wiring structures in the semiconductor devices of the present invention. Here, Fig. 12 shows the wiring

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structure constituted for the purpose of applying a positive voltage as the power source line, and Fig. 13 the wiring structure constituted for the purpose of applying a negative voltage as the earth line. These wiring structures are the embodiments of the present invention in that they are constituted on the basis of the technical thought of the present invention except that the kinds of the materials for forming the respective portions are different concerning the application method of voltage. Therefore, the constitution of the former and the preparation method thereof are described before description of the constitution and the preparation method thereof in difference from the former.

In Fig. 12, the symbol 710 is a P^- type semiconductor substrate comprising, for example, silicon, etc. On the surface of the substrate 710 is formed a groove 711 by conventional means such as etching, etc., and the inner surface excluding the bottom surface of the groove 711 and the surface of the substrate 710 is formed an insulation layer 712 comprising oxidized silicon, etc. formed by the thermal oxidation method or the CVD method, etc. continuously. From the bottom surface of the groove 711 to internally of the substrate 710 as described above, if necessary, an N^+ type diffusion layer 713 is provided, which is formed by thermal diffusion as

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the semiconductor region doped with an impurity of the opposite type to the conduction type of the semiconductor such as silicon forming the substrate 710.

Internally of such groove 711, a metal wiring layer 714 comprising a metal such as Al, etc. is provided. The metal wiring layer 714 may be also formed by use of a conventional method such as bias sputtering, etc., but preferably it can be also formed by use of the Al-CVD method as described below. The Al-CVD method is a film forming method with good reproducibility which can form a metal film of Al, etc. selectively on the substrate 710, namely the bottom of the groove 711 in this case without formation on the insulation layer 712 comprising silicon oxide.

The wiring film thus formed is used for connection between the predetermined electrode terminals mutually between two functional devices or, if necessary, 3 or more functional devices, to constitute an electrical circuit. For example, it may be used suitably used for connection between two source-drains of MOSFET or collectors of a bipolar transistor, or between MOSFET or a bipolar transistor and a diffusion resistance, between MOSFET or a bipolar transistor and a capacity device, etc.

Next, an example for preparing the wiring

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structure with such constitution is described.

First, as shown in Fig. 12, a P^- type silicon substrate 710 is prepared as the semiconductor substrate.

Subsequently, on the surface of the substrate 710, after application of a patterning by use of a resist, a groove 711 for formation of a wiring layer is formed by application of etching.

Then, an insulation layer 712 with a film thickness of 0.5 to 1.0 μm is formed according to the thermal oxidation method or the CVD method on the surface of the substrate 710 and the inner surface of the groove 711.

Next, after application of a patterning by use of a resist on the whole surface of the substrate 711 excluding the bottom of the groove 711, the oxidized film layer formed on the bottom of the groove 711 is removed by anisotropic etching such as RIE (reactive ion etching) to have the silicon portion of the substrate 710 exposed.

Next, at the silicon exposed portion of the bottom of the groove 711, an impurity of the type opposite to the conduction type of the material for forming the substrate 710 is doped according to the ion injection method of the thermal diffusion method, followed by diffusion to form an N^+ type diffusion layer 713.

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in the case when the width dimension itself is short, there is the advantage that an Al film of good quality can be formed from the bottom of the groove 711. Therefore, it is sufficiently applicable to a fine structure with an aspect ratio of 1.0 or more as a matter of course, even 1.5 or more, further 2.0 or more. Further, because an Al film of good quality can be also formed internally of a deep groove 711 easily, the current tolerance of the metal wiring layer 714 can be easily increased by enlarging the depth dimension without enlarging the width dimension of the metal wiring layer 714.

Next, the wiring structure shown in Fig. 13 is described. In Fig. 13, the same portions as the constitution in Fig. 12 are affixed with the same symbols for brevity of the description.

In Fig. 13, the symbol 720 is an N^- type semiconductor substrate comprising, for example, silicon, as the substrate. On the surface of the substrate 720 is formed a groove 711 by conventional means such as ethcing, etc. and on the inner surface excluding the bottom internally of the groove and the surface of the substrate 720 is formed continuously an insulation film 712 comprising silicon oxide, etc. according to the thermal oxidation method or the CVD method. Internally of the substrate of the substrate 720 from the bottom of the groove 711 as described

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above, an impurity of the conduction type opposite to that of the semiconductor such as silicon, etc. for forming the substrate 720 to provide a P^+ type diffusion layer 21 as the semiconductor region formed by thermal diffusion.

Internally of such groove 711, a metal wiring layer 714 comprising a metal such as Al, etc. is provided. In such metal wiring layer 714, electrical separation is effected from the N^- type silicon substrate 720 through the insulation layer 712 as the insulation film formed on the inner surface of the groove 711 and the P-N separation layer formed on the bottom of the groove 711. Therefore, substantially no leak current from the metal wiring layer 714 to the substrate will occur.

The wiring structure of the present invention with such constitution can be utilized for all functional devices, namely field effect transistors, bipolar transistors, diffusion resistances, etc.

Fig. 14 is an example of the wiring structure of the present invention, which is a schematic sectional view showing a wiring structure of two metal layers.

In Fig. 14, the symbol 730 is an N^- type semiconductor substrate comprising, for example, silicon. On the surface of the substrate 730 is formed a groove 731 according to conventional means

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such as etching, etc., and on the inner surface excluding the bottom internally of the groove 731 and on the surface of the substrate 730 are formed continuously an oxidized film layer 732 comprising silicoin oxide, etc. according to the thermal oxidation method or the CVD method. From the bottom of the groove 731 as described above to internally of the substrate 730 is doped an impurity of the conduction type opposite to that of the semiconductor such as silicon, etc. forming the substrate 730 to provide a P^+ diffusion layer 733 formed by thermal diffusion.

Internally of such groove 731, a first wiring layer 734 comprising, for example, Al, etc. is formed according to the selective Al-CVD method as described below. The first metal wiring layer 734 has its upper surface coplanar with the surface of the substrate 730.

On a part of the oxidized film layer 732 as described above, openings 735 for taking out the electrode of the semiconductor device reaching the surface of the substrate 730 are formed.

On the surface of the oxidized film layer 732 together with the inner portion of the openings 735 and the inner portion of the groove 731 at upper portion of the first metal wiring layer 734, a second metal wiring layer 736 comprising a metal such as Al,

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etc. is formed. A passivation film 737 comprising, for example, silicon nitride, etc. is formed on the second metal wiring layer 736 and the oxidized film 732.

Referring next to Fig. 15A to Fig. 15C, a method for preparing a semiconductor device having the wiring structure with the constitution shown in Fig. 3.

First, as shown in Fig. 14A, an N^- type silicon substrate 730 is prepared.

Next, after application of a patterning by use of a resist on the surface of the substrate 730, a groove 731 for formation of a first metal wiring layer is formed.

Next, an oxidized film layer 732 with a film thickness of about 0.5 to 1.0 μm is formed on the surface of the substrate 730 the inner surface of the groove 731 according to the thermal oxidation method.

Next, after application of a patterning by use of a resist on the whole surface of the substrate 730 excluding the bottom of the groove 731, the oxidized film layer formed on the groove 731 is removed by anisotropic etching of RIE (reactive ion etching) to have the silicon portion of the substrate 730 exposed.

Next, the silicon exposed portion at the bottom of the groove 731 is doped with B as the

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impurity of the conduction type opposite to that of the material for forming the substrate 730 according to the ion injection method, followed by diffusion to form a P^+ diffusion layer 733.

Next, on the P^+ type diffusion layer 733 is formed a first metal wiring layer 734 comprising Al, etc. according to the selective Al-CVD method as described above. The first metal wiring layer 734 is formed so that its upper surface became coplanar with the upper surface of the substrate 730 around the groove 731. The first metal wiring layer 734 is separated electrically from the N^- type silicon substrate 730 through the oxidized film layer 732 as the insulation film formed on the inner surface of the groove 731 and the P^+ type diffusion layer 733 as the P-N separation layer formed on the bottom of the groove 731. And, it is confirmed that there is substantially no leak of current from the first wiring layer 734 to the substrate 730.

Next, after application of a patterning by use of a resist on the surface of the oxidized film layer 732, openings 735 for taking out the electrode of the semiconductor device reaching the surface of the substrate 730 are formed in a part of the oxidized film layer 732 (Fig. 15B).

Next, internally of the openings 735 and internally of the groove 731 at the upper portion of

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the first metal wiring layer 734 is formed by depositing a second metal wiring lower layer 736a comprising Al utilizing DMAH and hydrogen as the Al-CVD method at a substrate surface temperature of 270 °C. The second method wiring lower layer 736a is formed so that its surface may be coplanar with the upper surface of the oxidized film layer 732. Next, on the respective upper surfaces of the second metal wiring lower layer 736a and at the predetermined positions on the surface of the oxidized film layer 732 are formed the upper second metal wiring layer 736b comprising Al according to the sputtering method (see Fig. 15C).

Further, on the second metal wiring layer 736 and the oxidized film layer 732, a passivation film 737 comprising silicon nitride with a film thickness of about 0.5 to 1.0 μm is formed according to the plasma CVD method to obtain a semiconductor device equipped with the metal double layer wiring structure as shown in Fig. 14.

Also in the semiconductor device with such constitution, the first metal wiring layer 734 provided internally of the N^- type silicon substrate 730 is separated from the N^- type silicon substrate 730 through the oxidized film layer 732 as the insulation film on the inner surface of the groove 731 and the P^+ type diffusion layer 733 as the P-N

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separation layer at the bottom of the groove 731, and there will be substantially no leak current from the first metal wiring layer 734 to the substrate 730. In the first metal wiring layer 734, the desired current tolerance can be ensured by enlarging the depth dimension without enlarging its flat area. Also, since the unevenness of the surface of the semiconductor device can be inhibited minimum, there is no relative movement of the first metal wiring layer 734 to the substrate 730 to effect improvement of the precision of the formation position of the first metal wiring layer 734, and also the number of the multiple layers of wiring can be increased within the range of a limited thickness of the device. Further, since no interlayer insulation film is required between the first metal wiring layer and the second metal wiring layer, the surface stepped difference can be reduced in the case of providing wiring layers of the third metal wiring layer et seq, whereby reliability of the wiring layers of the third layer et seq can be improved.

As described above, according to the present invention, a wiring structure capable of ensuring necessary current tolerance can even with a small wiring flat area and also capable of being formed at a high positional precision can be obtained.

The film forming method suitable for the

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present invention is to form a deposited film by the surface reaction on an electron-donative substrate by use of a gas of an alkylaluminum hydride and hydrogen gas (hereinafter called the Al-CVD method).

Particularly, by use of monomethylaluminum hydride (MMAH) as the starting gas or dimethylaluminum hydride (DMAH) as the starting gas, and H_2 gas as the reaction gas, and heating the substrate surface under the mixture of these gases, an Al film of good quality can be deposited. Here, during the selective deposition of Al, it is preferable to maintain the surface temperature at the decomposition temperature of the alkylaluminum hydride or higher and less than 450 °C, more preferably 260 °C to 440 °C.

As the method for heating the substrate to the above-mentioned temperature range, there are direct heating and indirect heating. Particularly, by maintaining the substrate at the above-mentioned temperature by direct heating, an Al film of good quality can be formed at high deposition speed. For example, when the substrate surface temperature during Al film formation is made 260 °C to 440 °C which is more preferable temperature range, a film of good quality can be obtained at higher deposition speed of 300 Å to 5000 Å/min. which is higher than in the case of resistance heating. As such direct

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heating method (substrate itself is heated by direct transmission of the energy from the heating means to the substrate), for example, lamp heating by means of halogen lamp, xenon lamp, etc. may be included. As the method for indirect heating, there is resistance heating, by which heating can be performed by use of a heat-generating body, etc. provided at the substrate supporting member for supporting the substrate to form deposited film arranged in the space for formation of the deposited film.

By applying the CVD method to the substrate having the electron-donative surface portion and the non-electron donative surface portion co-present thereon, a single crystal of Al is formed under good selectivity only on the electron-donative substrate surface portion. The Al thus formed will have all of excellent characteristics desirable for the electrode/wiring material. That is, reduction of generation probability of hillock, reduction of generation probability of alloy spike will be accomplished.

This may be considered to be due to the fact that substantially no or extremely small formation of alloy spike, etc. on account of the eutectic reaction with the subbing silicon, etc. is seen, because Al of good quality can be formed on the surface comprising a semiconductor or an electro-conductive

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member as the electron-donative surface, and also the Al is excellent in crystallinity. And, when employed for the electrode of a semiconductor device, an effect surpassing the concept of the Al electrode which has been contemplated in the prior art, and could not be even expected in the prior art can be obtained.

Having described above about the fact that the Al deposited on an electron-donative surface, for example, within the opening with the semiconductor substrate surface exposed becomes to have a single crystalline structure, according to the Al-CVD method, a metal film composed mainly of Al as described below can be also selectively deposited, and its film quality also exhibits excellent characteristics.

For example, in addition to a gas of an alkylaluminum hydride and hydrogen,

a gas containing Si atoms such as SiH_4, Si_2H_6, Si_3H_8, $Si(CH_3)_4$, $SiCl_4$, SiH_2Cl_2, $SiHCl_3$, or the like.

a gas containing Ti atoms such as $TiCl_4$, $TiBr_4$, $Ti(CH_3)_4$, etc.,

a gas containing Cu atoms such as copper bisacetylacetonate $Cu(C_5H_7O_2)$, copper bisdipivaloylmethanite $Cu(C_{11}H_{19}O_2)_2$, copper bishexafluoroacetylacetonate $Cu(C_5HF_6O_2)_2$, etc.

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may be introduced in a suitable combination to form a gas mixture atmosphere, thereby forming an electrode by selective deposition of an electroconductive material such as Al-Si, Al-Ti, Al-Cu, Al-Si-Ti, Al-Si-Cu, etc.

The Al-CVD method as described above is a film forming method excellent in selectivity, and also the surface characteristic of the film formed has good surface characteristic. Hence, by application of a non-selective film forming method to the next deposition step, Al or a metal film composed mainly of Al can be also formed on the Al film selectively deposited as described above and SiO_2, etc. as the insulating film, whereby a suitable metal film having high useability for general purpose as the wiring of semiconductor device can be obtained.

Specific examples of such metal film include the following. There may be included combinations of Al, Al-Si, Al-Ti, Al-Cu, Al-Si-Ti, Al-Si-Cu, etc. deposited selectively with Al, Al-Si, Al-Ti, Al-Cu, Al-Si-Ti, Al-Si-Cu, etc.

As the film forming method for non-selective deposition, there are other CVD methods than the Al-CVD method as described above, the sputtering method, etc.

(Film Forming Apparatus)

Next, a suitable film forming apparatus for

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forming the electrode according to the present invention is described.

Fig. 16 to Fig. 18 show schematically a sequential metal film forming apparatus suitable for applying the film forming method as described above.

The sequential metal film forming apparatus, as shown in Fig. 16, is constituted of loadlock chamber 311 connected mutually communicated under shielding from outer air through the gate valves 310a to 310f, a CVD reaction chamber 312 as the first film forming chamber, an Rf etcing chamber 313, a sputtering chamber 314 as the second film forming chamber and a loadlock chamber 315, and the respective chambers are constituted reducible in pressure by evacuation with the evacuation systems 316a to 316e. Here, the above loadlock chamber 311 is a chamber for replacing the substrate atmosphere before deposition treatment with H_2 atmosphere after evacuation in order to improve the throughput characteristic. The next CVD reaction chamber 312 is a chamber for selective deposition on the substrate according to the Al-CVD method as described above under normal pressure or reduced pressure, in which a substrate holder 318 having a heat-generating member 317 which can heat the substrate to be formed to a range of 200 °C to 450 °C is provided internally, and starting gases such as alkylaluminum

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hydride bubbled and gasified in the bubbler 319-1 are introduced into the chamber through the starting gas introducing line 319 for CVD, and also hydrogen gas as the reactive gas is introduced through the gasline 319'. The next Rf etching chamber 313 is a chamber for carrying out cleaning of the substrate surface after selective deposition (etching) under Ar atmosphere, and internally thereof are provided at least a substrate holder 320 capable of heating the substrate to a range of 100 °C to 250 °C and an electrode line for Rf etching 321, and also an Ar gas feeding line 322 is connected. The next sputtering chamber 314 is a chamber for depositing non-selectively a metal film by sputtering under Ar atmosphere on the substrate surface, and internally thereof are provided a substrate holder 323 heated within a range of 200 °C to 250 °C and a target electrode 324 for mounting a sputter target material 324a, and also an Ar gas feeding line 325 is connected. The final loadlock chamber 315 is a control chamber before taking out the substrate after completion of the metal film deposition into the outer air, and constituted so that the atmosphere may be replaced with N_2.

Fig. 17 shows another constitutional example of a sequential metal film forming apparatus suitable for applying the film forming method as described

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above, and the same portions as described above in Fig. 16 are made the same symbols. The difference of the apparatus in Fig. 17 from that in Fig. 16 resides in that a halogen lamp 330 is provided as the direct heating means and the substrate surface can be directly heated, and for that purpose, the substrate holder 312 is provided with a nail 331 for holding the substrate under suspended state.

By heating directly the substrate surface with such constitution, the deposition speed can be further improved as described above.

The sequential metal film forming apparatus with the above constitution, as shown in Fig. 18, is substantially equivalent to one with the structure having the above loadlock chamber 311, the CVD reaction chamber 312, the Rf etching chamber 313, the sputtering chamber 314, the loadlock chamber 315 connected mutually to one another with the conveying chamber 326 as the relay chamber. With this constitution, the loadlock chamber 311 functions also as the loadlock chamber 315. In the above conveying chamber 326, as shown in the Figure, an arm 327 as the conveying means reversibly rotatable in the AA direction and stretchable in the BB direction is provided, and with the arm 327, as shown in the arrowhead in Fig. 19, the substrate can be moved following the steps successively from the loadlock

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chamber 311 to the CVD chamber 312, the Rf etching chamber 313, the sputtering chamber 314, the loadlock chamber 315 without exposure to outer air.

(Film Forming Procedure)

The film forming procedure for forming the electrode and wiring according to the present invention is described.

Fig. 20 is a schematic perspective view for illustration of the film forming procedure for formation of the electrode and wiring according to the present invention.

First, the outline is described. A semiconductor substrate having openings formed on an insulating film is prepared, which substrate is arranged in a film forming chamber, and its surface is maintained at, for example, 260 °C to 450 °C to deposit selectively Al at the portion where the semiconductor is exposed according to the hot CVD method in a mixed atmosphere of DMAH as the alkylaluminum hydride and hydrogen gas. Of course, as described above, a metal film composed mainly of Al such as Al-Si, etc. may be also deposited selectively by introducing a gas containing Si atoms, etc. Next, on the Al selectively deposited by the sputtering method and the insulating film, Al or a metal film composed mainly of Al is non-selectively formed. Then, by patterning of the metal film

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non-selectively deposited to a desired wiring shape, electrodes and wirings can be formed.

Referring next to Fig. 17 to Fig. 20, description is made in more detail. First, a substrate is prepared. As the substrate, for example, a single crystalline Si wafer having an insulating film provided with openings with respective apertures provided thereon is prepared.

Fig 20A is a schematic view showing a part of the substrate. Here, 401 is a single crystalline silicon substrate as a conductive substrate, 402 a thermally oxidized silicon film as the insulating film (layer). 403 and 404 are openings (exposed portions), having apertures different from each other. 410 is the groove bottom with Si exposed.

The procedure for forming Al film which becomes the electrode as the first wiring layer on the substrate is as follows with Fig. 20.

First, the substrate as described above is arranged in the loadlock chamber 311. Hydrogen is introduced into the loadlock chamber 311 to make it under hydrogen atmosphere. And, the reaction chamber 312 is internally evacuated to approximately 1×10^{-8} Torr by the evacuation system 316b. However, Al film can be formed even if the vacuum degree within the reaction chamber 312 may be worse than 1×10^{-8} Torr.

And, the gas of DMAH bubbled from the gas

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line 319 is fed. For the carrier gas for the DMAH line, H_2 is employed.

The second gas line 319' is for H_2 as the reaction gas, and by flowing H_2 through the second gas line 319' and controlling the opening degree of the slow leak valve not shown to adjust the pressure within the reaction chamber 312 to a predetermined value. A typical pressure in this case is preferably about 1.5 Torr. Through the DMAH line, DMAH is introduced into the reaction tube. The total pressure is made about 1.5 Torr, and the DMAH pressure 5.0×10^{-3} Torr. Then, current is passed to the halogen lamp 330 to heat directly the wafer. Thus, Al is selectively deposited.

After elapse of a predetermined deposition time, feeding of DMAH is once stopped. The predetermined deposition time of the Al film deposited in this process is the time until the thickness of the Al film on the Si (single crystalline silicon substrate 1) becomes equal to the film thickness of the SiO_2 (thermally oxidized silicon film 2), and can be determined previously by experimentation.

The temperature of the substrate surface by direct heating at this time is made about 270 °C. According to the steps up to this stage, the Al film 405 is selectively deposited within the openings and

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the grooves as shown in Fig. 20B.

All of the steps as described above are referred to as the first film forming step for formation of electrode within contact hole.

After the above first film forming step, the CVD reaction chamber 312 is evacuated until reaching a vacuum degree of 5×10^{-3} Torr or lower by the evacuation system 316b. At the same time, the Rf etching chamber 313 is evacuated to 5×10^{-6} Torr or lower. After confirmation that the both chambers have reached the above vacuum degree, the gate valve 310c is opened, the substrate moved from the CVD reaction chamber 312 to the Rf etching chamber 313 by the conveying means, and the gate valve 310c closed. The substrate is conveyed to the Rf etching chamber 313, and the Rf etching chamber 313 is evacuated by means of the evacuation system 316c until reaching a vacuum degree of 10^{-6} Torr or lower. Then, argon is fed through the argon feeding line 322 for Rf etching, and the Rf etching chamber 131 maintained under an argon atmosphere of 10^{-1} to 10^{-3} Torr. The substrate holder 320 of Rf etching is maintained at about 200 °C, Rf power of 100 W supplied to the electrode for Rf ethcing 321 for about 60 seconds, and discharging of argon is caused to occur within the Rf etching chamber 313 for about 60 seconds. By doing so, the surface of the

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substrate can be etched with argon ions to remove unnecessary surface layer of the CVD deposited film. The etching depth in this case is made about 100 Å in terms of the oxide. Here, surface etching of the CVD deposited film is effected in the Rf etching chamber, but since the surface layer of the CVD film of the substrate conveyed through vacuum contains no oxygen, etc., no Rf etching may be effected. In that case, the Rf etching chamber 313 function as the temperature changing chamber for effecting temperature change within a short time, when the temperatures in the CVD reaction chamber 12 and the sputtering chamber 314 are greatly different.

In the Rf etching chamber 313, after completion of Rf etching, flowing of argon is stopped, and the argon within the Rf etching chamber 313 is evacuated. After the Rf etching chamber 313 is evacuated to 5×10^{-6} Torr and the sputtering chamber 314 to 5×10^{-6} Torr or lower, the gate valve 310d is opened. Then, the substrate is moved from the Rf etching chamber 313 to the sputtering chamber 314 by means of a conveying means, followed by closing of the gate valve 310d.

After the substrate is conveyed to the sputtering chamber 314, the sputtering chamber 314 is made under an argon atmosphere of 10^{-1} to 10^{-3} Torr similarly as in the Rf etching chamber 313, and the

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temperature of the substrate holder 323 for mounting the substrate set to about 200 to 250 °C. And discharging of argon is effected at a DC power of 5 to 10 KW to cut a target material such as Al or Al-Si (Si: 0.5 %) and effect film formation of a metal such as Al, Al-Si, etc. at a deposition speed of about 10000 Å/min. on the substrate. This step is a non-selective deposition step. This is called the second film forming step for formation of the wiring to be connected to the electrode.

After formation of a metal film of about 5000 Å, flowing of argon and application of DC power are stopped. After evacuation of the loadlock chamber 311 to 5 x 10^{-3} Torr or lower, the gate valve 310e is opened and the substrate moved. After the gate valve 310e is closed, N_2 gas is permitted to flow into the loadlock chamber 311 until reaching atmospheric pressure, the gate valve 310f opened and the substrate taken out of the apparatus.

According to the second Al film deposition step as described above, the Al film 406 can be formed on the SiO_2 film 402.

And, by patterning the Al film 406 as shown in Fig. 20D, a wiring with a desired shape can be obtained.

(Experimental Examples)

In the following, how excellent is the

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above-described Al-CVD method is and how good of the quality the Al film deposited within the openings is are described based on the experimental results.

First, as the substrate, a plurality of N-type single crystalline silicon wafers were prepared, which are thermally oxidized on the surface to form SiO_2 of 8000 Å, and have various openings with various apertures from 0.25 μm x 0.25 μm square to 100 μm x 100 μm square patterned to have the subbing Si single crystal exposed (Sample 1-1).

These are subjected to formation of Al films according to the Al-CVD method under the conditions as described below. Under the common conditions by use of DMAH as the starting gas, and hydrogen as the reaction gas, a total pressure of 1.5 Torr, a DMAH partial presure of 5.0×10^{-3} Torr, the power amount passed through the halogen lamp is adjusted and the substrate surface temperature set within the range of 200 °C to 490 °C to form films.

The results are shown in Table 1.

Table 1

Substrate surface temperature(°C)	200	230	250	260	270	280	300	350	400	440	450	460	470	480	490
Deposition speed ($\mathring{A}$/min)	← 1000 - 1500			×			3000 - 5000								→
Line defect of Si	← Not recognized														→
Carbon content	← Not detected														→
Resistivity ($\Omega\mu$cm)	← 2.7 - 3.3			×				2.8 - 3.4							→
Reflectance (%)	← 85 - 95				×			90 - 95			×		- 60		→
Hillock density of 1 μm or more	← 1 - 10^2			×				0 - 10			×		10 - 10^4		→
Spike generation (destruction probability of 0.15 μm junction)	←	0									×		0 - 30		→

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As can be seen from Table 1, at a substrate surface temperature by direct heating of 260 °C or higher, Al is deposited selectively at a high deposition speed of 3000 to 5000 Å/min. within the openings.

When the characteristics of the Al film within the openings at substrate surface temperature range of 260 °C to 440 °C are examined, they are found to be excellent such that no carbon is contained, with resistivity being 2.8 to 3.4 μΩcm, reflectance 90 to 95 %, hillock density of 1 μm or higher 0 to 10 and substantially no spike generation (destruction probability of 0.15 μm junction).

In contrast, at substrate surface temperatures of 200 °C to 250 °C, the film is found to be considerably good as compared with the prior art although the film quality is slightly worse as compared with the case of 260 °C to 440 °C, but the deposition speed is 1000 to 1500 Å/min., which can never be said to be sufficiently high.

When the substrate surface temperature becomes 450 °C or higher, the characteristics of the Al film with the openings are lowered with the reflectance becoming 60 % or less, hillock density of 1 μm or more 10 to 10^4 cm^{-2}, alloy spike generation 0 to 30 %.

Next, description is made about how suitably

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the method as described above can be used openings such as contact hole or thru-hole.

That is, it can be also preferably applied to the contact hole/thru-hole structure comprising the material as described below.

On the Sample 1-1 as described above, an Al film is formed on a substrate (sample) as described below under the same conditions as when the Al film is formed.

On a single crystalline silicon as the first substrate surface material is formed a silicon oxide film according to the CVD method as the second substrate surface material, and patterning effected according to the photolithographic steps to have the single crystalline silicon surface partially exposed.

The film thickness of the thermally oxidized SiO_2 film has a film thickness of 8000 Å, the exposed portion of the single crystalline silicon a size of 0.25 μm x 0.25 μm to 100 μm x 100 μm. Thus, Sample 1-2 is prepared (hereinafter such samples are represented as "CVD SiO_2 (hereinafter abbreviated as SiO_2)/single crystalline silicon").

Sample 1-3 is boron doped oxide film formed by normal pressure CVD (hereinafter abbreviated as BSG)/single crystalline silicon,

Sample 1-4 phosphorus doped oxide film formed by normal pressure CVD (hereinafter abbreviated as

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PSG)/single crystalline silicon,

Sample 1-5 phosphorus and boron doped oxide film formed by normal pressure CVD (hereinafter abbreviated as BSPG)/single crystalline silicon,

Sample 1-6 nitride film formed by plasma CVD (hereinafter abbreviates as P-SIN)/single crystalline silicon,

Sample 1-7 hot nitride film (hereinafter abbreviated as T-SiN)/single crystalline silicon,

Sample 1-8 nitride film formed by low pressure CVD (hereinafter abbreviated as LP-SiN)/ single crystalline silicon,

Sample 1-9 nitride film formed by means of an ECR apparatus (hereinafter abbreviated as ECR-SiN)/ single crystalline silicon.

Further, according to all combinations of the first substrate surface materials (18 kinds) and the second substrate surface materials (9 kinds), Samnples 1-11 to 1-179 (note: Sample Nos. 1-10, 20, 30, 40, 50, 60, 70, 80, 90, 100, 110, 120, 130, 140, 150, 160, 170 are lacking) are prepared. As the first substrate surface material, single crystalline silicion (single crystalline Si), polycrystalline silicon (polycrystalline Si), amorphous silicon (amorphous Si), tungsten (W), molybdenum (Mo), tantalum (Ta), tungsten silicide (WSi), titanium silicide (TiSi), aluminum (Al), aluminum silicon

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(Al-Si), titanium aluminum (Al-Ti), titanium nitride (Ti-N), copper (Cu), aluminum silicon copper (Al-Si-Cu), aluminum palladium (Al-Pd), titanium (Ti), molybdenum silicide (Mo-Si), tantalum silicide (Ta-Si) are employed. As the second substrate surface material, T-SiO_2, SiO_2, BSG, PSG, BPSG, P-SiN, T-SiN, LP-SiN, ECR-SiN are employed. For all of the samples as described above, good Al films comparable with the sample 1-1 could be formed.

Next, on the substrate having Al deposited selectively as described above, Al is deposited non-selectively according to the sputtering method as described above, followed by patterning.

As the result, the Al film formed according to the sputtering method, and the Al film selectively selected within the openings are found to be under the contact state with both electrically and mechanically high durability due to good surface characteristic of the Al film.

(Experimental Examples)

Samples of semiconductor device are trially made according to the methods as described in Examples 1 to 8, and as the result of experimentation, good characteristics as expected can be obtained.

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WHAT IS CLAIMED IS:

1. A semiconductor device having a device region and a device separation region formed on a semiconductor substrate doped with impurities, and the device separation region having a metal wiring formed on the surface of said device region or the back surface of said substrate,

characterized in that an aluminum region extending in the longitudinal direction connected to said metal wiring is formed within said device separation region.

2. A semiconductor device having device separation region, which device having a device region and a metal region composed mainly of aluminum which becomes the device separation region extending out in the longitudinal direction formed on an insulating substrate, one end of the metal region being in contact with said insulating substrate and the other end with the surface exposed.

3. A semiconductor device according to Claim 1, wherein said semiconductor device is a solid image pick up device.

4. A semiconductor device, comprising a semiconductor substrate having at least two

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functional devices, and having a buried metal wiring layer for connecting said at least two functional devices provided internally of said semiconductor substrate.

5. A semiconductor device according to Claim 4, wherein further at least one metal wiring layer is laminated on said metal wiring layer.

6. A semiconductor device according to Claim 4, wherein the metal wiring layer provided within said semiconductor substrate is formed of a single crystalline aluminum.

7. A semiconductor device according to Claim 6, wherein said semiconductor substrate and the metal wiring layer provided within said substrate are electrically separated with a layer region of the conduction type opposite to that of said substrate.

8. A semiconductor device according to Claim 4, wherein said semiconductor device includes a logic circuit.

9. A semiconductor device according to Claim 2, wherein said semiconductor device is a solid image pick up device.

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10. A semiconductor device according to Claim 5, wherein the metal wiring layer provided within said semiconductor substrate is formed of a single crystalline aluminum.

11. A semiconductor device, comprising a plurality of active regions each separated one from the other by a device separation region, which device is characterised in that:
each device separation region is provided with a metal or metallic filling.

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DEVICE SEPARATION STRUCTURE AND SEMICONDUCTOR DEVICE IMPROVED IN WIRING STRUCTURE

ABSTRACT OF THE DISCLOSURE

A semiconductor device has a device region, and a device separation region formed on a semiconductor substrate doped with impurities. And, the device separation region has a metal wiring formed on the surface of the device region or the back surface of the substrate. An aluminum region extending in the longitudinal direction connected to the metal wiring is formed within the device separation region.

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(Fig. 3)

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FIG. 1A
PRIOR ART

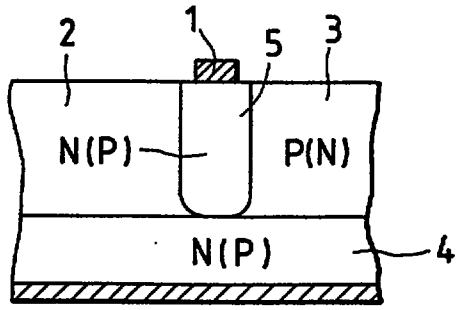


FIG. 1B
PRIOR ART

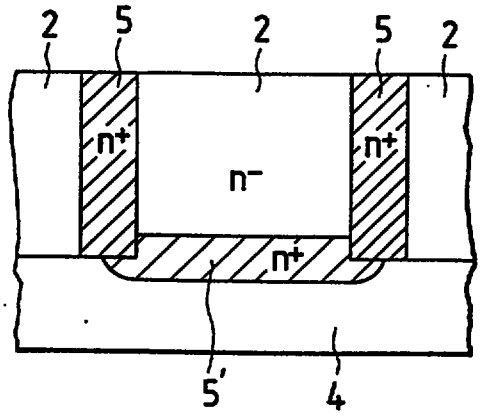


FIG. 2A
PRIOR ART

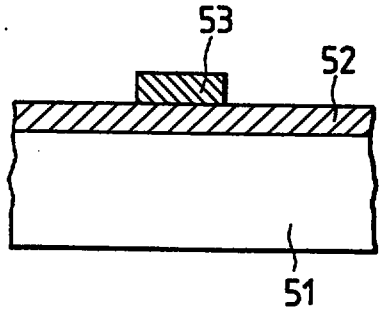
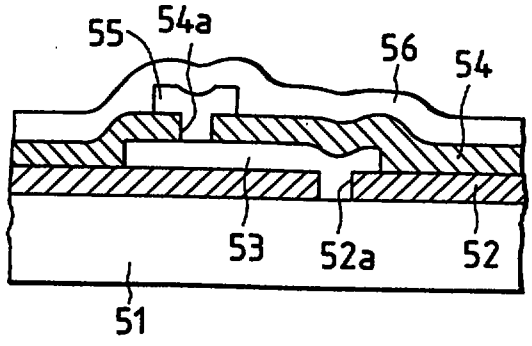


FIG. 2B
PRIOR ART



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FIG. 3

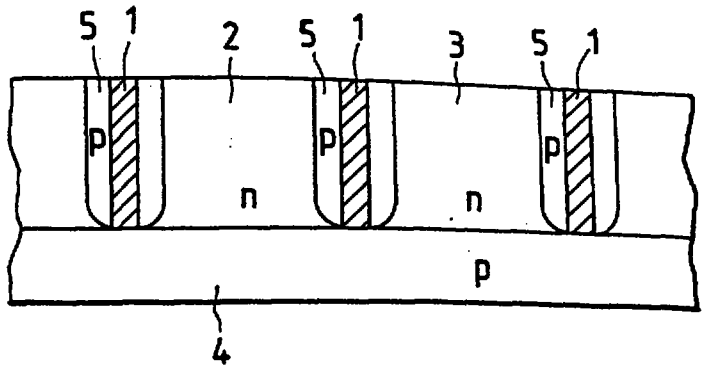


FIG. 4

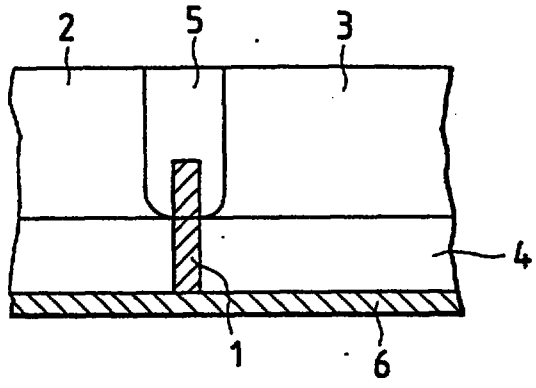
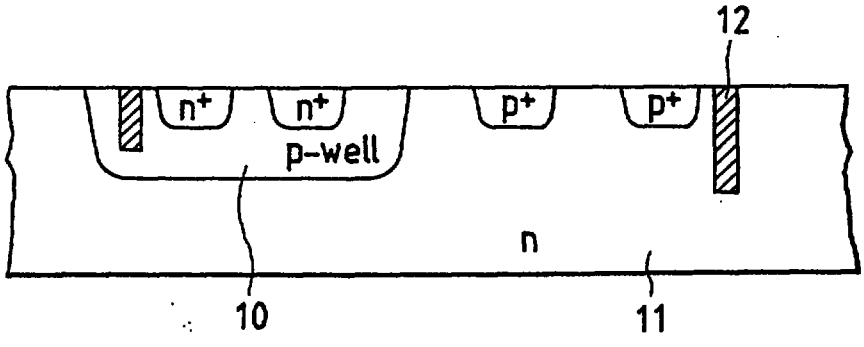


FIG. 5



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FIG. 6A

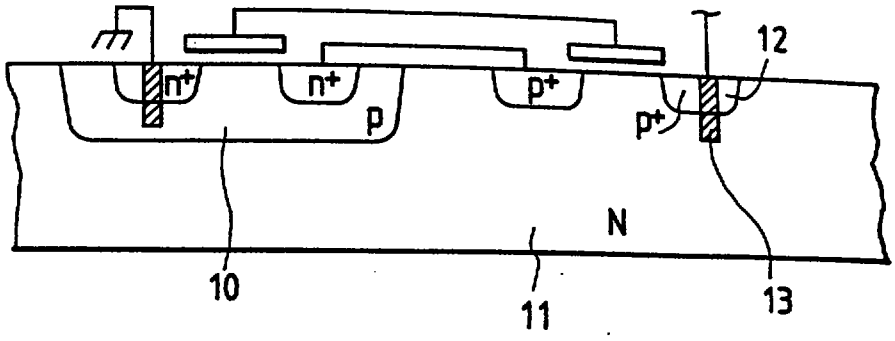
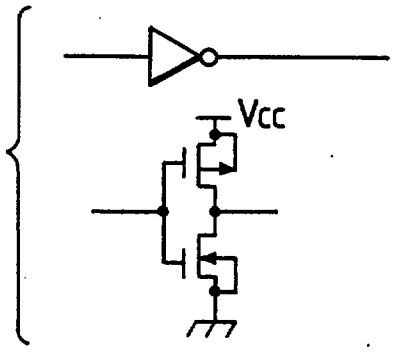


FIG. 6B



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FIG. 7A

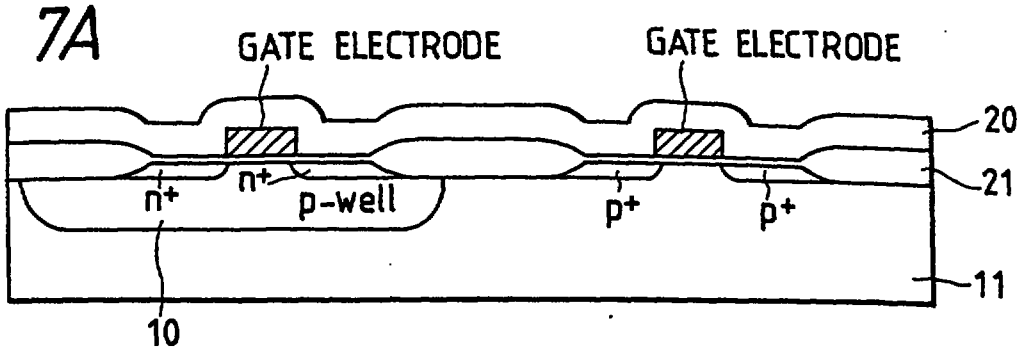


FIG. 7B

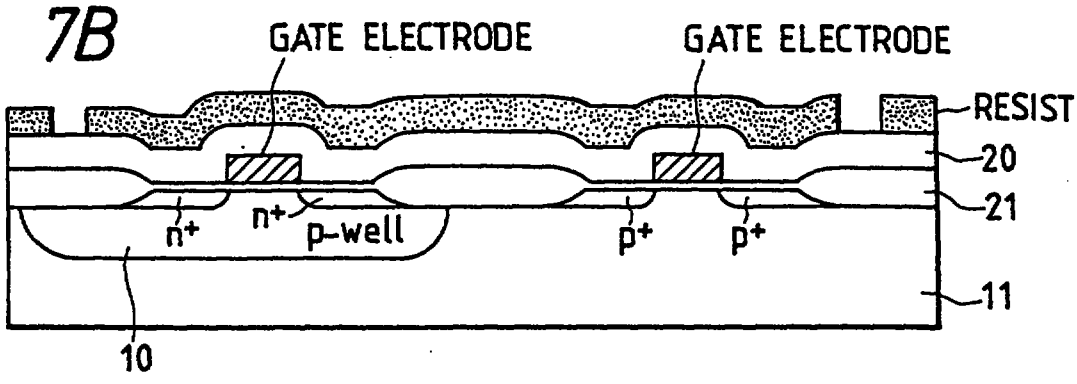


FIG. 7C

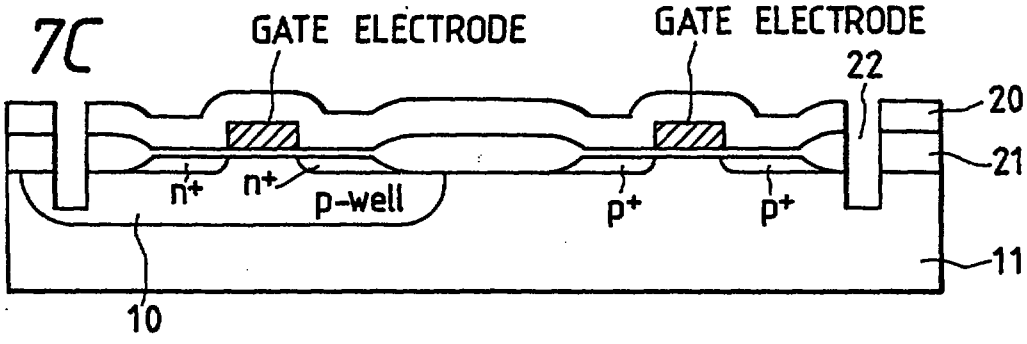
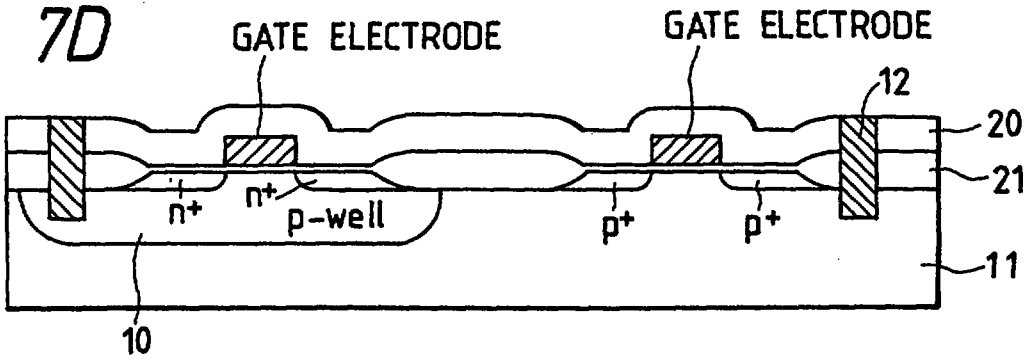


FIG. 7D



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FIG. 8

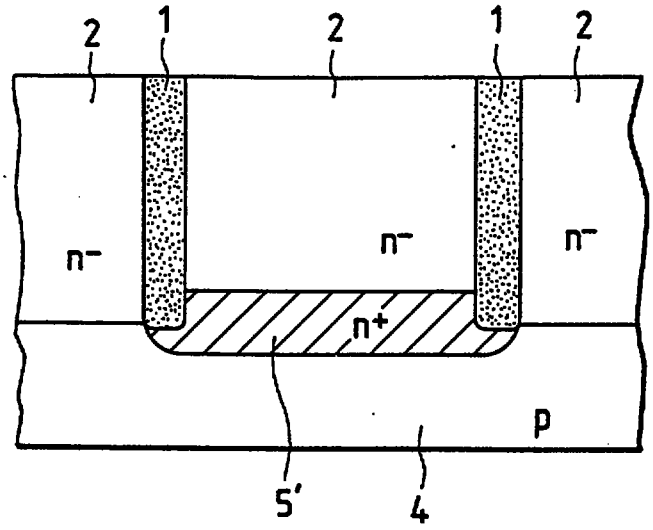
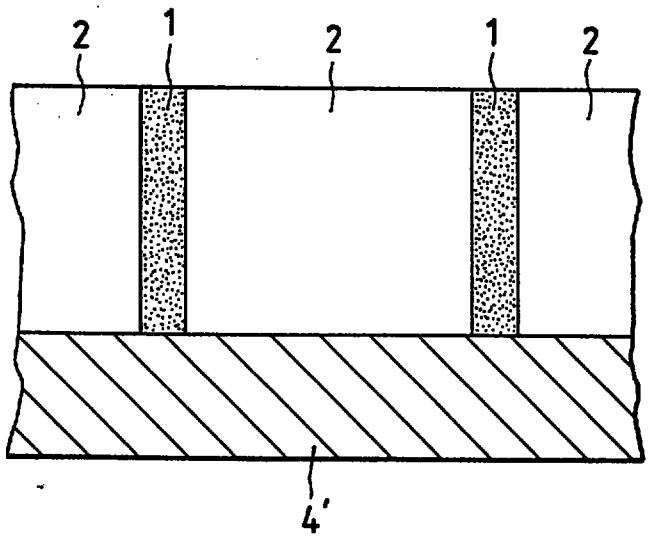


FIG. 9



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FIG. 10A

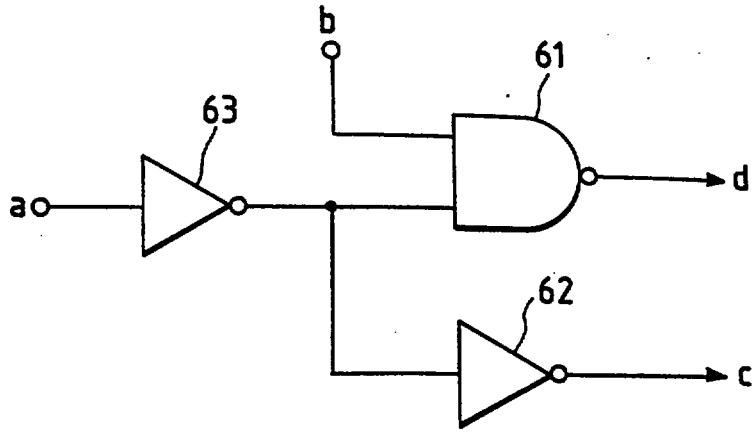
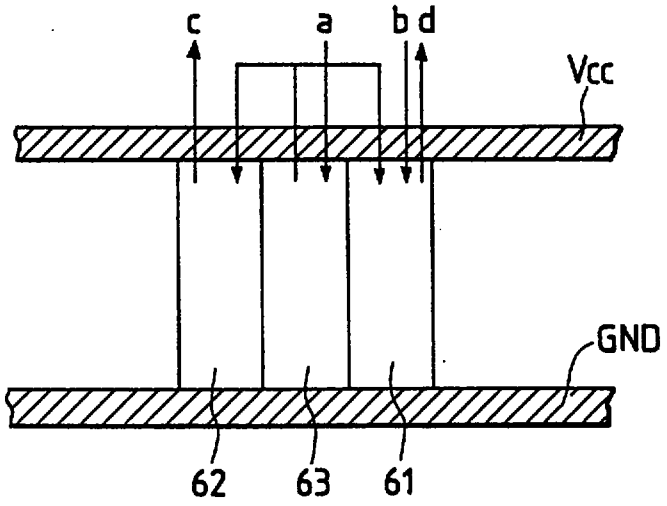
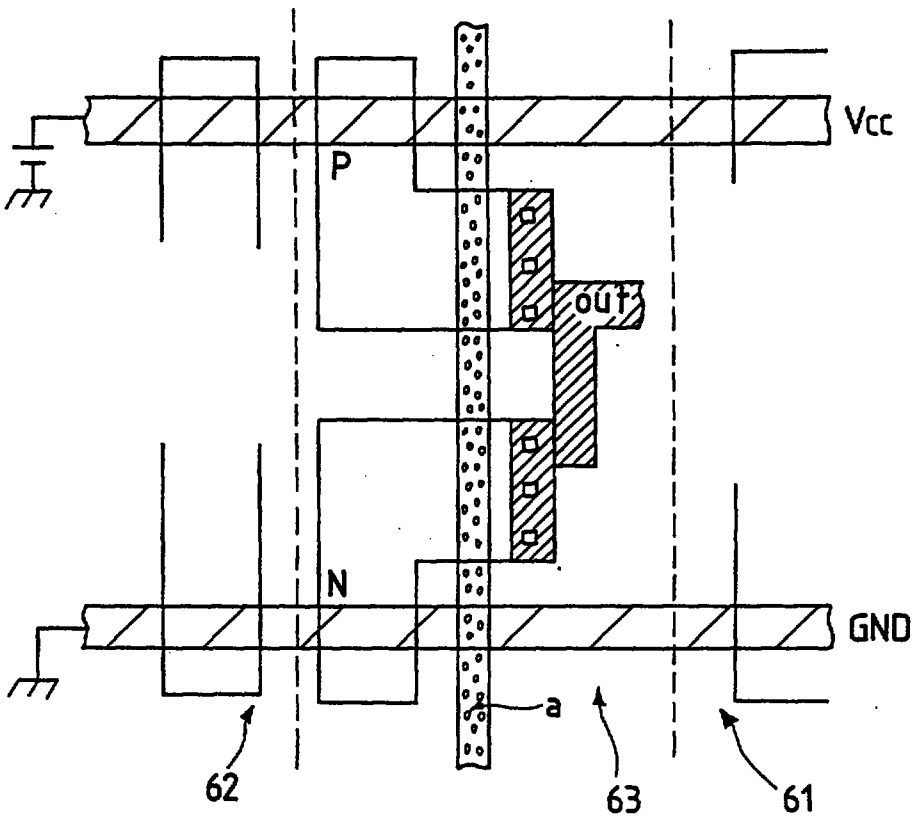


FIG. 10B



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FIG. 11



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FIG. 12

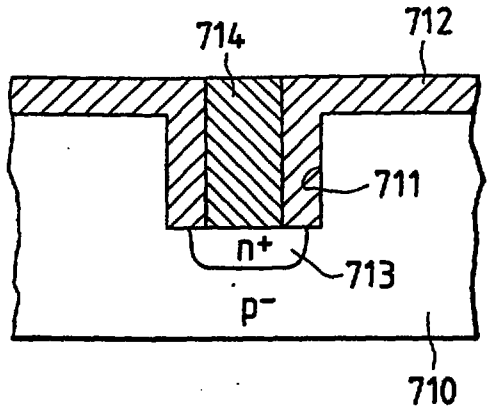


FIG. 13

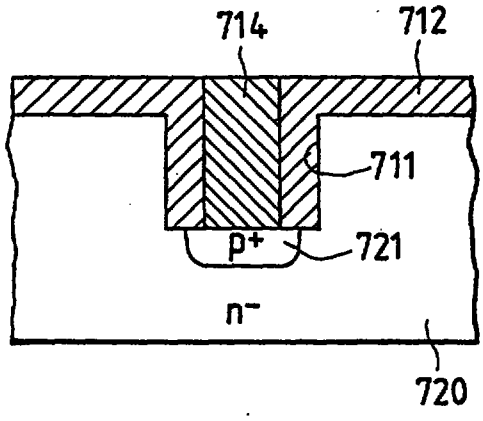
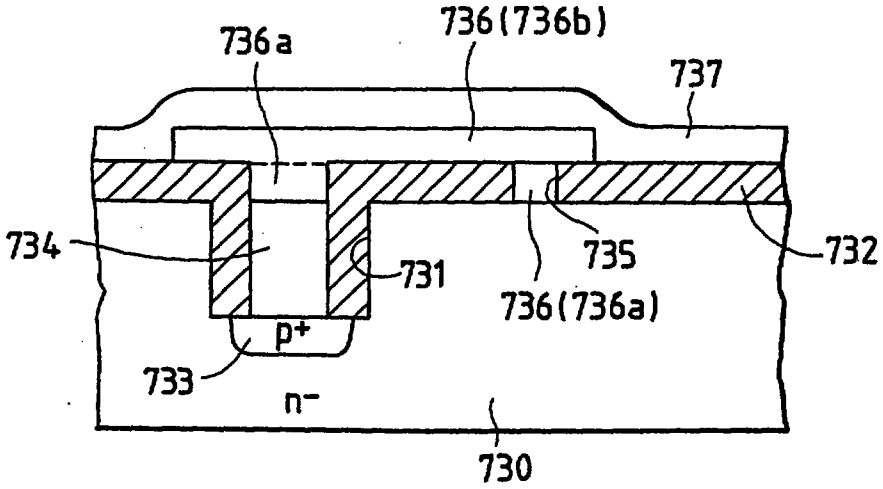


FIG. 14



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FIG. 15A

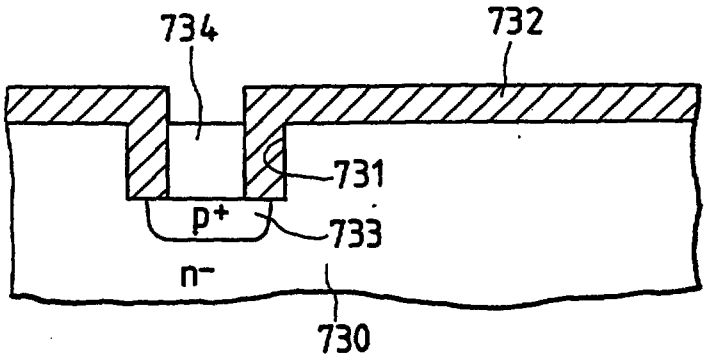


FIG. 15B

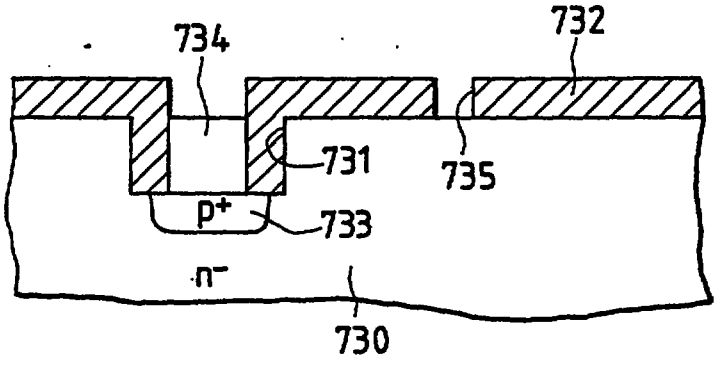
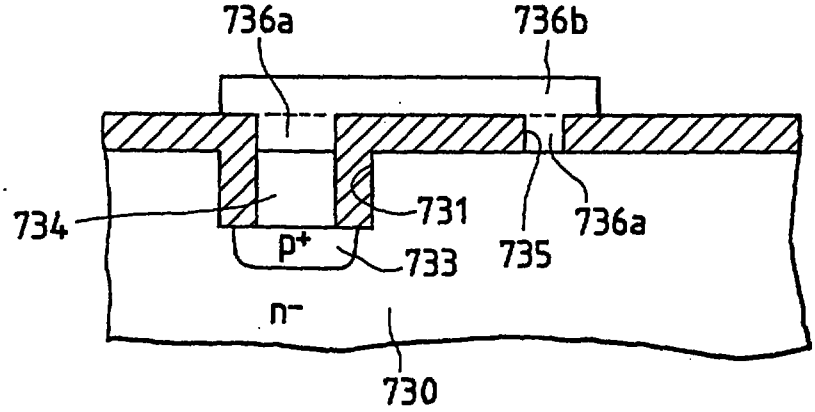


FIG. 15C



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FIG. 16

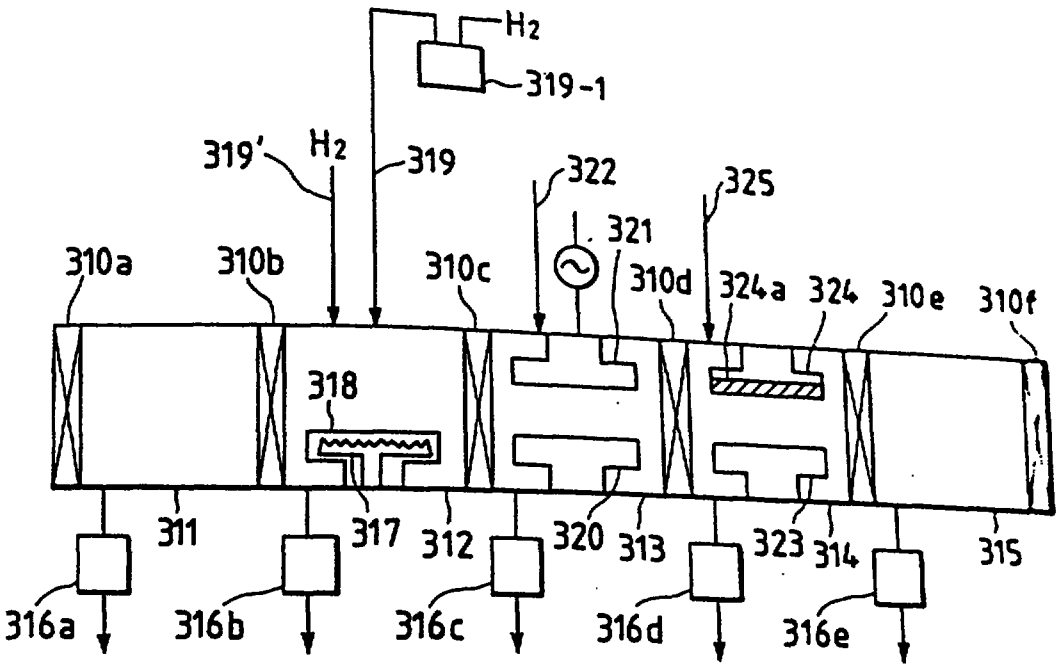
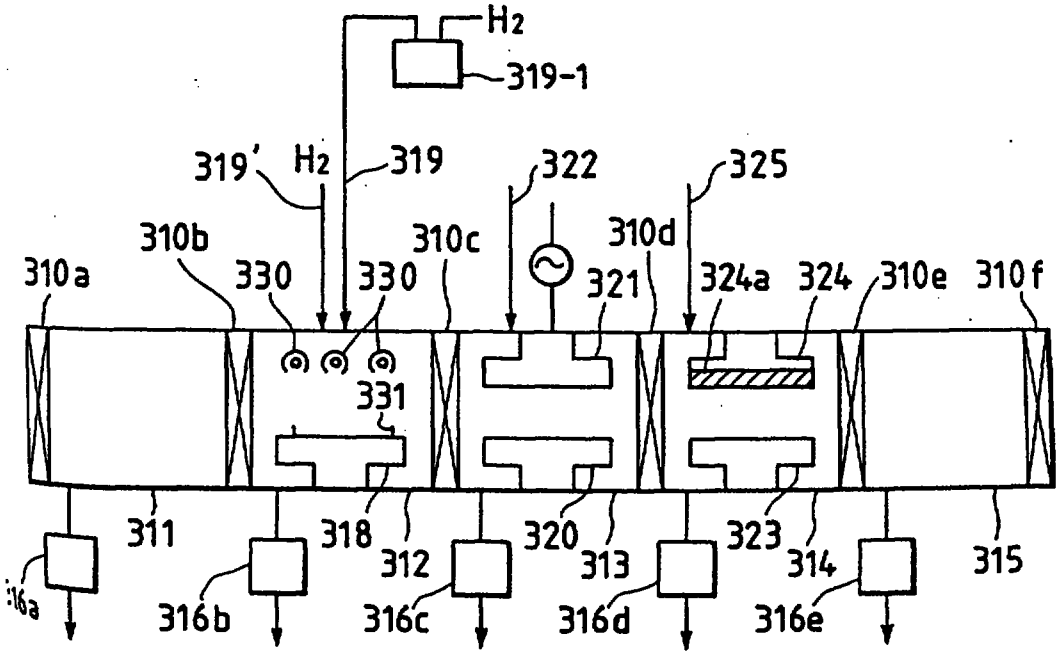


FIG. 17



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FIG. 18

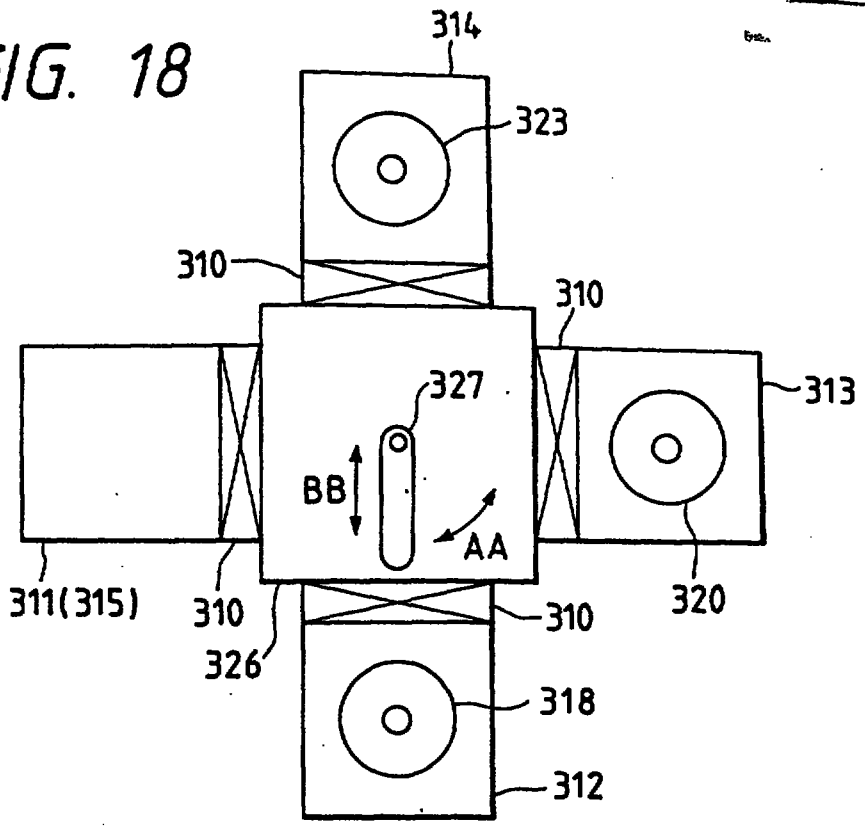
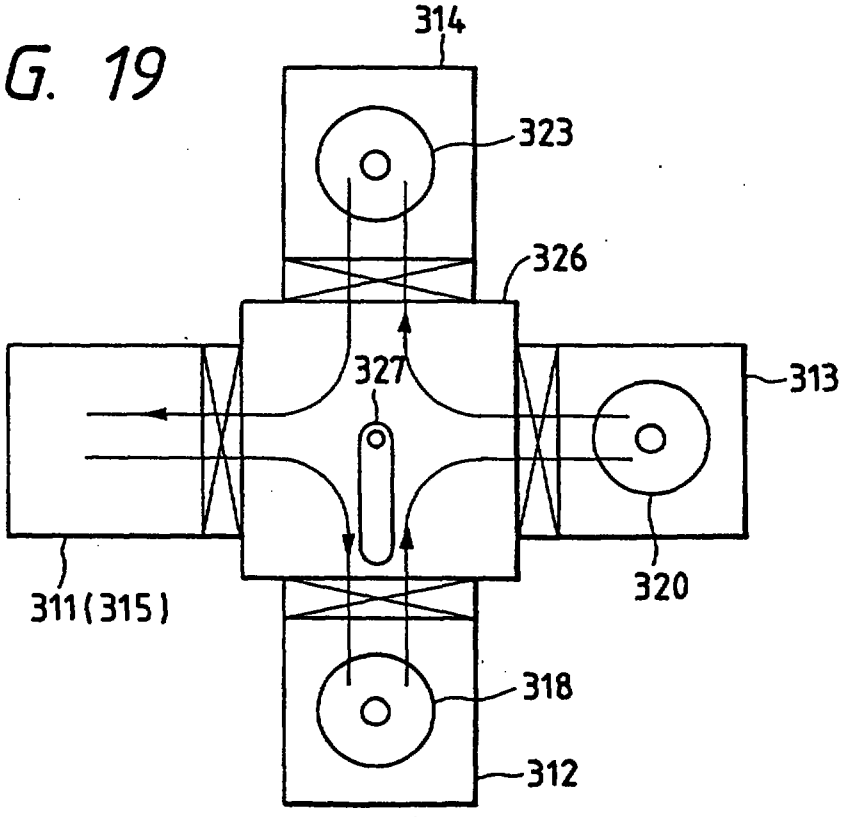


FIG. 19



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FIG. 20A

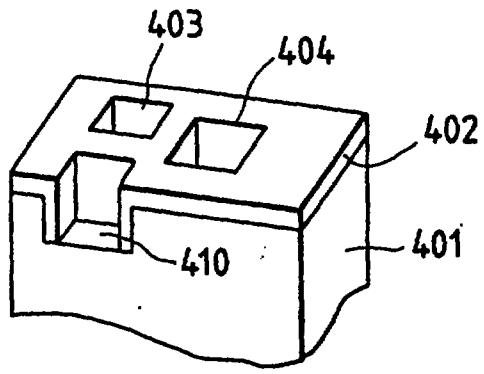


FIG. 20B

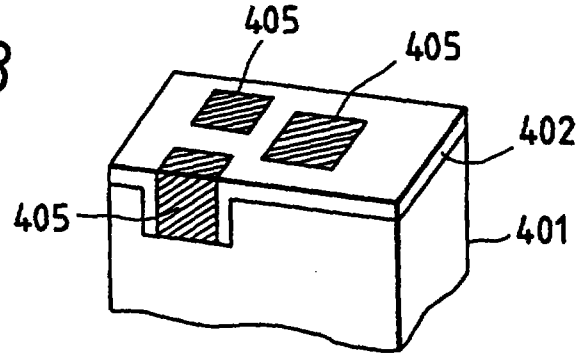


FIG. 20C

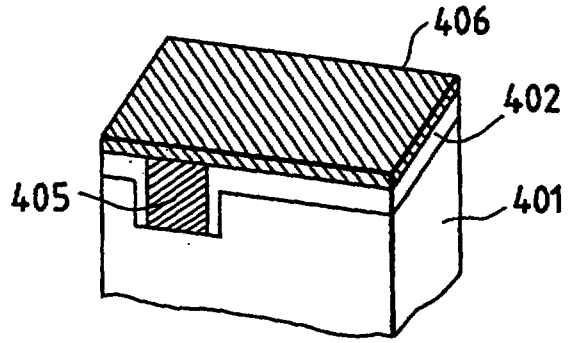
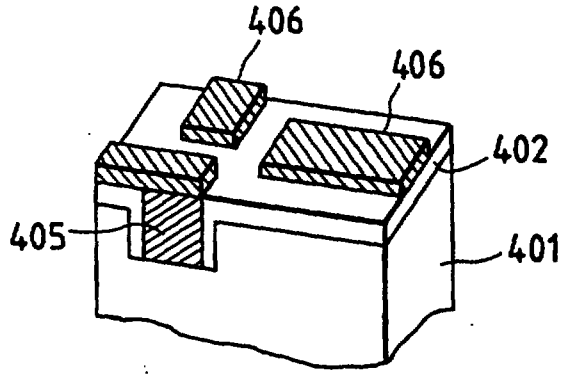


FIG. 20D



* C L M S *

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What is claimed is:

1. A semiconductor device comprising:

a semiconductor body;

a plurality of element regions formed within said semiconductor body;

an isolating region for making each of said element regions electrically independent;

wherein said isolation region comprises (i) a conductive region formed of single crystalline aluminum filling a groove at one surface side of said body, (ii) a doped region provided on a bottom of said groove and formed of a semiconductor material doped with an impurity to form a pn junction with said element region, and (iii) an insulating region disposed at side surfaces of said groove and said doped region.

2. A semiconductor device comprising:

a semiconductor body;

a plurality of element regions formed within said semiconductor body; and

an isolating region for making each of said element regions electrically independent;

wherein said isolating region comprises a conductive region formed of single crystalline aluminum filling a groove formed at one surface side of said semiconductor body, a region doped with an impurity disposed on side surfaces and bottom of said groove, and said doped region forms a pn junction with said element region.

3. A semiconductor device according to claim 1, wherein said semiconductor device is a solid-state image pick-up device.

4. A semiconductor device according to claim 1, further comprising at least two functional devices, and comprising a buried metal wiring layer for connecting said at least two functional devices provided within said semiconductor substrate.

5. A semiconductor device according to claim 4, further comprising at least a first metal wiring layer laminated on said metal wiring layer.

6. A semiconductor device according to claim 4, wherein said metal wiring layer within said semiconductor substrate is formed of a single crystalline aluminum.

* C L M S *

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7. A semiconductor device according to claim 6, wherein said semiconductor substrate and said metal wiring layer within said substrate are electrically separated by a layer region of a conduction type opposite to that of said substrate.

8. A semiconductor device according to claim 4, wherein said semiconductor device comprises a logic circuit.

9. A semiconductor device according to claim 2, wherein said semiconductor device is a solid-state image pick-up device.

10. A semiconductor device according to claim 5, wherein said metal wiring layer within said semiconductor substrate is formed of a single crystalline aluminum.

* * * * *

This Sheet Has Been Replaced

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Date : 30 DEC 1997

Subsequently, on the N^+ type diffusion layer 713, according to a conventional film forming method such as sputtering or the Al-CVD method, a metal wiring layer 714 comprising Al, etc. is formed. The metal wiring layer 714 should be desirably formed so that its upper may be coplanar with the upper surface of the insulation layer 712 formed on the surface of the substrate 710 around the groove 711 in accomplishing surface flattening of the semiconductor device. In such metal wiring layer 714, electrical separation is effected from the P^- type silicon substrate 710 through the insulation layer 712 as the insulation film formed on the inner surface of the groove 711 and the N+ type diffusion layer 713 as the P-N separation layer formed on the bottom of the groove 711.

According to the selective Al-CVD method as described above, the Al film is deposited selectively on the N^+ type diffusion layer 713 comprising silicon as described above, but not on the insulation layer 712 comprising silicon oxide. Therefore, by use of the selective Al-CVD method, there is the advantage that no patterning with resist, etc. as required in the case of a conventional film forming method such as sputtering, etc. need be applied. Also, the depth dimension of the groove 711 as described above is relatively longer than the width dimension, and even

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DEVICE SEPARATION STRUCTURE AND SEMICONDUCTOR DEVICE IMPROVED IN WIRING STRUCTURE

ABSTRACT OF THE DISCLOSURE

A semiconductor device has a device region, and a device separation region formed on a semiconductor substrate doped with impurities. And, the device separation region has a metal wiring formed on the surface of the device region or the back surface of the substrate. An aluminum region extending in the longitudinal direction connected to the metal wiring is formed within the device separation region.

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(Fig. 3)