ABSTRACT

A FILL PATTERN IN KERF AREAS TO PREVENT LOCALIZED NON-UNIFORMITIES OF INSULATING LAYERS AT DIE CORNERS ON SEMICONDUCTOR SUBSTRATES

A method for making a planar spin-on-glass (SOG) layer over integrated circuits at the corners of the chip (die) areas is achieved. This method allows more reliable integrated circuits to be made, and is particularly useful for liquid crystal displays (LCDs) by eliminating optical distortion at the corners of the LCD die areas. When a conducting layer is patterned to form portions of the integrated circuits over the chip areas, the layer is concurrently patterned to form a fill layer in the kerf areas. The spacing between the fill layer in the kerf areas and the edges of the patterned conducting layer in the die areas is selected to have a width sufficiently narrow to provide a uniform coating of SOG over the corners of the die areas without buildup of the SOG. After depositing a thin SiO_x cap layer, a uniform SOG layer is deposited. The fill layer in the kerf areas also prevents dishing of the SOG layer when the SOG is chem-mech polished back. The process steps of this invention can be repeated to provide multilevels of electrical interconnections as required to complete the integrated circuits without causing non-uniformity of the SOG at the die corners.

(FIGURE 6 IS SUGGESTED FOR PUBLICATION)