POWER AMPLIFICATION WITH REDUCED GAIN VARIATION

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application claims priority to U.S. Provisional Application No. 63/168,870 filed March 31, 2021, entitled POWER AMPLIFICATION WITH REDUCED GAIN VARIATION, the disclosure of which is hereby expressly incorporated by reference herein in its respective entirety.

BACKGROUND

Field

[0002] The present disclosure relates to power amplification of signals such as radio-frequency (RF) signals.

Description of the Related Art

[0003] In many radio-frequency (RF) applications, it is desirable to amplify a signal. In an example context of a transmit operation, such amplification of signal can provide power amplification of the signal, and the power-amplified signal can be transmitted from an RF device such as a wireless device.

SUMMARY

[0003a] In an aspect, the present disclosure refers to a power amplifier comprising: an input stage that includes an amplifying transistor having an input node and an output node, such that a signal at the input node has a first power level and an amplified signal at the output node has a second power level; a bias circuit configured to provide a bias signal to the amplifying transistor; a feedback circuit that couples the output node of the amplifying transistor to the input node of the amplifying transistor, the feedback circuit including a resistance and a capacitance arranged in series; and a gain compensation circuit implemented relative to the input stage such that the second power level is compensated for a variation in temperature associated with the power amplifier; wherein the gain compensation

circuit is implemented along the feedback circuit to adjust a gain of the input stage based on the variation in temperature; the gain compensation circuit includes a variable capacitance circuit configured to provide a variable capacitance value based on the variation in temperature; the variable capacitance circuit is configured to provide analog values based on the variation in temperature; the variable capacitance circuit includes a diode capacitance circuit controlled by a control signal that depends on the variation in temperature; the diode capacitance circuit includes a plurality of diodes and controlled by a control voltage to provide the variable capacitance value based on the variation in temperature; and the plurality of diodes includes a first diode and a second diode arranged such that an anode of the first diode is on an input side of the variable capacitance circuit, and anode of the second diode is on an output side of the variable capacitance circuit, and cathodes of the first and second diodes are coupled to each other, the control voltage being provided to a node between the cathodes of the first and second diodes.

[0003b] In an aspect, the present disclosure refers to a semiconductor die comprising: a substrate; and a power amplifier implemented on the substrate, the power amplifier including an input stage that includes an amplifying transistor having an input node and an output node, such that a signal at the input node has a first power level and an amplified signal at the output node has a second power level, the power amplifier further including a feedback circuit that couples the output node of the amplifying transistor to the input node of the amplifying transistor, the feedback circuit including a resistance and a capacitance arranged in series, the power amplifier further including a gain compensation circuit implemented relative to the input stage such that the second power level is compensated for a variation in temperature associated with the power amplifier; wherein the gain compensation circuit is implemented along the feedback circuit to adjust a gain of the input stage based on the variation in temperature; the gain compensation circuit includes a variable capacitance circuit configured to provide a variable capacitance value based on the variation in temperature; the variable capacitance circuit is configured to provide analog values based on the variation in temperature; the variable capacitance circuit includes a diode capacitance circuit controlled by a control signal that depends on the variation in temperature; the diode capacitance circuit includes a plurality of diodes and controlled by a control voltage to provide the

variable capacitance value based on the variation in temperature; and the plurality of diodes includes a first diode and a second diode arranged such that an anode of the first diode is on an input side of the variable capacitance circuit, and anode of the second diode is on an output side of the variable capacitance circuit, and cathodes of the first and second diodes are coupled to each other, the control voltage being provided to a node between the cathodes of the first and second diodes.

[0003c] In an aspect, the present disclosure refers to a packaged module comprising: a packaging substrate; and a semiconductor die mounted on the packaging substrate and including a power amplifier, the power amplifier including an input stage that includes an amplifying transistor having an input node and an output node, such that a signal at the input node has a first power level and an amplified signal at the output node has a second power level, the power amplifier further including a feedback circuit that couples the output node of the amplifying transistor to the input node of the amplifying transistor, the feedback circuit including a resistance and a capacitance arranged in series, the power amplifier further including a gain compensation circuit implemented relative to the input stage such that the second power level is compensated for a variation in temperature associated with the power amplifier; wherein the gain compensation circuit is implemented along the feedback circuit to adjust a gain of the input stage based on the variation in temperature; the gain compensation circuit includes a variable capacitance circuit configured to provide a variable capacitance value based on the variation in temperature; the variable capacitance circuit is configured to provide analog values based on the variation in temperature; the variable capacitance circuit includes a diode capacitance circuit controlled by a control signal that depends on the variation in temperature; the diode capacitance circuit includes a plurality of diodes and controlled by a control voltage to provide the variable capacitance value based on the variation in temperature; and the plurality of diodes includes a first diode and a second diode arranged such that an anode of the first diode is on an input side of the variable capacitance circuit, and anode of the second diode is on an output side of the variable capacitance circuit, and cathodes of the first and second diodes are coupled to each other, the control voltage being provided to a node between the cathodes of the first and second diodes.

[0003d] In an aspect, the present disclosure refers to a wireless device comprising: a transceiver configured to generate a signal; a power amplifier configured to amplify the signal, the power amplifier including an input stage that includes an amplifying transistor having an input node and an output node, such that a signal at the input node has a first power level and an amplified signal at the output node has a second power level, the power amplifier further including a feedback circuit that couples the output node of the amplifying transistor to the input node of the amplifying transistor, the feedback circuit including a resistance and a capacitance arranged in series, the power amplifier further including a gain compensation circuit implemented relative to the input stage such that the second power level is compensated for a variation in temperature associated with the power amplifier; and an antenna in communication with the power amplifier and configured to support transmission of the amplified signal provided by the power amplifier; wherein the gain compensation circuit is implemented along the feedback circuit to adjust a gain of the input stage based on the variation in temperature; the gain compensation circuit includes a variable capacitance circuit configured to provide a variable capacitance value based on the variation in temperature; the variable capacitance circuit is configured to provide analog values based on the variation in temperature; the variable capacitance circuit includes a diode capacitance circuit controlled by a control signal that depends on the variation in temperature; the diode capacitance circuit includes a plurality of diodes and controlled by a control voltage to provide the variable capacitance value based on the variation in temperature; and the plurality of diodes includes a first diode and a second diode arranged such that an anode of the first diode is on an input side of the variable capacitance circuit, and anode of the second diode is on an output side of the variable capacitance circuit, and cathodes of the first and second diodes are coupled to each other, the control voltage being provided to a node between the cathodes of the first and second diodes.

[0004] In accordance with an example, the present disclosure relates to a power amplifier that includes an input stage that includes an amplifying transistor having an input node and an output node, such that a signal at the input node has a first power level and an amplified signal at the output node has a second power level. The power amplifier further includes a bias circuit configured to provide a bias signal to the amplifying transistor, and a feedback

circuit that couples the output node of the amplifying transistor to the input node of the amplifying transistor. The feedback circuit includes a resistance and a capacitance arranged in series. The power amplifier further includes a gain compensation circuit implemented relative to the input stage such that the second power level is compensated for a variation in temperature associated with the power amplifier.

[0005] In some examples, the gain compensation circuit can be implemented along an input path to the input node of the amplifying transistor, such that the gain compensation circuit adjusts the first power level of the signal provided to the input node of the amplifying transistor based on the variation in temperature. The gain compensation circuit can include a variable attenuator configured to provide different attenuation values based on a control signal that depends on the variation in temperature.

[0006] In some examples, the gain compensation circuit can be implemented along an output path from the input node of the amplifying transistor, such that the gain compensation circuit adjusts the second power level of the amplified signal from the output node of the amplifying transistor based on the variation in temperature. The gain compensation circuit can include a variable attenuator configured to provide different attenuation values based on a control signal that depends on the variation in temperature.

[0007] In some examples, the gain compensation circuit can be implemented along the feedback circuit to adjust a gain of the input stage based on the variation in temperature. The gain compensation circuit can include a variable resistance circuit configured to provide a variable resistance value based on the variation in temperature. The variable resistance value can provide some or all of the resistance of the feedback circuit. The variable resistance circuit can be configured to provide a plurality of discrete values based on the variation in temperature.

[0008] In some examples, the variable resistance circuit can include a plurality of resistances arranged to be electrically parallel, with at least one of the plurality of resistances being configured to be switchable.

[0009] In some examples, the variable resistance circuit can be configured to provide analog values based on the variation in temperature. The variable resistance circuit can include a diode resistance circuit controlled by a control signal that depends on the variation in temperature. The variable resistance circuit can include a plurality of transistors arranged in series and controlled by a control voltage to provide the variable resistance value based on the variation in temperature. The control voltage being provided to the variable resistance circuit can depend on the variation in temperature. The plurality of transistors arranged in series can include a plurality of BiHEMT transistors.

[0010] In some examples, the gain compensation circuit can include a variable capacitance circuit configured to provide a variable capacitance value based on the variation in temperature. The variable capacitance value can provide some or all of the capacitance of the feedback circuit. The variable capacitance circuit can be configured to provide a plurality of discrete values based on the variation in temperature. The variable capacitance circuit can include a plurality of capacitances arranged to be electrically parallel, with at least one of the plurality of capacitances being configured to be switchable.

[0011] In some examples, the variable capacitance circuit can be configured to provide analog values based on the variation in temperature. The variable capacitance circuit can include a diode capacitance circuit controlled by a control signal that depends on the variation in temperature. The variable capacitance circuit can include a plurality of diodes and controlled by a control voltage to provide the variable capacitance value based on the variation in temperature. The control voltage being provided to the variable capacitance circuit can depend on the variation in temperature. The plurality of diodes can include a first diode and a second diode arranged such that an anode of the first diode is on an input side of the variable capacitance circuit, and anode of the second diode is on an output side of the variable capacitance circuit, and cathodes of the first and second diodes are coupled to each other, with the control voltage being provided to a node between the cathodes of the first and second diodes.

[0012] In some examples, the power amplifier can further include a second stage configured to further amplify the amplified signal from the input stage. In some examples, the second stage can include first and second amplifying transistors arranged in a cascode configuration.

[0013] In some examples, the bias circuit can be configured such that the bias signal provided to the amplifying transistor depends on the variation in temperature. The bias circuit can be configured to utilize a reference current to generate the bias signal, with the reference current depending on the variation in temperature.

[0014] In an example, the present disclosure relates to a semiconductor die that includes a substrate and a power amplifier implemented on the substrate. The power amplifier includes an input stage that includes an

amplifying transistor having an input node and an output node, such that a signal at the input node has a first power level and an amplified signal at the output node has a second power level. The power amplifier further includes a feedback circuit that couples the output node of the amplifying transistor to the input node of the amplifying transistor. The feedback circuit includes a resistance and a capacitance arranged in series. The power amplifier further includes a gain compensation circuit implemented relative to the input stage such that the second power level is compensated for a variation in temperature associated with the power amplifier.

[0015] In some examples, the power amplifier can further include a bias circuit configured to provide a bias signal to the amplifying transistor.

[0016] In an example, the present disclosure relates to a packaged module that includes a packaging substrate and a semiconductor die mounted on the packaging substrate and including a power amplifier. The power amplifier includes an input stage that includes an amplifying transistor having an input node and an output node, such that a signal at the input node has a first power level and an amplified signal at the output node has a second power level. The power amplifier further includes a feedback circuit that couples the output node of the amplifying transistor to the input node of the amplifying transistor. The feedback circuit includes a resistance and a capacitance arranged in series. The power amplifier further includes a gain compensation circuit implemented relative to the input stage such that the second power level is compensated for a variation in temperature associated with the power amplifier.

[0017] In some examples, the packaged module can further include a bias circuit configured to provide a bias signal to the amplifying transistor. In some examples, the bias circuit can be implemented on the semiconductor die.

[0018] In some examples, the packaged module can further include one or more passive devices with each generating at least some heat during operation of the power amplifier. The variation in temperature can result from either or both of operation of the power amplifier and use of the one or more passive devices.

In an example, the present disclosure relates to a wireless device that includes a transceiver configured to generate a signal, and a

WHAT IS CLAIMED IS:

1. A power amplifier comprising:

an input stage that includes an amplifying transistor having an input node and an output node, such that a signal at the input node has a first power level and an amplified signal at the output node has a second power level;

a bias circuit configured to provide a bias signal to the amplifying transistor;

a feedback circuit that couples the output node of the amplifying transistor to the input node of the amplifying transistor, the feedback circuit including a resistance and a capacitance arranged in series; and

a gain compensation circuit implemented relative to the input stage such that the second power level is compensated for a variation in temperature associated with the power amplifier;

wherein the gain compensation circuit is implemented along the feedback circuit to adjust a gain of the input stage based on the variation in temperature;

the gain compensation circuit includes a variable capacitance circuit configured to provide a variable capacitance value based on the variation in temperature;

the variable capacitance circuit is configured to provide analog values based on the variation in temperature;

the variable capacitance circuit includes a diode capacitance circuit controlled by a control signal that depends on the variation in temperature;

the diode capacitance circuit includes a plurality of diodes and controlled by a control voltage to provide the variable capacitance value based on the variation in temperature; and

the plurality of diodes includes a first diode and a second diode arranged such that an anode of the first diode is on an input side of the variable capacitance circuit, and anode of the second diode is on an output side of the variable capacitance circuit, and cathodes of the first and second

diodes are coupled to each other, the control voltage being provided to a node between the cathodes of the first and second diodes.

2. The power amplifier of claim 1 wherein the gain compensation circuit includes a variable resistance circuit configured to provide a variable resistance value based on the variation in temperature.

3. The power amplifier of claim 2 wherein the variable resistance value provides some or all of the resistance of the feedback circuit.

4. The power amplifier of claim 2 wherein the variable resistance circuit is configured to provide a plurality of discrete values based on the variation in temperature.

5. The power amplifier of claim 4 wherein the variable resistance circuit includes a plurality of resistances arranged to be electrically parallel, at least one of the plurality of resistances configured to be switchable.

6. The power amplifier of claim 2 wherein the variable resistance circuit is configured to provide analog values based on the variation in temperature.

7. The power amplifier of claim 6 wherein the variable resistance circuit includes a diode resistance circuit controlled by a control signal that depends on the variation in temperature.

8. The power amplifier of claim 6 wherein the variable resistance circuit includes a plurality of transistors arranged in series and controlled by a control voltage to provide the variable resistance value based on the variation in temperature.

9. The power amplifier of claim 8 wherein the control voltage being provided to the variable resistance circuit depends on the variation in temperature.

10. The power amplifier of claim 8 wherein the plurality of transistors arranged in series includes a plurality of BiHEMT transistors.

11. The power amplifier of claim 1 wherein the variable capacitance value provides some or all of the capacitance of the feedback circuit.

12. The power amplifier of claim 1 wherein the variable capacitance circuit is configured to provide a plurality of discrete values based on the variation in temperature.

13. The power amplifier of claim 12 wherein the variable capacitance circuit includes a plurality of capacitances arranged to be electrically parallel, at least one of the plurality of capacitances configured to be switchable.

14. The power amplifier of claim 1 wherein the control voltage being provided to the variable capacitance circuit depends on the variation in temperature.

15. The power amplifier of claim 1 further comprising a second stage configured to further amplify the amplified signal from the input stage.

16. The power amplifier of claim 15 wherein the second stage includes first and second amplifying transistors arranged in a cascode configuration.

17. The power amplifier of claim 1 wherein the bias circuit is configured such that the bias signal provided to the amplifying transistor depends on the variation in temperature.

18. The power amplifier of claim 17 wherein the bias circuit is configured to utilize a reference current to generate the bias signal, the reference current depending on the variation in temperature.

19. A semiconductor die comprising:

a substrate; and

a power amplifier implemented on the substrate, the power amplifier including an input stage that includes an amplifying transistor having an input node and an output node, such that a signal at the input node has a first power level and an amplified signal at the output node has a second power level, the power amplifier further including a feedback circuit that couples the output node of the amplifying transistor to the input node of the amplifying transistor, the feedback circuit including a resistance and a capacitance arranged in series, the power amplifier further including a gain compensation circuit implemented relative to the input stage such that the second power level is compensated for a variation in temperature associated with the power amplifier;

wherein the gain compensation circuit is implemented along the feedback circuit to adjust a gain of the input stage based on the variation in temperature;

the gain compensation circuit includes a variable capacitance circuit configured to provide a variable capacitance value based on the variation in temperature;

the variable capacitance circuit is configured to provide analog values based on the variation in temperature;

the variable capacitance circuit includes a diode capacitance circuit controlled by a control signal that depends on the variation in temperature;

the diode capacitance circuit includes a plurality of diodes and controlled by a control voltage to provide the variable capacitance value based on the variation in temperature; and

the plurality of diodes includes a first diode and a second diode arranged such that an anode of the first diode is on an input side of the variable capacitance circuit, and anode of the second diode is on an output side of the variable capacitance circuit, and cathodes of the first and second diodes are coupled to each other, the control voltage being provided to a node between the cathodes of the first and second diodes.

20. The semiconductor die of claim 19 wherein the power amplifier further includes a bias circuit configured to provide a bias signal to the amplifying transistor.

21. A packaged module comprising:

a packaging substrate; and

a semiconductor die mounted on the packaging substrate and including a power amplifier, the power amplifier including an input stage that includes an amplifying transistor having an input node and an output node, such that a signal at the input node has a first power level and an amplified signal at the output node has a second power level, the power amplifier further including a feedback circuit that couples the output node of the amplifying transistor to the input node of the amplifying transistor, the feedback circuit including a resistance and a capacitance arranged in series, the power amplifier further including a gain compensation circuit implemented relative to the input stage such that the second power level is compensated for a variation in temperature associated with the power amplifier;

wherein the gain compensation circuit is implemented along the feedback circuit to adjust a gain of the input stage based on the variation in temperature;

the gain compensation circuit includes a variable capacitance circuit configured to provide a variable capacitance value based on the variation in temperature;

the variable capacitance circuit is configured to provide analog values based on the variation in temperature;

the variable capacitance circuit includes a diode capacitance circuit controlled by a control signal that depends on the variation in temperature;

the diode capacitance circuit includes a plurality of diodes and controlled by a control voltage to provide the variable capacitance value based on the variation in temperature; and

the plurality of diodes includes a first diode and a second diode arranged such that an anode of the first diode is on an input side of the variable capacitance circuit, and anode of the second diode is on an output side of the variable capacitance circuit, and cathodes of the first and second diodes are coupled to each other, the control voltage being provided to a node between the cathodes of the first and second diodes.

22. The packaged module of claim 21 further comprising a bias circuit configured to provide a bias signal to the amplifying transistor.

23. The packaged module of claim 22 wherein the bias circuit is implemented on the semiconductor die.

24. The packaged module of claim 21 further comprising one or more passive devices each generating at least some heat during operation of the power amplifier.

25. The packaged module of claim 24 wherein the variation in temperature results from either or both of operation of the power amplifier and use of the one or more passive devices.

26. A wireless device comprising:

a transceiver configured to generate a signal;

a power amplifier configured to amplify the signal, the power amplifier including an input stage that includes an amplifying transistor having an input node and an output node, such that a signal at the input node has a first power level and an amplified signal at the output node has a second power level, the power amplifier further including a feedback circuit that couples the output node of the amplifying transistor to the input node of the amplifying transistor, the feedback circuit including a resistance and a capacitance arranged in series, the power amplifier further including a gain compensation circuit implemented relative to the input stage such that the second power level is compensated for a variation in temperature associated with the power amplifier; and

an antenna in communication with the power amplifier and configured to support transmission of the amplified signal provided by the power amplifier;

wherein the gain compensation circuit is implemented along the feedback circuit to adjust a gain of the input stage based on the variation in temperature;

the gain compensation circuit includes a variable capacitance circuit configured to provide a variable capacitance value based on the variation in temperature;

the variable capacitance circuit is configured to provide analog values based on the variation in temperature;

the variable capacitance circuit includes a diode capacitance circuit controlled by a control signal that depends on the variation in temperature;

the diode capacitance circuit includes a plurality of diodes and controlled by a control voltage to provide the variable capacitance value based on the variation in temperature; and

the plurality of diodes includes a first diode and a second diode arranged such that an anode of the first diode is on an input side of the variable capacitance circuit, and anode of the second diode is on an output side of the variable capacitance circuit, and cathodes of the first and second diodes are coupled to each other, the control voltage being provided to a node between the cathodes of the first and second diodes.