CLAIMS

1. A memory circuit, arranged adjacent to a data transmission region and comprising:

at least one memory structure arranged parallel to the data transmission region, wherein the memory structure comprises a first memory array and a second memory array arranged adjacent to each other in a first direction, a distance between the first memory array and the data transmission region is less than a distance between the second memory array and the data transmission region, and the first direction is a direction of approaching the data transmission region; and

the first memory array comprises a read/write module and a forwarding module; the second memory array comprises a read/write module; the first memory array performs a data interaction with the data transmission region based on the read/write module in the first memory array; and the second memory array performs a data transmission with the data transmission region based on the read/write module in the second memory array and the forwarding module in the first memory array, a data transmission path between the first memory array and the data transmission region is separated from another data transmission path between the second memory array and the data transmission region.

2. The memory circuit according to claim 1, wherein the first memory array and the second memory array each comprise an even number of memory blocks that are successively arranged in the first direction, two adjacent non-repeated memory blocks share one read/write module, and the read/write module is arranged between two corresponding memory blocks.

3. The memory circuit according to claim 2, wherein the memory block further comprises a plurality of memory sub-blocks successively arranged in a second direction perpendicular to the first direction, and the plurality of memory sub-blocks share one read/write module.

4. The memory circuit according to claim 1 or 2, wherein the read/write module

in the first memory array and the read/write module in the second memory array are arranged in the first direction, and in a second direction perpendicular to the first direction, the forwarding module is arranged at a corresponding side of the read/write module.

5. The memory circuit according to claim 4, wherein one forwarding module is arranged at a corresponding side of each read/write module.

6. The memory circuit according to claim 1, wherein data transmission wires between the read/write module and the data transmission region and data transmission wires between the forwarding module and the data transmission region are arranged between adjacent power supply wires; and the power supply wire is configured to receive and transmit a power supply signal, to provide the power supply signal to the first memory array and the second memory array.

7. The memory circuit according to claim 6, wherein the data transmission wires comprise a low-bit transmission wire and a high-bit transmission wire, the low-bit transmission wire is configured to transmit low-bit data in a memory array, and the high-bit transmission wire is configured to transmit high-bit data in the memory array.

8. A data transmission circuit, arranged in a data transmission region and comprising:

at least two data transmission structures, wherein each of the data transmission structures is connected to at least one memory circuit according to any one of claims 1 to 7 and is configured to read data from the memory circuit and write data into the memory circuit;

each of the data transmission structures comprises a memory transmission terminal, a bus transmission terminal, and an interactive transmission terminal; the memory transmission terminal is configured to connect the memory circuit, the bus transmission terminal is configured to connect a data bus, and the interactive transmission terminal is configured to connect another one of the data transmission structures;

data inputted from the memory transmission terminal is outputted through the bus transmission terminal or the interactive transmission terminal;

data inputted from the bus transmission terminal is outputted through the memory transmission terminal or the interactive transmission terminal;

data inputted from the interactive transmission terminal is outputted through the bus transmission terminal or the memory transmission terminal; and the data inputted from the interactive transmission terminal is data inputted through the bus transmission terminal or the memory transmission terminal of the another one of the data transmission structures; and

a control module, connected to the data transmission structure and receiving an input control signal and an adjustment control signal that are provided by a memory that the control module belongs to; wherein the control module is configured to output the input control signal in a delayed manner based on the adjustment control signal, so as to generate an output control signal corresponding to the input control signal, and the input control signal and the output control signal are used for indicating a data transmission path of the data transmission structure.

9. The data transmission circuit according to claim 8, wherein the data transmission structure comprises:

an input unit, configured to receive at least one piece of input data and the input control signal, and output input data corresponding to the input control signal based on the input control signal;

an output unit, configured to receive the input data outputted by the input unit and at least one output control signal, and output input data based on a valid port represented by the output control signal; and

a latch unit, connected to the output unit and configured to latch the input data outputted by the output unit.

10. The data transmission circuit according to claim 9, wherein the input unit comprises:

a plurality of input controllers, wherein each of the input controllers corresponds to the memory transmission terminal, the bus transmission terminal, or the interactive transmission terminal;

each of the input controllers is configured to correspondingly receive the input data from the memory transmission terminal, the bus transmission terminal or the interactive transmission terminal and the input control signal; and

the input controller is configured to be turned on based on the input control signal, to output the input data.

11. The data transmission circuit according to claim 9, wherein the output unit comprises:

a plurality of output controllers, wherein each of the output controllers corresponds to the memory transmission terminal, the bus transmission terminal or the interactive transmission terminal;

each of the output controllers is configured to receive the input data outputted by the input unit corresponding to the memory transmission terminal, the bus transmission terminal or the interactive transmission terminal and the output control signal; and

the output controller is configured to be turned on based on the output control signal, to output the input data.

12. The data transmission circuit according to claim 9, wherein the data transmission structure further comprises:

an input selection unit, configured to receive at least one input control signal, and generate a strobe corresponding to the input control signal, wherein the strobe corresponds to a valid port represented by the input control signal, and a selection delay exists between the strobe and the input control signal; and

a trigger unit, comprising a clock terminal connected to the input selection unit, an input terminal connected to the input unit, and an output terminal connected to the output unit, and configured to transmit, based on the strobe, input data received by the input terminal to the output terminal.

13. The data transmission circuit according to claim 12, wherein the input selection unit comprises:

a trigger sub-unit, configured to receive the at least one input control signal, and generate an indication signal if the input control signal is received;

a delay sub-unit. connected to the trigger sub-unit, and configured to delay the indication signal; and

a conversion sub-unit, connected to the delay sub-unit, and configured to convert the indication signal delayed into the strobe.

14. The data transmission circuit according to claim 12, wherein the data transmission structure further comprises: an inverter unit, disposed between the trigger unit and the input unit, and configured to output the input data or invert and output the input data based on an inversion control signal.

15. The data transmission circuit according to claim 14, wherein the inverter unit comprises:

a flip control sub-unit, configured to receive the inversion control signal, and generate a first control signal and a second control signal based on the inversion control signal; and

a first selection sub-unit and a second selection sub-unit connected in parallel, wherein an input terminal of the first selection sub-unit and an input terminal of the second selection sub-unit are configured to receive the input data, and an output terminal of the first selection sub-unit and an output terminal of the second selection sub-unit are connected to the trigger unit;

the first selection sub-unit is configured to be turned on based on the first control signal, and invert and output the input data; and

the second selection sub-unit is configured to be turned on based on the second control signal, and output the input data.

16. The data transmission circuit according to claim 8, wherein the memory transmission terminal comprises a first transmission terminal, a second transmission terminal, a third transmission terminal, and a fourth transmission terminal; the bus transmission terminal comprises a fifth transmission terminal and a sixth transmission terminal; the interactive transmission terminal comprises a seventh transmission terminal and an eighth transmission terminal; and

the first transmission terminal and the second transmission terminal are connected

to the first memory array; the third transmission terminal and the fourth transmission terminal are connected to the second memory array; the first transmission terminal and the third transmission terminal are configured to transmit low-bit data; the second transmission terminal and the fourth transmission terminal are configured to transmit high-bit data; the fifth transmission terminal and the sixth transmission terminal are configured to perform an interactive data transmission between the data bus and the data transmission structure that the fifth transmission terminal and the sixth transmission terminal belong to; and the seventh transmission terminal and the eighth transmission terminal are configured to perform an interactive data transmission between two data transmission structures.

17. The data transmission circuit according to claim 16, wherein

the fifth transmission terminal is configured to perform the interactive data transmission between the data bus and the data transmission structure that the fifth transmission terminal belongs to; and

the sixth transmission terminal is configured to perform a one-way data transmission from the data transmission structure, that the sixth transmission terminal belongs to, to the data bus.

18. A memory, adopting the memory circuit according to any one of claims 1 to 7 to arrange memory arrays.