WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a semiconductor substrate comprising a chip region and an edge region;

a lower dielectric layer on the semiconductor substrate;

a chip pad on the lower dielectric layer of the chip region;

an upper dielectric layer on the lower dielectric layer, the upper dielectric layer comprising a first opening exposing the chip pad on the chip region and a second opening exposing the lower dielectric layer on the edge region; and

a redistribution pad connected to the chip pad, the redistribution pad comprising a via portion in the first opening and a pad portion extending from the via portion onto the upper dielectric layer;

wherein the lower dielectric layer has a first thickness on the chip region and a portion of the lower dielectric layer on the edge region has a second thickness, the second thickness being less than the first thickness.

2. The semiconductor device of claim 1, wherein the lower dielectric layer comprises a dielectric material whose dielectric constant is less than that of the upper dielectric layer.

3. The semiconductor device of claim 1, wherein, on the edge region, the lower dielectric layer comprises a first segment having the first thickness and a second segment having the second thickness.

4. The semiconductor device of claim 1, further comprising a redistribution spacer that is on a sidewall of the second opening and comprises a same material as that of the redistribution pad.

5. The semiconductor device of claim 1, further comprising:

a semiconductor integrated circuit on the chip region of the semiconductor substrate;

a test structure on the edge region of the semiconductor substrate; and

a metal line connecting the semiconductor integrated circuit and the chip pad to each other,

wherein the lower dielectric layer is on the semiconductor integrated circuit, the test structure, and the metal line.

6. The semiconductor device of claim 5, wherein the second opening of the upper dielectric layer overlaps the test structure in a cross sectional view of the semiconductor device.

7. The semiconductor device of claim 1, wherein the upper dielectric layer comprises:

a first upper dielectric layer on the chip pad; and

second and third upper dielectric layers stacked on the first upper dielectric layer,

wherein the second upper dielectric layer comprises an insulating material different from those of the first and third upper dielectric layers.

8. The semiconductor device of claim 1, further comprising a passivation layer on the upper dielectric layer of the chip region,

wherein the passivation layer exposes a portion of the redistribution pad and a top surface of the upper dielectric layer on the edge region.

9. The semiconductor device of claim 8, further comprising a redistribution spacer that is on a sidewall of the second opening and comprises a same material as that of the redistribution pad,

wherein the passivation layer extends from the chip region to the edge region.

10. A semiconductor device, comprising:

a semiconductor substrate comprising a chip region and an edge region;

a lower dielectric layer on the semiconductor substrate;

a chip pad on the lower dielectric layer of the chip region;

an upper dielectric layer on the lower dielectric layer and on the chip pad; and

a redistribution pad penetrating the upper dielectric layer and connected to the chip pad, the redistribution pad comprising a via portion in the upper dielectric layer and coupled to the chip pad and comprising a pad portion extending from the via portion onto the upper dielectric layer,

wherein the upper dielectric layer comprises a recessed portion on the edge region;

wherein the lower dielectric layer has a first thickness on the chip region, and

wherein a portion of the lower dielectric layer has a second thickness below the recessed portion relative to the semiconductor substrate, the second thickness being less than the first thickness.

11. The semiconductor device of claim 10, wherein the lower dielectric layer comprises a dielectric material whose dielectric constant is less than that of the upper dielectric layer.

12. The semiconductor device of claim 10, further comprising:

a semiconductor integrated circuit on the chip region of the semiconductor substrate;

a test structure on the edge region of the semiconductor substrate; and

a metal line connected to the semiconductor integrated circuit,

wherein the lower dielectric layer is on the semiconductor integrated circuit, the metal line, and the test structure, and

wherein the recessed portion of the upper dielectric layer overlaps the test structure in a cross sectional view of the semiconductor device.

13. The semiconductor device of claim 12, further comprising a test pad on the lower dielectric layer and connected to the test structure,

wherein the redistribution pad further comprises a redistribution test via that penetrates the upper dielectric layer and is connected to the test pad, and

wherein the pad portion extends from the chip region to the edge region and is connected to the redistribution test via.

14. The semiconductor device of claim 10, wherein the recessed portion has a bottom surface between a top surface of the upper dielectric layer on the chip region and a top surface of the lower dielectric layer on the chip region.

15. The semiconductor device of claim 10, wherein the upper dielectric layer comprises:

a first upper dielectric layer on the chip pad; and

second and third upper dielectric layers stacked on the first upper dielectric layer,

wherein the second upper dielectric layer comprises an insulating material different from those of the first and third upper dielectric layers, and

wherein the recessed portion of the upper dielectric layer exposes the second upper dielectric layer.

16. The semiconductor device of claim 10, further comprising a redistribution spacer that is disposed on a sidewall of the recessed portion and comprises a same material as that of the redistribution pad.

17. The semiconductor device of claim 10, further comprising a passivation layer on the upper dielectric layer,

wherein the passivation layer exposes a portion of the redistribution pad and

the upper dielectric layer on the edge region.

18. The semiconductor device of claim 10, further comprising a passivation layer that is disposed on the upper dielectric layer and exposes a portion of the redistribution pad,

wherein the passivation layer extends from the chip region to the edge region and is on a sidewall of the recessed portion.