ETCHANT TREATMENT PROCESSES FOR SUBSTRATE SURFACES AND CHAMBER SURFACES

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] Embodiments of the invention generally relate to the field of electronic manufacturing processes and devices, more particular, to methods of etching and depositing silicon-containing materials while forming electronic devices.

Description of the Related Art

[0002] Electronic devices such as semiconductor devices are fabricated by an assortment of steps including the deposition and removal of silicon-containing materials. The deposition and removal steps as well as other process steps may cause the substrate surface containing a silicon-containing material to become rough and/or bare contaminants. Also, particulates and other contaminants accumulate on the interior surfaces within a process chamber during the deposition and removal steps. The particulates may eventually further contaminate the substrate surface. Rough or contaminated substrate surfaces generally lead to poor quality interfaces which provide poor device performance and reliability.

[0003] Etching processes have been developed to combat contaminants and roughness on substrate surfaces. However, the traditional etching processes have some draw backs. Usually, etchants, such as hydrogen chloride (HCl), require a high activation temperature in order to remove silicon-containing materials. Therefore, etching processes are often conducted at temperatures of 1,000°C or higher. Such high temperatures are not desirable during a fabrication process due to thermal budget considerations, possible uncontrolled nitridation reactions or over-etching to the substrate surface and loss of economically efficiencies. Etching processes with such extreme conditions may damage interior surfaces within the chamber, such as thermal quartz liners. Chlorine (Cl_2) has been used to remove silicon-containing materials during etch processes at lower temperatures than processes that utilize hydrogen chloride etchants. However, chlorine reacts very

quickly with silicon-containing materials and thus the etch rate is not easily controllable. Therefore, silicon-containing materials are usually over etched by processes using chlorine gas.

[0004] Also, traditional etching processes generally are conducted in an etching chamber or a thermal processing chamber. Once the etching of the silicon-containing material is complete, the substrate is transferred into a secondary chamber for a subsequent deposition process. Often, the substrate is exposed to the ambient environment between the etching process and the deposition process. The ambient environment may introduce water and/or oxygen to the substrate surface forming an oxide layer.

[0005] Prior to the etching process or the deposition process, a substrate is usually exposed to a pre-treatment process including a wet clean process (*e.g.*, a HF-last process), a plasma clean or an acid wash process. After a pre-treatment process and prior to starting an etching process, the substrate may have to reside outside the process chamber or controlled environment for a period of time called the queue time (Q-time). During the Q-time, the substrate is exposed to ambient environmental conditions that include oxygen and water at atmospheric pressure and room temperature. The ambient exposure forms an oxide layer on the substrate surface, such as silicon oxide. Generally, longer Q-times form thicker oxide layers and therefore more extreme etching processes must be conducted at higher temperatures and pressures to maintain throughput.

[0006] Therefore, there is a need to have an etching process for treating a silicon-containing material on a substrate surface to remove any surface contaminants contained thereon and/or to smooth the substrate surface. There is also a need to be able to treat the substrate surface within a process chamber which could subsequently be used during the next process step, such as to deposit an epitaxy layer. Furthermore, there is a need to maintain the process temperature at a low temperature, such as below 1,000°C, and preferably below 800°C, even for substrates that have endured long Q-times (*e.g.*, about 10 hours). Also, there is a

need to reduce particulate accumulation on the interior surfaces of a process chamber, while not damaging these interior surfaces.

SUMMARY OF THE INVENTION

[0007] In one embodiment, a method for finishing or treating a silicon-containing surface is provided which includes smoothing the surface and removing contaminants contained on the surface. In one example, a substrate is placed into a process chamber and heated to a temperature within a range from about 500°C to about 700°C. The substrate is exposed to an etching gas containing an etchant, a silicon source and a carrier gas. Chlorine gas (Cl_2) may be used as the etchant so that a relatively low temperature is used during the etching process. A silicon source is usually provided simultaneously with the etchant in order to counter act any over-etching caused by the etchant. That is, the silicon source is used to deposit silicon on a substrate surface while the etchant removes the silicon. The rates at which the etchant and the silicon source are exposed to the substrate are adjusted so that the overall reaction favors material removal and/or redistribution. Therefore, in one example, the etch rate may be finely controlled (*e.g.*, several angstroms or less per minute) while removing a silicon-containing material during an overall reaction. In another example, silicon-containing material is removed from higher portions of the surface (*i.e.*, peaks) while added to the lower portions of the surface (*i.e.*, troughs) during a redistribution process. A silicon-containing surface with a surface roughness of about 6 nm root mean square (RMS) or more may be transformed into a much smoother surface with a surface roughness of less than about 0.1 nm RMS.

[0008] In another embodiment, a method for etching a silicon-containing surface is provided which includes removing silicon-containing material at a fast rate in order to form a recess in a source/drain (S/D) area on a substrate. In another example, a substrate is placed into a process chamber and heated to a temperature within a range from about 500°C to about 800°C. While the substrate is heated, the silicon-containing surface is exposed to an etching gas containing an etchant and a carrier gas. Chlorine gas may be selected as an etchant used during a fast etch rate

process that usually contains no silicon sources or a low concentration of a silicon source. The silicon source may be added to the etching gas to have additional control of the removal rate.

[0009] In another embodiment, a process chamber is cleaned during a chamber clean process by exposing the interior surfaces of the process chamber to an etching gas to remove particulates and other contaminants. The interior surfaces usually contain a silicon-containing material (*e.g.*, quartz) that may be damaged during an etchant clean process. Therefore, besides an etchant and a carrier gas, the etching gas may further contain a silicon source to counter act any over-etching caused by the etchant. In one example, a chamber clean gas contains chlorine gas and silane. A carrier gas, such as nitrogen, may be combined with the etchant, the silicon source, or both. Generally, the process chamber is heated to a higher temperature during a chamber clean process than during either a slow etch process or a fast etch process. In one example, the process chamber may be heated to a temperature within a range from about 700°C to about 1,000°C during a chamber clean process.

[0010] In another embodiment, a method for forming a silicon-containing material on a substrate surface is provided which includes positioning a substrate containing a silicon material within a process chamber, and exposing the substrate to an etching gas containing chlorine gas and silane during an etching process. The method may further provide exposing the substrate to a deposition gas containing the chlorine gas and the silane during an epitaxial deposition process, removing the substrate from the process chamber, and exposing the process chamber to a chamber clean gas containing the chlorine gas and the silane during a chamber clean process. In one example, the silicon material is removed during the etching process at a rate of about 100 Å/min or less, preferably, at the rate of about 10 Å/min or less, and more preferably, at the rate of about 2 Å/min or less. In another example, the silicon material is removed during the etching process at a rate greater than 100 Å/min, preferably, at a rate within a range from about 200 Å/min to about 1,000 Å/min.

[0011] In another embodiment, a method for etching a silicon-containing monocrystalline material on a substrate having at least a second material (*e.g.*, a nitride material, an oxide material, or combinations thereof) is provided which includes positioning a substrate within a process chamber, exposing the substrate to an etching gas containing chlorine gas and a carrier gas, removing a predetermined thickness of the silicon-containing monocrystalline material to form an exposed monocrystalline surface, and depositing an epitaxy layer on the exposed monocrystalline surface within the process chamber. The etching gas may include a silicon source, such as silane, disilane, dichlorosilane, tetrachlorosilane, hexachlorodisilane, a derivative thereof, or a combination thereof and the carrier gas may include nitrogen, argon, helium, or a combination thereof. In one example, the process chamber is heated at a temperature within a range from about 500°C to about 700°C and pressurized at a pressure within a range from about 10 Torr to about 750 Torr. The monocrystalline material may be removed at a rate within a range from about 200 Å per minute to about 1,000 Å per minute to form a recess formation within a source/drain area on the substrate. The source/drain area may be used within a CMOS, Bipolar, BiCMOS, or a similar device. The epitaxial layer usually contains silicon, silicon-germanium, silicon-carbon, silicon-germanium-carbon, a derivative thereof, or a combination thereof.

[0012] In another embodiment, a method for forming a silicon-containing monocrystalline material on a substrate is provided which includes exposing a substrate to a HF-last wet clean process, positioning the substrate within a process chamber, exposing the substrate to an etching gas comprising chlorine gas and a carrier gas, and removing a predetermined thickness of the silicon-containing monocrystalline material to form an exposed monocrystalline surface. The method may further provide depositing an epitaxy layer on the exposed monocrystalline surface in the process chamber, and cleaning the process chamber with the chlorine gas to remove silicon-containing contaminant adhered thereon. The epitaxy layer may be deposited by a deposition gas containing chlorine gas and the carrier gas may be nitrogen. In one example, nitrogen and chlorine-gas are co-flowed during the process chamber clean step.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] So that the manner in which the above recited features of the invention can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0014] Figure 1 is a flow chart depicting a process for treating a silicon-containing material by one embodiment described herein;

[0015] Figures 2A-2C show schematic illustrations of a substrate at different stages during a process described herein;

[0016] Figure 3 is a flow chart depicting a process for treating a silicon-containing material by another embodiment described herein;

[0017] Figures 4A-4C show schematic illustrations of another substrate at different stages during a process described herein; and

[0018] Figure 5 is a flow chart depicting a process for fabricating substrates and thereafter cleaning the process chamber by another embodiment described herein.

DETAILED DESCRIPTION

[0019] Embodiments of the invention provide processes for etching and depositing silicon-containing materials on substrate surfaces. In one embodiment, a slow etch process (*e.g.*, <100 Å/min) and fast etch process (*e.g.*, >100 Å/min) utilizes an etchant and a silicon source within the etching gas. In another embodiment, the process chamber is exposed to an etching gas during a chamber clean step for removing deposits or contaminants from the interior surfaces. In another embodiment, a process chamber is cleaned during a chamber clean

process by exposing the interior surfaces of the process chamber to an etching gas to remove particulates and other contaminants.

Slow Etch Process (pre-clean and smooth)

[0020] A slow etch process (*e.g.*, <100 Å/min) may be conducted to remove contaminants and surface irregularities, such as roughness, from a substrate surface. In one aspect, the substrate surface may be etched to expose an underlayer free or substantially free of contaminants. In another aspect, material of the substrate surface may be redistributed to minimize or remove peaks and troughs that attribute to surface irregularities. During the slow etch process, the substrate is exposed to an etching gas containing an etchant, a silicon source, and an optional carrier gas. The overall reaction may be controlled in part by manipulating the relative flow rates of the etchant and the silicon source, using a specific etchant source and a silicon source and by adjusting the temperature and the pressure.

[0021] The substrate may be exposed to a pre-treatment process to prepare the substrate surface for the subsequent etching process. A pre-treatment process may include a wet clean process, such as a HF-last process, a plasma clean, an acid wash process, or combinations thereof. In one example, the substrate is treated with a HF-last wet clean process by exposing the surface to a hydrofluoric acid solution (*e.g.*, about 0.5 wt% HF in water) for a duration of about 2 minutes.

[0022] Figure 1 illustrates a flow chart depicting process 100 for removing contaminants 212 and rough areas 218 from substrate 200 that is graphically illustrated by Figure 2A. Substrate 200 contains silicon-containing layer 205 and surface 210. Contaminants 212 and rough areas 218 are contained on and in surface 210. Rough areas 218 may be formed by peaks 216 and troughs 214 within surface 210. A predetermined thickness 220 of material from silicon-containing layer 205 may be removed during the slow etch process to reveal exposed surface 230 (Figure 2B). Subsequently, layer 240 may be formed on exposed surface 230 during an optional deposition process (Figure 2C). In one example, layer 240 contains a silicon-containing material deposited by an epitaxy deposition process.

[0023] Embodiments of the invention provide processes to etch and deposit silicon-containing materials on various substrates surfaces and substrates, such as substrates 200 and 400 and layers 205 and 405 (Figures 2A-2C and 4A-4C) A "substrate" or "substrate surface" as used herein refers to any substrate or material surface formed on a substrate upon which film processing is performed. For example, a substrate surface on which processing may be performed include materials such as silicon, silicon-containing materials, silicon oxide, strained silicon, silicon on insulator (SOI), fluorine-doped silicate glass (FSG), carbon doped silicon oxides, silicon nitride, doped silicon, silicon germanium, silicon germanium carbon, germanium, silicon carbon, gallium arsenide, glass, sapphire, or other materials depending on the application. A substrate surface may also include dielectric materials such as silicon dioxide, silicon nitride, silicon oxynitride, and/or carbon doped silicon oxides. Substrates may have various dimensions, such as 200 mm or 300 mm diameter round wafers, as well as, rectangular or square panes. Embodiments of the processes described herein etch and deposit on many substrates and surfaces, especially, silicon and silicon-containing materials. Substrates on which embodiments of the invention may be useful include, but are not limited to semiconductor wafers, such as crystalline silicon (*e.g.,* Si<100> or Si<111>), silicon oxide, strained silicon, silicon germanium, doped or undoped polysilicon, doped or undoped silicon wafers silicon nitride, and patterned or non-patterned wafers.

[0024] Throughout the application, the terms "silicon-containing" materials, compounds, films or layers should be construed to include a composition containing at least silicon and may contain germanium, carbon, boron, arsenic, phosphorous gallium and/or aluminum. Other elements, such as metals, halogens or hydrogen may be incorporated within a silicon-containing material, compound, film or layer, usually with concentrations of about part per million (ppm). Compounds or alloys of silicon-containing materials may be represented by an abbreviation, such as Si for silicon, SiGe, for silicon germanium, SiC for silicon carbon and SiGeC for silicon germanium carbon. The abbreviations do not represent chemical equations with stoichiometrical relationships, nor represent any particular reduction/oxidation state

of the silicon-containing materials. Silicon-containing materials, compounds, films, or layers may include substrates or substrate surfaces.

[0025] Contaminants 212 on surface 210 include organic residues, carbon, oxides, nitrides, halides (*e.g.,* fluorides or chlorides), or combinations thereof. For example, surface 210 may contain a layer of silicon oxide after being exposed to the ambient air or may contain a layer of silicon fluoride after being treated with a HF-last wet clean process. Surface 210 may also contain irregularities or regional areas of roughness, such as troughs 214 and peaks 216 within rough areas 218.

[0026] Substrate 200 may be positioned within a process chamber and heated to a predetermined temperature (step 110). The substrate and the process chamber may be heated completely or a portion thereof to temperature within a range from about 300°C to about 800°C, preferably, from about 500°C to about 700°C, and more preferably, from about 550°C to about 650°C. The process chamber may be maintained at a pressure within a range from about 1 mTorr to about 760 Torr, preferably, from about 0.1 Torr to about 500 Torr, and more preferably, from about 1 Torr to about 100 Torr.

[0027] In one embodiment, a cold wall reactor is used as a process chamber for processes conducted at lower temperatures. A cold wall reactor may provide temperature control of each independent portion within the reactor, such as reactor walls, reactor dome and substrate susceptor. Usually, the reactor dome may be formed from quartz. In one example, the cold wall reactor may have reactor walls maintained at a temperature less than about 400°C, preferably, less than about 200°C, and more preferably, less than about 150°C, a reactor dome maintained at a temperature within a range from about 300°C to about 800°C, preferably, from about 400°C to about 700°C, and more preferably, from about 500°C to about 600°C, and a substrate susceptor maintained at a temperature within a range from about 300°C to about 800°C, preferably, from about 500°C to about 700°C, and more preferably, from about 550°C to about 650°C.

[0028] The etching gas used during the slow etch process (step 120) contains an etchant, a silicon source and an optional carrier gas. The etchant, the silicon source and the carrier gas may be premixed, co-flowed or independently flowed into the process chamber. In one aspect, the etchant and a carrier gas are either co-flowed or combined together as a gas mixture, the silicon source and a carrier gas are either co-flowed or combined together as a gas mixture and the two gas mixtures may be co-flowed together prior to entering the process chamber. For example, a gas mixture of chlorine and nitrogen may be co-flowed into the process chamber with a mixture of silane and nitrogen. In another example, a gas mixture of chlorine and nitrogen may be co-flowed into the process chamber with a mixture of silane and hydrogen.

[0029] Preferably, the etchant is chlorine gas (Cl_2). In one example, it has been found that chlorine works exceptionally well as an etchant for silicon-containing materials at temperatures lower than processes using more common etchants, such as hydrogen chloride. Therefore, an etch process utilizing chlorine may be conducted at a lower process temperature. The silicon source may be administered simultaneously with the etchant in order to counter act any over-etching of susceptible surfaces on substrate 200. The silicon source is used to deposit silicon on the silicon-containing layer while the etchant removes the silicon-containing material. The rates at which the etchant and the silicon source are exposed to the substrate are adjusted so that the overall reaction favors material removal and/or material redistribution. Therefore, the overall reaction is removing or redistributing silicon-containing material and the etch rate may be finely controlled to several angstroms per minute.

[0030] The etchant is usually administered into the process chamber at a rate within a range from about 1 standard cubic centimeters per minute (sccm) to about 1 standard liters per minute (slm), preferably, from about 5 sccm to about 150 sccm, and more preferably, from about 10 sccm to about 30 sccm, for example, about 20 sccm. While chlorine is the preferred etchant, other etchants that may be used solely or in combination include chlorine trifluoride (ClF_3), tetrachlorosilane ($SiCl_4$), or a derivative thereof.

[0031] The silicon source is usually provided into the process chamber for slow etch processes at a rate within a range from about 5 sccm to about 500 sccm, preferably, from about 10 sccm to about 100 sccm, and more preferably, from about 20 sccm to about 80 sccm, for example, about 50 sccm. Silicon sources that may be used in the etching include silanes, halogenated silanes, organosilanes, or derivatives thereof. Silanes include silane (SiH_4) and higher silanes with the empirical formula $Si_xH_{(2x+2)}$, such as disilane (Si_2H_6), trisilane (Si_3H_8), and tetrasilane (Si_4H_{10}), as well as others. Halogenated silanes include compounds with the empirical formula $X'_ySi_xH_{(2x+2-y)}$, where X' is independently selected from F, Cl, Br, or I, such as hexachlorodisilane (Si_2Cl_6), tetrachlorosilane ($SiCl_4$), trichlorosilane (Cl_3SiH), dichlorosilane (Cl_2SiH_2) and chlorosilane ($ClSiH_3$). Organosilanes include compounds with the empirical formula $R_ySi_xH_{(2x+2-y)}$, where R is independently selected from methyl, ethyl, propyl or butyl, such as methylsilane ($(CH_3)SiH_3$), dimethylsilane ($(CH_3)_2SiH_2$), ethylsilane ($(CH_3CH_2)SiH_3$), methyldisilane ($(CH_3)Si_2H_5$), dimethyldisilane ($(CH_3)_2Si_2H_4$), and hexamethyldisilane ($(CH_3)_6Si_2$). The preferred silicon sources may include silane, dichlorosilane, or disilane.

[0032] The carrier gas is usually provided into the process chamber at a flow rate within a range from about 1 slm to about 100 slm, preferably, from about 5 slm to about 80 slm, and more preferably, from about 10 slm to about 40 slm, for example, about 20 slm. Carrier gases may include nitrogen (N_2), hydrogen (H_2), argon, helium, or combinations thereof. In one embodiment, an inert carrier gas is preferred and includes nitrogen, argon, helium, or combinations thereof. A carrier gas may be selected based on the precursor(s) used and/or the process temperature of the slow etch process of step 120.

[0033] Preferably, nitrogen is utilized as a carrier gas in embodiments featuring low temperature (*e.g.*, <800°C) processes. Low temperature processes are accessible due in part to the use of chlorine gas in the etching process. Nitrogen remains inert during low temperature etching processes. Therefore, nitrogen is not incorporated into the silicon-containing materials on the substrate during low temperature processes. Also, a nitrogen carrier gas does not form hydrogen-terminated surfaces as does a hydrogen carrier gas. The hydrogen-terminated

surfaces formed by the adsorption of hydrogen carrier gas on the substrate surface inhibit the growth rate of subsequently deposited silicon-containing layers. Finally, the low temperature processes may take economic advantage of nitrogen as a carrier gas, since nitrogen is far less expensive than hydrogen, argon, or helium. In one example of an etching gas, chlorine is the etchant, silane is the silicon source and nitrogen is the carrier gas.

[0034] Substrate 200 and surface 210 may be exposed to a slow etch gas to remove a predetermined thickness 220 of silicon-contalning layer 205 during step 120 (Figures 2A-2B). Surface 210 is etched during the removal of the predetermined thickness 220. The slow etch gas is exposed to substrate 200 for a time period within a range from about 5 seconds to about 5 minutes, preferably, from about 30 seconds to about 2 minutes. The amount of time is adjusted relative to the etch rate used in a particular process. The etch rate of a slow etch process is usually less than about 100 Å/min, preferably, less than about 50 Å/min. In one embodiment, the slow etch rate is within a range from about 2 Å/min to about 20 Å/min, preferably, from about 5 Å/min to about 15 Å/min, for example, about 10 Å/min. In another embodiment, the etch rate is about 2 Å/min or less, preferably, about 1 Å/min or less, and more preferably, approaches a redistribution of material on the substrate such that the net removal rate is non-measurable relative to the thickness of the layer. As the etch process is slowed to a redistribution reaction, material of silicon-containing layer 205 may be removed from peaks 216 and added to troughs 214 within surface 210 to form exposed surface 230. Troughs 214 may be filled by the material derived from peaks 216 and/or virgin material being produced by the introduction of precursors (*e.g.*, silicon source) within the slow etch gas.

[0035] A slow etch process may be utilized to reduce the surface roughness on substrate 200. In one example, surface 210 with a surface roughness of about 6 nm root mean square (RMS) or more, may be exposed to a slow etch gas to remove material from silicon-containing layer 205 by predetermined thickness 220 to reveal exposed surface 230. Exposed surface 230 may have a surface roughness of about 1 nm RMS or less, preferably, about 0.1 nm RMS or less, and more preferably,

about 0.07 nm RMS. Contaminants 212 and rough areas 218 previously disposed on or in surface 210 are removed during process 100. Exposed surface 230 is usually free or substantially free of contaminants that include organic residues, carbon, oxides, nitrides, halides (*e.g.*, fluorides or chlorides), or combinations thereof.

[0036] An optional purge process may be performed within the process chamber during step 125 (Figure 1). The purge process helps remove residual etch gas from substrate 200, which in turn enhances the growth during the subsequent deposition process (step 130). During a low pressure purge process, the process chamber may have an internal pressure within a range from about 0.1 mTorr to about 100 Torr, preferably, from about 1.0 mTorr to about 10 Torr, and more preferably, from about 10.0 mTorr to about 1 Torr. The purge process may be conducted for a time period within a range from about 30 seconds to about 10 minutes, preferably, from about 1 minute to about 5 minutes, and more preferably, from about 2 minutes to about 4 minutes. Generally, all of the gas entering the process chamber may be turned off. However, in an alternative aspect, a purge gas may be administered anytime during the purge process. A purge gas may include nitrogen, hydrogen, argon, helium, forming gas, or combination thereof.

[0037] Layer 240 may be deposited on exposed surface 230 during step 130. Preferably, layer 240 is a silicon-containing material that may be selectively and epitaxially grown or deposited on exposed surface 230 by a chemical vapor deposition (CVD) process. Chemical vapor deposition processes, as described herein, include many techniques, such as atomic layer epitaxy (ALE), atomic layer deposition (ALD), plasma-assisted CVD (PA-CVD) or plasma-enhanced CVD (PE-CVD), plasma-assisted ALD (PA-ALD) or plasma-enhanced ALD (PE-ALD), atomic layer CVD (ALCVD), organometallic or metal-organic CVD (MOCVD or OMCVD), laser-assisted CVD (LA-CVD), ultraviolet CVD (UV-CVD), hot-wire (HWCVD), reduced-pressure CVD (RP-CVD), ultra-high vacuum CVD (UHV-CVD), derivatives thereof, or combinations thereof. In one example, a preferred process utilizes thermal CVD to epitaxially grow or deposit a silicon-containing compound as layer 240 on exposed surface 230. The deposition gas used during step 130 may also

contain at least one secondary elemental source, such as a germanium source and/or a carbon source. The germanium source may be added to the process chamber with the silicon source, etchant and carrier gas to form a silicon-containing compound. Therefore, the silicon-containing compound may contain silicon, SiGe, SiC, SiGeC, doped variants thereof, or combinations thereof. Germanium and/or carbon may be added to the silicon-containing material by including germanium source (*e.g.*, germane), or a carbon source (*e.g.*, methylsilane) during the deposition process. The silicon-containing compound may also contain dopants by including a boron source (*e.g.*, diborane), an arsenic source (*e.g.*, arsine), or a phosphorous source (*e.g.*, phosphine) during or after the deposition process. The dopant may be included within the silicon source, etchant and carrier gas to form a silicon-containing compound. Alternatively, the dopant may be added to the silicon-containing material by exposing the substrate to an ion implantation process.

[0038] In another example, a CVD process called alternating gas supply (AGS) may be used to epitaxially grow or deposit a silicon-containing compound as layer 240 on exposed surface 230. The AGS deposition process includes a cycle of alternating exposures of silicon-sources and etchants to the substrate surface. An AGS deposition process is further disclosed in commonly assigned and co-pending United States Serial No. 11/001,774, filed December 1, 2004, entitled "Selective Epitaxy Process with Alternating Gas Supply," which is incorporated herein by reference in its entirety for the purpose of describing an AGS process.

[0039] Process 100 may be used to etch and deposit silicon-containing materials within the same process chamber. Preferably, the slow etch process (step 120) and the subsequent deposition process (step 130) are performed within the same process chamber to improve throughput, be more efficient, decrease probability of contamination and benefit process synergies, such as common chemical precursors. In one aspect, a slow etch process and a deposition process each utilize the same silicon source, the same etchant and the same carrier gas. For example, an etch gas for a slow etch process may contain silane, chlorine, and nitrogen, while a deposition gas for a selective, epitaxial deposition process may also contain silane, chlorine, and nitrogen. The concentration ratio of the silicon source and the

reductant may be adjusted during the overall process to encourage a particular step. In one example, the concentration ratio of the silicon source and the reductant is increased to promote a deposition step. In another example, the concentration ratio of the silicon source and the reductant is decreased to promote an etch step.

Fast Etch Process

[0040] In another embodiment, a fast etch process (*e.g.*, >100 Å/min) may be used to selectively remove a silicon-containing material from a substrate surface. The fast etch process is a selective etch process to remove silicon-containing material while leaving barrier material unscathed. Barrier materials may include silicon nitride, silicon oxide, or silicon oxynitride used as spacers, capping layers, or mask materials.

[0041] Figure 3 illustrates a flow chart depicting process 300 is initiated by positioning the substrate into a process chamber and adjusting the process parameters during step 310. The substrate and the process chamber may be heated completely or a portion thereof to a temperature within a range from about 400°C to about 800°C, preferably, from about 500°C to about 700°C, and more preferably, from about 550°C to about 650°C. The process chamber is maintained at a pressure within a range from about 1 Torr to about 760 Torr, preferably, from about 0.1 Torr to about 500 Torr, and more preferably, from about 1 Torr to about 100 Torr.

[0042] The etching gas used during the fast etch process contains an etchant, a carrier gas and an optional silicon source (step 320). In one example, the etching gas contains chlorine, nitrogen, and silane. The etchant may be provided into the process chamber gas at a rate within a range from about 1 sccm to about 100 sccm, preferably from about 5 sccm to about 50 sccm, and more preferably, from about 10 sccm to about 30 sccm, for example, about 20 sccm. While chlorine is the preferred etchant during a fast etch process, other etchants that may be used solely or in combination include chlorine trifluoride, tetrachlorosilane, or a derivative thereof.

[0043] The carrier gas is usually provided into the process chamber at a flow rate within a range from about 1 slm to about 100 slm, preferably, from about 5 slm to about 80 slm, and more preferably, from about 10 slm to about 40 slm, for example, about 20 slm. Carrier gases may include nitrogen, hydrogen, argon, helium, or combinations thereof. In one embodiment, an inert carrier gas is preferred and includes nitrogen, argon, helium, or combinations thereof. A carrier gas may be selected based on the precursor(s) used and/or the process temperature during the etching process of step 320. Preferably, nitrogen is used as a carrier gas during embodiments featuring low temperature (*e.g.*, <800°C) processes. In one example, an etching gas for a first etch process contains chlorine and nitrogen.

[0044] In some embodiments, a silicon source may be optionally added to the etching gas for providing additional control of the etch rate during a fast etch process. The silicon source may be delivered into the process chamber at a rate within a range from about 5 sccm to about 500 sccm, preferably, from about 10 sccm to about 100 sccm, and more preferably, from about 20 sccm to about 80 sccm, for example, about 50 sccm. The etching gas may contain a silicon source, such as silanes, halogenated silanes, organosilanes, or derivatives thereof, as described herein.

[0045] Substrate 400 contains at least one film stack feature 410 (Fig 4A). Silicon-containing layer 405 may be a doped or undoped, bare silicon substrate or include a silicon-containing layer disposed thereon. Film stack feature 410 includes gate layer 412 on gate oxide layer 414 surrounded by spacers 416 and protective capping layer 418. Generally, gate layer 412 is composed of a polysilicon and gate oxide layer 414 is composed of silicon dioxide, silicon oxynitride, or hafnium oxide. Partially encompassing the gate oxide layer 414 is a spacer 416, which is usually an isolation material containing silicon oxide, silicon nitride, silicon oxynitride, derivatives thereof, or combinations thereof. In one example, spacer 416 is a nitride/oxide stack (*e.g.*, $Si_3N_4/SiO_2/Si_3N_4$). Gate layer 412 may optionally have a protective capping layer 418 adhered thereon.

[0046] During step 320, substrate 400 is exposed to an etching gas to remove a predetermined thickness 425 of silicon-containing layer 405 and form a recess 430, as depicted in Figure 4B. The etching gas is exposed to substrate 400 for a time period within a range from about 10 seconds to about 5 minutes, preferably, from about 1 minute to about 3 minutes. The amount of time is adjusted relative to the etch rate used in a particular process. The etch rate of a fast etch process is usually faster than about 100 Å/min, preferably, faster than about 200 Å/min, such as at a rate within a range from about 200 Å/min to about 1,500 Å/min, preferably, from about 200 Å/min to about 1,000 Å/min, for example, about 600 Å/min.

[0047] In one example, the etching process may be kept at a fast rate to remove the predetermined thickness 425, and then reduced to a slow rate process to smooth the remaining surface. The reduced etching rate may be controlled by a slow etching process described by process 100.

[0048] An optional purge process may be performed within the process chamber during step 325. The purge process helps remove residual etch gas from substrate 400, which in turn enhances the growth during the subsequent deposition process (step 330). During a low pressure purge process, the process chamber may have an internal pressure within a range from about 0.1 mTorr to about 100 Torr, preferably, from about 1.0 mTorr to about 10 Torr, and more preferably, from about 10.0 mTorr to about 1 Torr. The purge process may be conducted for a time period within a range from about 30 seconds to about 10 minutes, preferably, from about 1 minute to about 5 minutes, and more preferably, from about 2 minutes to about 4 minutes. Generally, all of the gas entering the process chamber may be turned off. However, in an alternative aspect, a purge gas may be administered into the process chamber anytime during the purge process.

[0049] Once the predetermined thickness 425 of substrate 400 is removed, layer 440 may be deposited during step 330 (Figure 4C). Preferably, layer 440 is a silicon-containing material that may be selectively and epitaxially deposited on the exposed surface of recess 430 a CVD process. In one example, the CVD process includes an AGS deposition technique. Alternatively, recess 430 may be exposed to

another fabrication process prior to the deposition of layer 440, such as a doping process. One example of a doping process includes ion implantation, in which a dopant (*e.g.,* boron, phosphorous, or arsenic) may be implanted into the surface of the recess 430.

[0050] Process 300 may be used to etch and deposit silicon-containing materials in the same process chamber. Preferably, the fast etch process and the subsequent deposition is performed in the same process chamber to improve throughput, be more efficient, decrease probability of contamination and benefit process synergies, such as common chemical precursors. In one example, both the fast etch process and the selective, epitaxial deposition process of a silicon-containing compound use chlorine as an etchant and nitrogen as a carrier gas.

[0051] Figure 5 illustrates an alternative embodiment of the invention that includes cleaning the process chamber after finishing fabrication techniques during process 500. The substrate may be exposed to a pre-treatment process that includes a wet clean process, a HF-last process, a plasma clean, an acid wash process, or combinations thereof (step 510). After a pre-treatment process and prior to starting an etching process described herein, the substrate may have to remain outside the controlled environment of the process chamber for a period of time called queue time (Q-time). The Q-time in an ambient environment may last about 2 hours or more, usually, the Q-time last much longer, such as a predetermined time with a range from about 6 hours to about 24 hours or longer, such as about 36 hours. A silicon oxide layer usually forms on the substrate surface during the Q-time due to the substrate being exposed to ambient water and oxygen.

[0052] During step 520, the substrate is positioned into a process chamber and exposed to an etching process as described herein. The etching process may be a slow etch process as described in step 120, a fast etch process as described in step 320 or both. The etching process removes a pre-determined thickness of silicon-containing layer from the substrate to form an exposed silicon-containing layer. Subsequently, an optional purge process may be performed within the process chamber (step 525). Thereafter, a secondary material is deposited on the exposed

silicon-containing layer (step 530). Usually, the secondary material is in a selective, epitaxially deposited silicon-containing compound. The deposition process may include the processes as described during steps 130 and 330. In one embodiment, processes 100 and 300 may be used during steps 520 and 530.

[0053] A chamber clean process is conducted inside the process chamber to remove various contaminants therein (step 540). Etch processes and deposition processes may form deposits or contaminants on surfaces within the process chamber. Usually, the deposits include silicon-containing materials adhered to the walls and other inner surfaces of the process chamber. Therefore, a chamber clean process may be used to remove contaminants while not damaging interior surfaces of the process chamber.

[0054] In an example of process 500, the substrate is first exposed to a HF-last process. The substrate is placed into a process chamber and exposed to an etch process that contains chlorine and nitrogen at about 600°C. Thereafter, the process chamber is exposed to a purge process. Subsequently, a silicon-containing layer is epitaxially deposited on the substrate by a deposition process utilizing chlorine and nitrogen at about 625°C within the same process chamber. Thereafter, the substrate is removed and the process chamber is heated to about 675°C and exposed to a cleaning gas containing chlorine and nitrogen. Preferably, the etchant and the carrier gas are the same gases used during steps 520 and 540.

Chamber Clean Process

[0055] In another embodiment, a chamber clean gas containing a silicon source may be used to remove various contaminants from inside a process chamber during a chamber clean process, such as step 540. The interior surfaces of the process chamber usually contain a silicon-containing material (*e.g.*, quartz) that may be damaged during a traditional etchant clean process. Therefore, besides an etchant and a carrier gas, the chamber clean gas may further contain a silicon source to counter act any over-etching caused by the etchant.

[0056] The process chamber may contain an interior surface or components having a surface that is chemically vulnerable to an etchant. Also, the interior surface or componential part within the process chamber may have a protective coating that is vulnerable to an etchant. Generally, these interior surface within the process chamber may contain a silicon-containing surface, such as quartz, silicon oxide, silicon carbide, silicon carbide coated graphite, sapphire, silicide coatings, derivatives thereof, or combinations thereof. In other examples, the interior surface is a metal-containing surface within the process chamber, such as steel, stainless steel, iron, nickel, chromium, aluminum, alloys thereof, or combinations thereof. The interior surfaces may be on the interior of the walls, floor, and lid of the chamber, as well as internal components or portions thereof, such as a susceptor, a linear, an upper dome, a lower dome, a preheat ring, a showerhead, a dispersion plate, a probe, or the like.

[0057] The cleaning process includes heating the substrate susceptor to a temperature within a range from about 600°C to about 1,200°C, preferably, from about 650°C to about 1,000°C, and more preferably, from about 700°C to about 900°C, for example, about 800°C. The process chamber may have an internal pressure within a range from about 1 mTorr to about 760 Torr, preferably, from about 100 mTorr to about 750 Torr, and more preferably, from about 100 Torr to about 700 Torr, for example, 600 Torr. In one example, a cold wall reactor is used as a process chamber and may have reactor walls maintained at a temperature less than about 400°C, preferably, less than about 200°C, and more preferably, less than about 150°C and a quartz reactor dome maintained at a temperature within a range from about 300°C to about 800°C, preferably, from about 400°C to about 700°C, and more preferably, from about 500°C to about 600°C.

[0058] The cleaning process is conducted for a time period within a range from about 30 seconds to about 10 minutes, preferably, from about 1 minute to about 5 minutes, and more preferably, from about 2 minutes to about 4 minutes. A chamber cleaning gas may contain an etchant, a silicon source and a carrier gas. Preferably, the etchant, the silicon source and the carrier gas used during the chamber cleaning process are the same gases used during a previous fabrication step, such as a slow

etch process or a fast etch process. The etchant may be provided into the process chamber during the chamber clean process at a rate within a range from about 10 sccm to about 100 slm, preferably, from about 100 sccm to about 5 slm. In one example, the etchant has a flow rate of about 5 slm, preferably, about 10 slm, and more preferably, about 20 slm. In another example, the etchant has a flow rate of about 50 sccm, preferably, about 130 sccm, and more preferably, about 1,000 sccm. Etchants that may be used within the cleaning gas include chlorine, chlorine trifluoride, tetrachlorosilane, hexachlorodisilane, or derivatives thereof.

[0059] The silicon source may be provided into the process chamber during the chamber clean process at a rate within a range from about 10 sccm to about 100 slm, preferably, from about 100 sccm to about 5 slm. In one example, the silicon source has a flow rate of about 5 slm, preferably, about 10 slm, and more preferably, about 20 slm. In another example, the silicon source has a flow rate of about 50 sccm, preferably, about 130 sccm, and more preferably, about 1,000 sccm. Silicon sources that may be used in the etching include silanes, halogenated silanes, organosilanes or derivatives thereof. Silanes include silane (SiH_4) and higher silanes with the empirical formula $Si_xH_{(2x+2)}$, such as disilane (Si_2H_6), trisilane (Si_3H_8), and tetrasilane (Si_4H_{10}), as well as others. Halogenated silanes include compounds with the empirical formula $X'_ySi_xH_{(2x+2-y)}$, where X' is independently selected from F, Cl, Br or I, such as hexachlorodisilane (Si_2Cl_6), tetrachlorosilane ($SiCl_4$), trichlorosilane (Cl_3SiH), dichlorosilane (Cl_2SiH_2), and chlorosilane ($ClSiH_3$). Organosilanes include compounds with the empirical formula $R_ySi_xH_{(2x+2-y)}$, where R is independently selected from methyl, ethyl, propyl or butyl, such as methylsilane ($(CH_3)SiH_3$), dimethylsilane ($(CH_3)_2SiH_2$), ethylsilane ($(CH_3CH_2)SiH_3$), methyldisilane ($(CH_3)Si_2H_5$), dimethyldisilane ($(CH_3)_2Si_2H_4$), and hexamethyldisilane ($(CH_3)_6Si_2$). Preferred silicon sources may include silane, dichlorosilane, or disilane.

[0060] The carrier gas may be provided into the process chamber during the chamber clean process at a rate within a range from about 100 sccm to about 100 slm. In one example, the carrier gas has a flow rate of about 20 slm, preferably, about 50 slm, and more preferably, about 100 slm. In another example, the carrier gas has a flow rate of about 100 sccm, preferably, about 1 slm, and more preferably,

about 10 slm. Carrier gases may include nitrogen, hydrogen, forming gas, argon, helium or combinations thereof. In a preferred example, a chamber clean gas contains chlorine gas, silane and a carrier gas, such as nitrogen. A chamber clean process that may be used within embodiments of the invention described herein is further disclosed in commonly assigned U.S. Patent No. 6,042,654, which is incorporated herein by reference in its entirety. The chamber clean process may be repeated after processing each individual substrate or after multiple substrates. In one example, the chamber clean process is conducted after processing every 25 substrates. In another example, the chamber clean process is conducted after processing every 5 substrates. In another example, the chamber clean process is conducted after processing every 100 substrates. Although a substrate may remain in the process chamber during the chamber clean process, preferably, the substrate is removed and the process is performed on an empty chamber.

[0061] Embodiments, as described herein, provide processes that may be utilized during fabrication processes for Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and bipolar transistors, such as Bipolar device fabrication (*e.g.,* base, emitter, collector, and emitter contact), BiCMOS device fabrication (*e.g.,* base, emitter, collector, emitter contact), and CMOS device fabrication (*e.g.,* channel, source/drain, source/drain extension, elevated source/drain, substrate, strained silicon, silicon on insulator, and contact plug). Other embodiments provide processes that may be utilized during gate fabrication processes, base contact fabrication processes, collector contact fabrication processes, emitter contact fabrication processes, or elevated source/drain fabrication processes.

[0062] The processes of the invention may be conducted on fabrication equipment used for ALE, CVD, and ALD processes. A system that may be used to etch or deposit the silicon-containing films as described herein include the Epi Centura® system or the Poly Gen® system, both available from Applied Materials, Inc., located in Santa Clara, California. A process chamber useful to etch and deposit as described herein is further disclosed in commonly assigned U.S. Patent No. 6,562,720, which is incorporated herein by reference in its entirety for the

purpose of describing the apparatus. Other enabling apparatuses include batch furnaces and high-temperature furnaces.

EXAMPLES

[0063] The following hypothetical examples may be conducted on 300 mm silicon wafers within an Epi Centura® system, available from Applied Materials, Inc., located in Santa Clara, California.

[0064] Example 1 – Pre-clean process comparative without silane: A substrate was exposed to an HF-last process to form a fluoride terminated surface. The substrate was placed in the process chamber and heated to about 600°C while the pressure was maintained at about 20 Torr. The substrate was exposed to an etching gas containing N_2 at a flow rate of about 20 slm and Cl_2 at flow rate of about 120 sccm. The surface was etched at a rate of about 500 Å/min.

[0065] Example 2 – Pre-clean process with silane: A substrate was exposed to an HF-last process to form a fluoride terminated surface. The substrate was placed in the process chamber and heated to about 600°C while the pressure was maintained at about 20 Torr. The substrate was exposed to an etching gas containing N_2 at a flow rate of about 20 slm, Cl_2 at flow rate of about 20 sccm and SiH_4 at a flow rate of about 50 sccm. The surface was etched at a rate of about 10 Å/min. Therefore, the addition of a silicon source, such as silane in Example 2, reduced the etch rate of the silicon-containing layer by about 50 times as compared to the etch rate in Example 1.

[0066] Example 3 – Smoothing process comparative without silane: A substrate surface containing a silicon-containing layer was cleaved forming a surface with a roughness of about 5.5 nm root mean square (RMS). The substrate was placed in the process chamber and heated to about 650°C while the pressure was maintained at about 200 Torr. The substrate was exposed to an etching gas containing N_2 at a flow rate of about 20 slm and Cl_2 at flow rate of about 20 sccm. The surface was etched at a rate of about 200 Å/min.

[0067] Example 4 – Smoothing process with silane: A substrate surface containing a silicon-containing layer was cleaved forming a surface with a roughness of about 5.5 nm root mean square. The substrate was placed in the process chamber and heated to about 650°C while the pressure was maintained at about 200 Torr. The substrate was exposed to an etching gas containing N_2 at a flow rate of about 20 slm, Cl_2 at flow rate of about 20 sccm and SiH_4 at a flow rate of about 50 sccm. The surface was etched at a rate of about 20 Å/min. The surface roughness was reduced to about 0.1 nm RMS. Therefore, the addition of a silicon source, such as silane used in Example 4, reduced the etch rate of the silicon-containing layer by about 10 times as compared to the etch rate in Example 3.

[0068] Example 5 – Chlorine etch process followed by silicon-epitaxy: A silicon substrate contained a series of silicon nitride line features that are about 90 nm tall, about 100 nm wide and about 150 nm apart, baring the silicon surface. The substrate was placed in the process chamber and heated to about 600°C while the pressure was maintained at about 40 Torr. The substrate was exposed to an etching gas containing N_2 at a flow rate of about 20 slm and Cl_2 at flow rate of about 80 sccm. The surface was etched at a rate of about 750 Å/min. After about 30 seconds, about 35 nm of the silicon surface was etched. The silicon nitride features remain inert to the etching process. The pressure was increased to about 200 Torr and SiH_4 was added to the etching gas at a flow rate of about 50 sccm. The etch rate was reduced to about 18 Å/min to smooth the freshly etched silicon surface. After about 1 minute, the smooth surface is exposed to a selective epitaxy deposition process by increasing the flow of SiH_4 to about 100 sccm and maintaining the flow of N_2 and Cl_2 unchanged. A silicon-containing material was deposited on the silicon surface at a rate of about 25 Å/min.

[0069] Example 6 – Chlorine fast etch process containing silane: A silicon substrate contained a series of silicon nitride line features that are about 90 nm tall, about 100 nm wide and about 150 nm apart, baring the silicon surface. The substrate was placed in the process chamber and heated to about 600°C while the pressure was maintained at about 40 Torr. The substrate was exposed to an etching gas containing N_2 at a flow rate of about 20 slm, Cl_2 at flow rate of about 80

sccm and SiH_4 at flow rate of about 40 sccm. The surface was etched at a rate of about 400 Å/min.

[0070] Example 7 – Chamber clean process containing chlorine and silane: After a silicon epitaxial deposition process, the substrate was removed from the chamber. The process chamber was heated to about 800°C while the pressure was adjusted to about 600 Torr. The process chamber was exposed to an etching gas containing N_2 at a flow rate of about 20 slm, Cl_2 at flow rate of about 2 slm and SiH_4 at flow rate of about 1 slm. The chamber clean process was conducted for about 2 minutes.

[0071] While the foregoing is directed to embodiments of the invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

Claims:

1. A method of etching a silicon-containing material on a substrate surface, comprising:
positioning a substrate comprising the silicon-containing material containing a contaminant into a process chamber;
exposing the silicon-containing material to an etching gas comprising chlorine gas, a silicon source and a carrier gas at a temperature less than 800° C.; and
removing the contaminant and a predetermined thickness of the silicon-containing material.

2. The method of claim 1, wherein the silicon-containing material is removed at a rate in a range from about 2 Å per minute to about 20 Å per minute.

3. The method of claim 2, wherein the process chamber is maintained at a temperature in a range from about 500° C. to about 700° C.

4. The method of claim 3, wherein the carrier gas is selected from the group consisting of nitrogen, argon, helium and combinations thereof.

5. The method of claim 4, wherein the silicon source is selected from the group consisting of silane, disilane, dichlorosilane, tetrachlorosilane, hexachlorodisilane, derivatives thereof and combinations thereof.

6. The method of claim 5, wherein the carrier gas is nitrogen and the silicon source is silane.

7. The method of claim 2, wherein an epitaxy deposition process is conducted in the process chamber after the removing step.

8. The method of claim 7, wherein the contaminant is selected from the group consisting of oxides, fluorides, chlorides, nitrides, organic residues, carbon, derivatives thereof and

combinations thereof.

9. The method of claim 8, wherein the substrate is exposed to a wet clean process prior to positioning into the process chamber.

10. The method of claim 9, wherein the substrate is exposed to ambient conditions for a period of time in a range from about 6 hours to about 24 hours after the wet clean process and before positioning into the process chamber.

11. The method of claim 8, wherein the silicon-containing material further comprises a rough surface that is removed during the removing step.

12. The method of claim 1, wherein the step of removing further comprises:
forming a recess in a source and drain area on the substrate.

13. A method of smoothing a silicon-containing material on a substrate surface, comprising:
positioning a substrate into a process chamber, wherein the substrate contains a silicon-containing material comprising a first surface roughness of about 1 nm RMS or greater;
exposing the silicon-containing material to an etching gas comprising an etchant, a silicon source and a carrier gas at a temperature less than 800° C.; and
redistributing the silicon-containing material to form a second surface roughness of less than about 1 nm RMS.

14. The method of claim 13, wherein a predetermined thickness of the silicon-containing material is removed at a rate in a range from about 2 Å per minute to about 20 Å per minute.

15. The method of claim 13, wherein the process chamber is maintained at a temperature in a range from about 500° C. to about 700° C.

16. The method of claim 15, wherein the carrier gas is selected from the group consisting of nitrogen, argon, helium and combinations thereof.

17. The method of claim 16, wherein the silicon source is selected from the group consisting of silane, disilane, dichlorosilane, tetrachlorosilane, hexachlorodisilane, derivatives thereof and combinations thereof.

18. The method of claim 17, wherein the etchant is selected from the group consisting of chlorine, chlorine trifluoride, tetrachlorosilane, derivatives thereof and combinations thereof.

19. The method of claim 18, wherein the carrier gas is nitrogen, the silicon source is silane and the etchant is chlorine gas.

20. The method of claim 15, wherein an epitaxy deposition process is conducted in the process chamber after the redistributing step.

21. The method of claim 20, wherein the silicon-containing material further comprises a contaminant that is removed during the redistributing step and the contaminant is selected from the group consisting of oxides, fluorides, chlorides, nitrides, organic residues, carbon, derivatives thereof and combinations thereof.

22. The method of claim 20, wherein the substrate is exposed to a wet clean process prior to positioning into the process chamber.

23. The method of claim 22, wherein the substrate is exposed to ambient conditions for a period of time in a range from about 6 hours to about 24 hours after the wet clean process and before positioning into the process chamber.

24. The method of claim 13, wherein the step of redistributing further comprises:
forming a recess in a source and drain area on the substrate.

25. A method of etching a silicon-containing monocrystalline material on a substrate comprising at least a second material selected from the group consisting of a nitride material, an oxide material or combinations thereof, comprising:
positioning a substrate into a process chamber;
exposing the substrate to an etching gas comprising chlorine gas and a carrier gas at a temperature less than 800° C.;
removing a predetermined thickness of the silicon-containing monocrystalline material to form an exposed monocrystalline surface; and
depositing an epitaxy layer on the exposed monocrystalline surface in the process chamber.

26. The method of claim 25, wherein the etching gas further comprises a silicon source selected from the group consisting of silane, disilane, dichlorosilane, tetrachlorosilane, hexachlorodisilane, derivatives thereof and combinations thereof.

27. The method of claim 25, wherein the process chamber is maintained at a temperature in a range from about 500° C. to about 700° C.

28. The method of claim 27, wherein the carrier gas is selected from the group consisting of nitrogen, argon, helium and combinations thereof.

29. The method of claim 28, wherein the predetermined thickness of the monocrystalline material is removed at a rate in a range from about 200 Å per minute to about 1,000 Å per minute.

30. The method of claim 29, wherein the process chamber is maintained at a pressure in a range from about 10 Torr to about 750 Torr.

31. The method of claim 30, wherein the epitaxial layer comprises a material selected from the group consisting of silicon, silicon-germanium, silicon-carbon, silicon-germanium-carbon, derivatives thereof and combinations thereof.

32. The method of claim 25, wherein removing the predetermined thickness of the silicon-containing monocrystalline material forms a recess formation within a source/drain area on the substrate.

33. The method of claim 32, wherein the source/drain area is used within a device selected from the group consisting of CMOS, Bipolar or BiCMOS application.

34. The method of claim 25, wherein the step of removing further comprises:
forming a recess in a source and drain area on the substrate.

35. A method of forming a silicon-containing monocrystalline material on a substrate, comprising:
exposing a substrate to a HF-last wet clean process;
positioning the substrate into a process chamber;
exposing the substrate to an etching gas comprising chlorine gas and a carrier gas at a temperature less than 800° C.;
removing a predetermined thickness of the silicon-containing monocrystalline material to form an exposed monocrystalline surface;
depositing an epitaxy layer on the exposed monocrystalline surface in the process chamber; and cleaning the process chamber with the chlorine gas to remove silicon-containing contaminant adhered thereon.

36. The method of claim 35, wherein the epitaxy layer is deposited by a deposition gas containing the chlorine gas.

37. The method of claim 36, wherein the carrier gas is nitrogen.

38. The method of claim 37, wherein nitrogen is co-flowed with the chlorine in the deposition gas and during the process chamber clean step.

39. The method of claim 35, wherein the step of removing further comprises:
forming a recess in a source and drain area on the substrate.

40. The method of claim 35, wherein the process chamber is maintained at a temperature in a range from about 500° C. to about 700° C.