

METHOD OF FORMING AN OPTICAL DEVICE AND OPTICAL DEVICE

Field of the Invention

The invention relates to methods of forming light emitting devices. In particular, but not exclusively, the invention relates to light emitting devices with optimised light extraction.

Background of the Invention

It is known that light emitting diode (LED) devices provide efficient sources of light for a wide range of applications. Increases in LED light generation efficiency and extraction, along with the production of smaller LEDs (with smaller light emitting surface areas) and the integration of different wavelength LED emitters into arrays, has resulted in the provision of high quality colour arrays with multiple applications, in particular in display technologies.

Several display technologies are being considered and used for Micro LED Displays for use in various applications, including Augmented Reality, Merged Reality, Virtual Reality and Direct view displays, such as Smart Watches and Mobile devices. Technologies such as Digital Micro Mirrors (DMD) and Liquid Crystal on Silicon (LCoS) are based on reflective technologies, where an external light source is used to produce Red, Green and Blue photons in time sequential mode and the pixels either divert the light away from an optical element (DMD) or absorb light (LCoS) to adjust the brightness of a pixel in order to form an image. Liquid Crystal Displays (LCD) typically use a back light, an LCD panel on an addressable back plane and colour filters to produce an image. A back plane is required to turn individual pixels on and off and to adjust the brightness of individual pixels for each frame of video. Increasingly, emissive display technologies such as Organic Light Emitting Diode (OLED) or Active Matrix OLED (AMOLED) and more recently, Micro LED as they offer lower power consumption for untethered micro display applications and higher image contrast. Micro LED, in particular, offers higher efficiency and better reliability than micro OLED and AMOLED displays.

The invention being described in this document relates to a method for making a highly efficiency micro LED array combining techniques to improve Internal Quantum Efficiency (IQE) and Light Extraction Efficiency (LEE) to improve efficiency and brightness figures of merit.

Structures designed to increase light extraction efficiency are well known in the LED industry, including the use of a pseudo parabolic shaped MESA, to direct photons, generated in the multiple quantum wells (MQW), to an emitting surface.

The technique used to fabricate a MESA with such a shape involves a technique such as Reactive Ion Etch (RIE) or Inductively Coupled Etch (ICP). In such etch techniques, a high energy plasma comprising RF, high voltage (DC bias) and reactive gases, often including free radicals, is used to selectively etch the semiconducting material. The features are defined using a photolithographic process using a photo sensitive material to define areas which will be subject to the etch process and area which will remain un-etched. The precise shape of the MESA can be controlled by the profile of the photo sensitive material used to define the pattern and by etch pressure, power, gas flow and gas species.

Not only does this complicate the manufacturing process, but as a result of this etch process, the edge of the MESA can become damaged which affects the IQE of the micro LED.

As shown in Figure 1, as DC bias and Plasma density increases, more damage is done to the edge of the feature leading to surface leakage path formed by crystal damage, nitrogen vacancies and dangling bonds. Dry etching generates many crystal defects due to the high energy ion bombardment at the surface. Dangling bonds are easily oxidized and crystal damage generates many defect levels in the energy bands which act as carrier recombination centers at the surface, leading to non-radiative recombination.

The surface recombination velocity (non-radiative recombination velocity) is faster than the radiative recombination velocity in the bulk MQW, therefore the small micro LED is vulnerable to surface recombination and a consequential reduction in IQE.

A widely reported consequence of the damage caused during MESA etch is efficiency reduction with smaller micro LED dimensions, as shown in Figure 2. External Quantum Efficiency (EQE) is the product of internal quantum efficiency IQE (the ratio of the number of photons generated to the number of electrons) and the light extraction efficiency LEE (the ability to extract light out of from the p-n junction into the surroundings). The mechanism that drives this trend is the ratio of the perimeter of the micro LED to the area. As the micro LED reduces in size, the area of the sidewall increases in relation to the area of the MQWs so the surface leakage path at the edge of the micro LED causes increases in non-radiative recombination.

The efficiency of micro LEDs can be significantly increased by repairing the damage caused by the MESA etch, as shown in Figure 3. It is typically possible to effect a 10-fold improvement in EQE by executing an optimized damage repair regime. The peak EQE increases after damage repair and the peak EQE occurs at a lower current density so that at the typical operating conditions, a 10-fold increase in efficiency can be obtained. Such a regime, is not compatible however with preserving a MESA shape which is optimized for high LEE, as the repair process removes the semiconductor material which is damaged by the MESA etch, as shown in Figure 4.

Summary of the Invention

In order to mitigate for at least some of the above-described problems there is provided a method of forming one or more optical devices in accordance with the appended claims. Further, there is provided an optical device in accordance with the appended claims.

In a first aspect of the invention, there is provided a method of manufacturing an optical device, the method comprising the steps of (a) forming spacers on the substantially vertical sidewalls of a sacrificial mesa, the spacers being formed from a first electrically insulating, optically transparent material, and having an internal face contacting the mesa, and a second opposing external face; (b) depositing a reflective metallic layer so as to form a mirror layer on the external face of the spacers; (c) removing the sacrificial mesa so as to form a pocket between the internal faces of the spacers; and (d) installing a die having substantially vertical sidewalls into the pocket between the internal faces of the spacers.

Advantageously, the spacer material acts as an optical component to enhance light extraction from the die, whilst the metallic material acts as mirror layer on the sides of the spacers further enhancing light extraction.

Preferably the external faces of the spacers are angled relative to the internal faces.

Preferably the external faces of the spacers have a pseudo-parabolic profile. The parabolic shape works to direct emitted photons towards the light emitting surface of the device such that they are incident on said surface at an angle of incidence below the critical angle, thereby allowing photons to be extracted into air at a high frequency.

Preferably the profile of the external faces of the spacers approximate a Bézier curve having two control points with a Bézier coefficient of 0.5. This has been found to provide the maximum light extraction.

Preferably the spacers are forms of silicon nitride, silicon oxide or tin oxide.

Preferably the method further comprises the step of depositing a transparent conducting oxide over the die and spacers, which forms an electrical contact to the underlying die as well providing protection.

Preferably the transparent conducting oxide is indium tin oxide.

Preferably the transparent conducting oxide forms an electrical contact to the die, and a second electrical contact is formed on the opposing surface of the die.

Preferably the method further comprises the step of forming a light extraction feature on the transparent conducting oxide above the underlying die. The light extraction feature provides a further enhancement to the optical properties of the device.

Preferably the light extraction feature is in the form of convex lens.

Preferably the method further comprises the step of depositing a second electrically insulating, optically transparent material on the external face of each of the spacers, the second electrically insulating, optically transparent material having a different refractive index to that of the first electrically insulating, optically transparent material. This allows for the use of materials with graduated indices of refraction, such that the emitted photons can be better directed towards the light emitting surface.

Preferably the refractive index of the first material is greater than that of the second material such that light is increasingly reflected back towards the light emitting surface of the optical device

Preferably the method further comprises the step of applying index-matching material filler between the die and the internal faces of the spacers.

Preferably the sacrificial mesa is first created by forming two trenches either side of a designated region in a layer of sacrificial material.

Preferably the reflective metallic layer is further deposited along the exposed bottom portion of each of the trenches so as to act as a current spreading layer to the transparent conducting oxide.

Preferably the method further comprises the step of filling the trenches with an insulating material.

Preferably the die comprises an n-doped layer, a p-doped layer, and an active region configured to emit light when electrical current is applied to the die.

Preferably the sidewalls of the die are coated in an optically transparent, electrically insulating material.

In a second aspect of the invention there is provided an optical device manufactured according to steps (a)-(c), as well as any of the further steps described above.

Detailed Description of an Embodiment of the Invention

A detailed description of embodiments of the invention is described, by way of example only, with reference to the figures, in which:

Figure 1 shows a crystal damage to InGaN material with increasing plasma power and DC bias;

Figure 2 shows external quantum efficiency (EQE) vs current density for micro LED sizes reducing from A1 (256 μm) to A9 (1 μm).

Figure 3 shows the EQE of a micro LED with and without MESA damage reduction and repair.

Figure 4 shows a cross section of an etched MESA, pre (a) and post (b) damage repair process.

Figures 5-10 show the stages of the monolithic manufacturing process for the optical devices.

Figure 11 shows an optical device according to an aspect of the present invention.

Figure 12 shows the pixel configuration according to an aspect of the present invention.

Figures 13-16 show various embodiments of optical devices according aspects of the present invention.

Figure 17 shows embodiments wherein the optical device has a square (a), circular (b), triangular (c) and pentagonal (d) cross-section.

Figure 5(a) depicts a preliminary stage in the manufacturing process wherein a CMOS wafer 100 is prepared having a top layer composed of alternating metal 110 and oxide 120 regions. This structure is formed by known means.

At the stage shown in Figure 5(b), a separate carrier wafer 200 is prepared having a routinely spaced mesas formed of a sacrificial material 210. In an embodiment the sacrificial material is metal. In an alternative embodiment the sacrificial material is photoresist. In a further embodiment the sacrificial material is a LED chip. The skilled person appreciate that any suitable (i.e. easily patternable/positionable and removable) material may be employed for this purpose.

At the stage shown in Figure 5(c), optically transparent, electrically insulating spacers 220 are formed on the sidewalls of each of the sacrificial mesas 210, the spacer material having an index of refraction n_1 . Whilst the spacers 220 are illustrated having a sloped profile, they may also be parabolic. In an embodiment the spacers are formed by depositing a conformal coating of silicon dioxide via a known process and the resulting film is etched back using RIE etch to form uniform spacers 220. In alternative embodiments, the spacers are formed via different known dry etch processes, or via nanoimprint lithography or an embossing process. In a further embodiment the spacers are formed from silicon nitride or titanium oxide.

At the stage shown in Figure 6(a) a reflective, electrically conducting material 230 is conformally deposited across the upper surface of the carrier wafer 200, spacers 220 and sacrificial mesas 210. In an embodiment, the reflective, electrically conducting material 230 is a metal. In an embodiment, the reflective, electrically conducting material 230 is formed from aluminium and has a surface roughness of $R_a = 50$ nm. In a preferred embodiment the reflective, electrically conducting material 230 has a surface roughness of $R_a < 10$ nm. In an embodiment, the reflective, electrically conducting material 230 is deposited by a sputtering process, though the skilled person would be aware that any suitable material and/or depositing process may be employed.

At the stage shown in Figure 6(b), a silicon dioxide layer 240 is deposited and chemically mechanically polished such that it fills the voids between subsequent sacrificial mesas 210. The skilled person would again appreciate that any suitable insulating material could be used.

At the stage shown in Figure 7, the carrier wafer 200 is inverted and subsequently bonded to the CMOS wafer 100 of Figure 5 such that the metal regions 110 on the surface of the CMOS wafer 100 line up with the sacrificial mesas 210 of the carrier wafer 200. Bond adhesion is achieved using the silicon dioxide layer 240 by means known to the skilled person.

At the stages shown in the Figures 8(a) and 8(b), the carrier wafer 200 is removed by known means (such as a wet or dry etch) along with the underlying sacrificial mesas 210 and the corresponding portion of the reflective electrically conducting material 230, thereby creating pockets to receive light emitting structures such as dies 300.

At the stage shown in Figure 9(a), light emitting structures in the form of individual LED dies 301, 302 and 303 are installed in the pockets such that the vertical sidewalls of the dies fit between and run parallel to the vertical sidewalls of the spacers 220 left by the removal of the sacrificial mesas 210. The bottom face of each die is in contact with a corresponding metal region 110 of the CMOS wafer, thus forming an addressable electrical contact between to each die. In an embodiment, the vertically of the die sidewalls is achieved via a wet chemical etch, though the skilled person would know of other methods that could be applied employed to this end. In the illustrated embodiment, the dies are positioned such that they alternate in colour from red 301, to green 302, to blue 303 – the skilled person would however understand that any pattern of dies could be used depending on the ultimate application, with a further example provided in Figure 12.

At the stage shown in Figure 9(b), index matching material 305 (i.e. material having a refractive index matching that of the spacers 220) is applied to fill any gaps between the dies 300 and the spacers 220 either side. Multiple alternative index matching material will be known to the skilled person, and the selection of a particular material will naturally depend on the material used to form the spacers 220.

At the stage shown in Figure 10(a), a blanket transparent conducting oxide layer 400 is applied to the topmost surface via a known process, covering the dies 300 and spacers 220. In an embodiment, the transparent conducting oxide is formed of indium tin oxide (ITO), though the skilled person would understand that any suitably transparent and conducting material could be used. The application of the transparent conducting oxide layer 400 provide a common electrode for each of the underlying dies, with the reflective, electrically conducting material 230 applied between successive spacers 220 acting as a current spreading layer across the transparent conducting oxide layer 400.

In order to further increase the light extraction efficiency, the refractive index of the transparent conductive oxide 400 may be varied through variation in the porosity of the transparent conductive oxide. One known method for varying the porosity of a transparent conductive oxide, such as ITO, is oblique-angle deposition using electron-beam evaporation. By varying the angle of the deposition surface relative to the vapour flux deposition, the amount of shadow cast by as-deposited material may be controlled, thereby controlling the porosity of the as-formed layer. Further explanation of oblique angle deposition for ITO may be found in at least "Light-Extraction Enhancement of GaInN Light Emitting Diodes by Graded-Refractive-Index Indium Tin Oxide Anti-Reflection Contact", Jong Kyu Kim et. al., Advanced Materials, 0000, 00, 1-5.

As illustrated in Figure 10(b), certain slots are intentionally left as blank slots 370 to be fitted with a die of the required colour/specification at a later stage should one of the already installed die 360 be identified as sub-standard or otherwise non-functional. Accordingly, dies with sub-optimal performance can either be individually replaced, or intentionally damaged/deactivated and a corresponding die placed in the blank slot 370.

Figure 11 shows an exemplary chip structure of the LED dies 300. As illustrated, the die is formed with a multilayer structure having an active layer 310 configured to emit light when exposed to an electrical current. The active layer 310 is sandwiched between an n-cladding layer 320 such as n-doped gallium nitride and a p-cladding layer 330 such as p-doped gallium nitride. In an embodiment the active layer 310 contains multiple quantum wells. In further embodiments, alternative die structures are used having alternative and/or additional layers. The skilled person would appreciate that any number of potential dies can be used providing they operate as described below. In a particular embodiment, the die 300 includes an electron blocking layer situated between the p-cladding layer 330 and the active layer 310. In a further embodiment, the die 300 includes one or more buffer layers. The die structure has a top light emitting surface 321. As is illustrated, a p-contact layer 340 is provided in contact with the p-cladding layer 320. In an embodiment, the p-contact layer 340 is formed of a reflective material. As can be seen from at least Figure 9, the p-contact layer 340 forms a first electrical contact with the metal region 110 of the CMOS wafer, with a second electrical contact being made to the n-contact layer via the transparent conducting oxide layer 400. The sidewalls of the die are coated in a transparent, electrically insulating layer 350. In an embodiment, the transparent, electrically insulating layer is formed of silicon dioxide.

Figure 12 shows a top down view of one possible two-dimensional die configuration, with a blank slot 320 for redundancy purposes.

The above process produces an array of optical device 500 each consisting of a die 300 and the immediately neighboring spacers 220. An individual optical device 500 is shown in isolation in Figure 13. For simplicity, only the active layer 310, n-cladding layer 320 and p-cladding layer 330 of the die 300 are shown. The columns of index matching material 305 are disposed between the die 300 and the internal faces of the spacers 220, with the reflective, electrically conducting material 230 disposed in the external faces of the spacers 220.

Whilst the spacers 220 are shown in Figure 13 as having straight external faces angled outward relative to the internal faces and the sidewalls of the die 300, Figure 14 depicts an alternative embodiment in which the external faces of the spacers 220 have a pseudo-parabolic profile. The external faces can have any suitable profile described by a range of Bézier curves having two control points and coefficients B – where B is any of 0.1, 0.5, 0.2 and 0.05. In a preferred embodiment, the Bézier coefficient is 0.5, resulting in approximately straight, outwardly sloping profile as shown in Figure 13.

Figure 15 depicts a further embodiment in which a light extraction feature 410 is formed above the light emitting surface of the die 300. Whilst the light extraction feature 410 is depicted in the form of a convex lens, the skilled person would appreciate that it may be provided in any suitable form depending on the application. In a preferred embodiment, the light extraction feature 410 is in the form of a lens having a radius of curvature of 3 μm . In an embodiment, the light extraction feature 410 is patterned into the transparent conducting oxide layer 400 itself. In an alternative embodiment, it is provided by a separate layer formed of a suitable transparent material, such as resin.

Figure 16 depicts an embodiment in which the spacers 220 are each formed of an inner portion 220a and an outer portion 220b having refractive indices n_1 and n_2 respectively. In a preferred embodiment, $n_1 > n_2$ which can be achieved by using silicon nitride as the inner spacer material and aluminium oxide as the second spacer material. In a further embodiment, additional spacer layers can be used with a decreasing index of refraction away from the sidewalls of the light emitting structure 300 (i.e. $n_1 > n_2 > n_N$). Whilst depicted as two separate spacers in schematic Figure 16, the spacers can in fact be formed as a continuous layer, as shown in the cross-sectional views depicted in Figure 17, with the dies 300 having any preferred cross-section shape providing a corresponding void is created in the spacers 220 such that the die 300 can be located.

It will be understood by the skilled person that the pseudo-parabolic spacers 220 of Figure 14, the light extraction feature 410 of Figure 14 and the compound spacer material of Figure 16 are not mutually exclusive and can be combined into further embodiments having one or more or all of these features.

In use, a current is applied between the electrodes formed by the transparent conducting oxide 400 (in contact with the n-cladding layer 320 of the die 300) and the p-contact layer 340 on the bottom surface of the die 300, with the electrically conducting material 230 further operating as a current spreading layer. Light emitted by the active layer 310 is directed towards the light emitting top surface 321 either directly or i) via reflection from the electrical conducting material 230 on the external faces of the spacers 220, ii) via reflections and/or refractions at the spacers 220, iii) via the reflective p-contact layer 340 or iv) via multiple reflections within the structure including combinations of the above. Accordingly, the electrically conducting material 230, spacers 220 and reflective p-contact layer 340 are arranged to increase the proportion of light incident on the light emitting surface within the critical angular range to allow for transmission of light.

The claimed invention thus provides optical devices 500 having improved light collimation via a method of manufacture in which the sloped-profile spacers 220 are pre-formed on a substrate to receive dies 300 – thereby allowing for defective dies to be replaced or deactivated in favour of previously redundant dies.