## Description

### TECHNICAL FIELD

The present invention comprises a method of controlling the frequency of a coherent radio-receiver which receives, via a channel which is subjected to interferencies, signal-sequencies which include at least one synchronizing-sequence and at least one data-sequence, said method comprising the following signal-processing stages:

- converting a received signal-sequence to a baseband signal
- A/D-converting the baseband-signal to signal-points in a signal plan intended for analysis;
- adapting a Viterbi-algorithm having a desired number of states and a path-memory of desired length to the prevailing interferencies in the channel, with the aid of an adaptation signal from the synchronizing-sequence; and
- Viterbi-analyzing the analysis-intended signal-points in the data sequence individually, with the aid of a relatively large number of calculating-stages for the purpose of finally determining the bit-sequence of the signal-points, said number of stages being contingent on the length of the path-memory and an arrangement for carrying out the method.

### BACKGROUND ART

In many radio transmission systems, for instance time-shared so-called TDMA-systems, it is important that transmitter and receiver are well synchronized. It is also highly important that the local frequency generator of the receiver is locked very accurately to the transmitter frequency, particularly in the case of coherent transmission systems. An arrangement of apparatus for such a radio-transmission system is described in the article "Radio Test Performance of a Narrowband System" by Sjernvall, Hedberg and Ekemark, published in IEEE Vehicular Tech. Tampa, Florida, USA, June 1987.

The frequency error in the receiver where the receiver-frequency has been at least roughly set is estimated in a frequency-error calculating device, and a control processor generates a correction signal for each new transmitted signal sequence in accordance with the size of the correction obtained during the preceding signal sequence, and in accordance with the estimated frequency error. The correction signal is sent to a controllable local oscillator, according to the aforesaid article a so-called frequency synthesizer, which is constructed to generate mixing signals, the frequencies of which are corrected in dependence on the control-processor signal. This signal is digital and in practice is converted to analogue form in a digital/analogue converter before being sent to the local oscillator. Consequently, the number of stages in which the oscillator output frequency can be adjusted is dependent on the number of binary bits which the converter is able to convert. When a relatively small and simple converter is used, either the maximum frequency swing from the local oscillator will be small or the frequency stages will be relatively large.

The transmitted signal can be subjected to interferences in systems of the aforesaid kind. These interferences or disturbances may, for instance, be in the form of an added noise-signal or in the form of multiple-path propagation due to repeated reflection of the signal against buildings, mountains etc.. This is often the case in mobile radio transmissions, as is described in an article published in the Norwegian Technical Journal Telektronikk Nr 1, 1987, Torleiv Maseng and Odd Trandem: "Adaptive digital phase modulation". The article describes a coherent receiver which incorporates an equalizer in the form of an adaptive Viterbi-analyser as equalizer. As mentioned in the aforegoing, the transmitted signal similarly comprises periodically recurring signal sequences which include a synchronizing sequence and a data sequence. The signals are frequency-mixed and converted in an analogue-digital converter, in the aforedescribed manner, and stored in a memory. The Viterbi-analyzer is adapted to the prevailing transmission characteristics of the channel with the aid of the synchronizing sequence, these characteristics being determined primarily by said multiple-path propagation. The data sequence is analyzed in the Viterbi-analyzer for the purpose of extracting the content of the original transmitted signal.

An article in IEEE/IEICE Global Communications Conference, Tokyo, Nov. 15-18, 1987 by Franz Edbauer: "Coded 8-DPSK Modulation with Differentially Coherent Detection - An Efficient Modulation Scheme for Fading Channels" describes a radio receiver equipped with a Viterbi-analyzer. This analyzer assists in controlling the frequency of a received signal. According to this article, the Viterbi-analyzer is set permanently and cannot be adapted to handle variations in channel conditions for instance.

A more detailed description of the Viterbi-algorithm applied in the Viterbi-analyzer is given in Richard E. Blahut: "Theory and practice of error control codes", chapter 12, Addison-Wesley 1983.

### DISCLOSURE OF THE INVENTION

It is mentioned in the aforesaid article published in the journal Telektronikk that during signal transmission a small drift in frequency can occur, which is manifested in the form of a successive phase-shift of the receiver bits. When this phase-shift is small, no compensation is necessary. When the phase-shift reaches a given value, however, there is a danger that a decision-error will be made in the Viterbi-ana-

lyzer when analyzing the data sequence. The present invention is based on the concept of utilizing the states which occur in the Viterbi-analysis to effect an adjustment of the phase of the signal intended for analysis in the Viterbi-analyzer. In this respect there is utilized a preliminary decision on extracted data, taken from the path-memory of the Viterbi-analyzer with a given time-delay. The extracted values are compared with the signal to be Viterbi-analysed, in order to achieve the aforesaid phase-adjustment. The invention has the characterizing features set forth in the accompanying claims.

## BRIEF DESCRIPTION OF THE DRAWINGS

The invention will now be described in more detail with reference to an embodiment thereof and with reference to the accompanying Figures 1 to 7, of which

Figure 1 is a block-schematic illustration of a radio receiver;

Figure 2 is a diagram which illustrates a format for signal sequencies in a time-sharing transmission system;

Figure 3 illustrates a complex numeric coordinate sytem with signal modulation;

Figure 4 is a diagram illustrating time-displaced bit-sequencies;

Figure 5 is a block-schematic which illustrates the inventive radio receiver;

Figure 6 illustrates a complex numeric coordinate system with signal points; and

Figure 7 is a diagram which illustrates a further format for signal sequencies.

## BEST MODE FOR CARRYING OUT THE INVENTION

Figure 1 illustrates schematically a radio receiver intended for a system operating with time-shared transmission of information in digital form. A received signal S is mixed down in a known manner in a receiver stage 1 comprising a low-frequency and an intermediate-frequency stage. The receiver stage 1 receives a high-frequency and an intermediate-frequency signal from a local oscillator 2, for instance a frequency synthesizer. The mixed-down signal, the baseband signal, is converted in an analogue-digital converter and stored in a memory in a buffer 3. A signal is sent from the buffer to a block 4 which includes an equalizer and means for calculating a frequency error. This means may consist in a calculating unit in which the frequency error is calculated on the basis of the successive change in phase-position of the received signal in relation to the anticipated phase-positions of the signal. Data relating to the frequency error is supplied to a control processor 5 which calculates a control signal for correcting the frequency of the local oscillator. This control signal is digital and is converted in a D/A-converter 6 prior to being sent to the local oscillator 2. The mixing signal produced in the converter is changed in small increments, because the D/A-converter 2 will convert only a limited number of bits. This results in a residual frequency error which is liable to cause errors in the transmitted signal. Such a frequency error can also occur in receivers equipped with more accurate frequency-control facilities.

The block 4 produces an output signal S1 which corresponds to the received signal S. The signal S1 is sent to a block 7 which includes a channel-decoder and a speech-decoder, and means for converting the decoded signal S1 to an analogue speech-signal. The speech signal is sent to a loudspeaker 8.

Radio receivers of the kind described briefly in the aforegoing may be included in a system that incorporates time-shared signal transmission. The system will have time-separated channels which are N in number, as illustrated in Figure 2. Each user is assigned a given time slot n during which a signal frequency is transmitted. Each signal frequency includes a synchronizing-sequence S0 and data-sequence D0 which contains the information to be passed-on. The signals in the signal sequencies relevant in the case of the present invention are coherent, and an example of one such coherent signal is illustrated in Figure 3. The signal is represented by a vector V0 in a complex numeric coordinate system with the real axis referenced I and the complex axis referenced Q. A transmitted "1" corresponds to a phase-rotation through one quarter of a revolution in a positive directional sense, whereas a transmitted "0" corresponds to a phase-rotation through one quarter of a revolution between the points A, B, C and D in a negative directional sense. The vector V0 can be given in a conventional manner, by its real and imaginary parts, or in polar coordinates in terms of its length and its angle to the positive I-axis.

Each transmitted "1" and "0" takes up a given time-interval in the signal sequence, the so-called bit time. Figure 4 illustrates schematically a signal diagram in which T identifies time and t0 is the bit time. As before mentioned, the transmitted signal can reach the receiver via a direct path betwen the transmitter and the receiver and via one or more paths with signal-reflection against mountains, buildings etc.. The reflected signals travel a longer path than the direct signal, which results in a time-shift t1 between direct and reflected signals. The time-shift t1 may extend to several bit-times and cause intersymbol interference of the received signal S according to Figure 1. The shorter the bit-time, the more bits that are accommodated within the time shift and the more serious the intersymbol interference.

As mentioned in the aforegoing, the receiver of the Figure 1 embodiment includes an equalizer. The incoming mixed and digitalized signal is processed in

the equalizer, so as to be able to extract the content of the originally transmitted signal. In the case of an inventive receiver constructed in accordance with Figure 5, the equalizer comprises, in a known manner, an adaptive Viterbi-analyzer 10 which is used, in accordance with the invention, to control the frequency of the signal entering the Viterbi-analyzer. The use of a Viterbi-analyzer as an adaptive equalizer is described in the aforesaid article published in the journal Telektronikk and will be outlined summarily herebelow. The Viterbi-analyzer is connected to the buffer 3 shown in Figure 1 via a multiplier 11. The buffer is also connected to a correlator circuit 12 via the multiplier 11 which, in turn, is connected to a filter circuit 13. The output of the filter circuit is connected to the Viterbi-analyzer. The Viterbi-analyzer is provided with a desired number of conditions $M = 2^m$, where m = 2,3 ... .

The Viterbi-analyzer is adapted to the channel states which prevail during a signal sequence, in the following manner. According to Figure 2, the received signal sequence includes the synchronizing sequence SO, which is received by the correlator 12 from the buffer 3. The known synchronizing-sequence is stored in the correlator and the correlator compares the bit-pattern of the known synchronizing-sequence with the wave- form of the received synchronizing-sequence. The correlator sends a signal P to the filter circuit 13, in which a filter is built-up such as to correspond to the transmission properties of the channel during the duration of the received signal-sequence, so-called channel estimation. The Viterbi-analyzer 10 receives the data-sequence DO from the buffer 3, and with the assistance of a signal G from the filter circuit 13 is able to determine the content of the data-sequence DO through a large number of traditional Viterbi-calculations. Assume, for instance, that one of the signal points in DO received by the Viterbi-analyzer 10 lies in a point E1, as illustrated in Figure 6. The position of this point is contingent, inter alia, on the degree of accuracy to which transmitter and receiver are synchronized. Subsequent to full analysis in the Viterbi-analyzer 10, there is determined a final bit sequence which is transmitted with the signal S1 for conversion to a speech signal in accordance with Figure 1. For the purpose of obtaining a better understanding of the invention, it may be instructive to imagine the bit sequence as being converted to a signal- point E2.

As before mentioned, the received bits may undergo a successive phase shift, which in unfavourable circumstances may be so large as to render the possibility of referring the bits to any of the points A, B, C or D in Figure 3 highly improbable. This problem is solved in accordance with the invention by utilizing the conditions in the Viterbi-analyzer 10 for calculating a signal point and by controlling the frequency of the received signal-sequence with the aid of this calculated signal point. This frequency control corresponds to a successive shift in the phase-position of the received signal points.

The final bit-sequence according to the above is determined by means of a large number of calculating stages in the path-memory of the Viterbi-analyzer 10. The number of calculating stages is contingent on the length of the path-memory selected. These calculations take a relatively long time to carry out, i.e. many bit-times, since a large number of bits shall be fed into the path- memory before the calculations can be terminated. Although the use of the position of the signal-point E2 for frequency-control purposes introduces a relatively long time-delay, the use of this signal-point nevertheless lies within the scope of the invention. According to one advantageous embodiment of the invention, subsequent to a few calculating stages in the path-memory, bits which correspond to a time-delay TE are extracted from the Viterbi-analyzer 10 for the purpose of obtaining a relatively small time delay. It is assumed in this respect that there are extracted m+1 bits, corresponding to one state, and one bit for the relevant transition. The bits are extracted by a calculation circuit 14 which obtains the filter values in the filter circuit 13 through a signal H. The extracted bits are converted to a signal-point E3 according to Figure 6, with the aid of the filter values. The signal-point E3 forms an estimation of the final positions of the signal-point in the point E2, and the estimated position E3 differs from the position of the received signal-point E1 by an angle $\Delta\varphi 3$. This estimated position E3 is compared with the received value E1 in a comparison circuit 15. This circuit obtains the position of the estimated signal-point E3 from the calculating circuit 14, and also the position of the received signal-point E1 upstream of the input of the Viterbi-analyzer 10. The values relating to the position of the signal-point E1 are delayed in the time-interval TE in a delay circuit 16, so as to enable these values to be compared with the values of the estimated signal-point E3 delayed in the Viterbi-analyzer 10. As described above, signal-points are extracted sequentially from the data-sequence DO, and the respective received and estimated positions of these signal-points are compared successively in the comparison circuit 15. The values thus obtained, corresponding to the angle $\Delta\varphi 3$, are processed in a filter-and-integrating circuit 17 to form an angle-shift signal V. This signal-processing stage is carried out in accordance with known technical control methods and includes low-pass filtration and integration processes and
may

also include prediction of the angle-shift signal V. Low-pass filtration is carried out for the purpose of reducing the influence of rapidly-varying interference caused by noise, for instance. The low-pass filtered and integrated values V are passed to the multiplier 11, in which complex multiplication is carried out. This

complex multiplication corresponds to a successive shift in the angles of the signal-points. This results in an adjustment to the frequency of the signal passed to the Viterbi-analyzer, the data-sequence DO. The final value of V passed to the multiplier 11 upon completion of a whole signal-sequence SO, DO can be stored and subsequently used when calculating a start-value for frequency-control in the next-arriving signal-sequence in the time-slot of the user with number n. If the signal-point E2 is used for calculating the angle-shift signal V, a relatively slow frequency control is obtained, and the time interval TE corresponds to the time taken to complete a Viterbi-analysis of the received signal-point E1.

It should be noted that in the example above, the signal-points have been given in a complex speech plan with the coordinates I,Q. This has been marked in Figure 5 by connecting the circuits with double signal-paths, one for each coordinate. The signal-points, for example the signal-point E in Figure 6, can be given by a radius R and an angle $\varphi$. If signal-processing is effected with these magnitudes, a circuit corresponding to the multiplier 11 will consist of an addition circuit for adding the low-pass filtered and the integrated value, corresponding to the angle-shift signal V, directly to the phase-positions of the signals.

The aforedescribed inventive embodiment can be utilized in the transmission of signals as soon as a Viterbi-analyzer can be used. Examples of those modulation forms which can be used include QAM-modulation, Qadrature Amplitude Modulation, or GMSK-modulation, Gaussian Minimum Shift Keying.

GMSK-modulation is described in more detail in Conference Proceedings, Digital Cellular Radio Conference, October 12-14 1988, Hagen Westphalia FRG, in an article by Ulrich Langewellpott: "Modulation, Coding and Performance".

There has been described in the aforegoing an inventive arrangement for controlling the phase of the signal arriving at the Viterbi-analyzer. The invention also includes a frequency-control method for application in the aforedescribed arrangement. An inventive method includes the following known stages:

The received signal-sequence S is mixed-down with a known frequency to form a baseband signal. This signal is converted in an analogue/digital converter to signal points (I,Q) which are then stored. The received signal is subjected to interference during signal-transmission e.g due to multiple-path propagation, and the data speed is relatively high, and hence intersymbol interference can occur. Consequently, the received signal is equalized, which is effected, in accordance with the inventive method, with the aid of a known Viterbi-algorithm including a path-memory of desired length. This algorithm is adapted to prevailing channel conditions in a known manner, with the aid of the synchronizing-sequence SO. The transmitted data-sequence DO is analyzed in a Viterbi-analyzer in a relatively large number of calculating stages determined by the length of the path-memory, so as to extract the bit-sequence of the datasequence. The invention includes the following further stages:

Subsequent to carrying out a number of calculating stages on the received signal-point E1, a bit-sequence is extracted. The number of calculating stages is restricted by the length of the path-memory and the bit-sequence is determined by the path selected in the path-memory. The extracted signal-point E3 is calculated, which corresponds to the extracted bit-sequence. The extracted signal-point E3 is delayed by the time-interval TE in relation to the received signal-point E1, due to the fact that the signal-points arrive in a given rythmic sequence for Viterbi-analysis. The received signal-point E1 is branched-up prior to the Viterbi-analysis and the branched signal-point E1 is delayed by the time-interval TE. This state is compared with the state of the extracted signal-point E3 and the angle magnitude $\Delta\varphi 3$ corresponding to the phase-difference of the signal points is calculated. A sequence of angle-magnitudes for consecutive signal-points after E1 is calculated in a similar manner. The angle-magnitudes are processed by a process which includes low-pass filtration and integration,such as to form a shift signal, the angle-shift signal V, by means of which the angle of the incoming signal-points is displaced prior to the Viterbi-analysis.

According to one preferred method, the signal-point E1 is subjected to a few calculating stages prior to extracting the bit-sequence. This results in a short time-interval TE and a relatively rapid frequency control.

A format for the transmitted signal-sequence having a synchronizing sequence SO and a subsequent data-sequence DO has been described above with reference to Figure 2. In this format, the synchronizing-sequence SO is located in the centre of the signal-sequence and surrounded on either side by data-sequencies D1 and D2, as illustrated in Figure 7. An inventive receiver can be constructed so that the frequency of said receiver will be controlled in the following manner upon demodulation of this latter signal-sequence.

The Viterbi-analyzer is adapted through the synchronizing-sequence SO, in the aforedescribed manner. Demodulation of D1 commences at a point D11 and terminates at a point D12. Demodulation of D2, which continues thereafter, commences at a point D21 and terminates at a point D22. Angles which correspond to $\Delta\varphi 3$ for the data-sequence D1 are herewith calculated successively, and the angles are filtered and integrated in the aforesaid manner. Corresponding calculations are then made with respect to the data-sequence D2, wherein the final-value for the angle-shift signal in D1 can constitute the start value for D2. During the processing of a signal-sequence, it is also possible to adapt successively the filter-con-

stants in the filter-and-integrator circuit 17. This adaptation can be effected subsequently, as the number of analyzed signal-points increases and the value of the angle-shift signal V is changed. As before mentioned, the final value of the angle-shift signal in D2 for the terminated signal-sequence can be used for calculating a start-value for the angle-shift signal in the next-following signal-sequence. With respect to the filter constants, the value of the angle-shift signal V obtained for a signal-sequence can also be used to adapt the filter-constants in the next-following signal-sequence. It should be noted that when the transmitted signal-sequence has the format illustrated in Figure 7, it is necessary to store the received signal in a memory, suitably subsequent to A/D-conversion. A signal having the format illustrated in Figure 2 need not be stored.

In the aforedescribed exemplifying embodiments, the transmitted signal-sequence SO, DO has been binary-modulated, as described with reference to Figure 3. The Viterbi-analyzer 10, used for demodulating the signal-sequence, has two possible transitions between the states, corresponding to the two levels in the binary code. The invention can also be applied when the transmitted signal-sequence has several modulation levels, which is often the case when the signal is modulated in accordance with said QAM-modulation. The Viterbi-analyzer, which in this case is used for demodulation and the inventive frequency-control, has several possible transitions between the states. More specifically, the number of transitions is equal to the number of modulation levels of the selected modulation form.

## Claims

1. A method for controlling the frequency of a coherent radio-receiver which receives, via a channel which is subjected to interference, signal-sequences which include at least one synchronizing-sequence and at least one data-sequence, said method comprising the following signal-processing stages:
   - converting (1) a received signal-sequence to a baseband signal
   - A/D-converting (3) the baseband-signal to signal-points in a signal plan intended for analysis;
   - adapting a Viterbi-algorithm (10) having a desired number of states and a path-memory of desired length to the prevailing interferencies in the channel, with the aid of an adaptation signal from the synchronizing-sequence; and
   - Viterbi-analyzing (10) the analysis-intended signal-points in the data sequence individually, with the aid of a relatively large number of calculating-stages for the purpose of finally determining the bit-sequence of the signal-points, said number of stages being contingent on the length of the path-memory,

   characterized in that the method further includes the following signal-processing stages:
   - extracting (14) from each of the signal-points during the Viterbi-analysis, with a delay corresponding to a time-interval (TE), a bit-sequence which has been obtained subsequent to a desired number of calculating stages, said number being restricted by the length of the selected path memory;
   - calculating (14) an extracted signal-point (E3) corresponding to the extracted bit-sequence;
   - dividing (16) the analysis-intended signal-point (E1), corresponding to the extracted signal-point (E3), and delaying (16) said signal-point (E1) by the aforesaid time-interval (TE);
   - comparing (15) the time-delayed (TE), divided signal-point (E1) with the extracted signal-point (E3), and calculating an angular magnitude ($\Delta\varphi 3$) corresponding to the phase-difference of the compared signal-points (E1, E3):
   - calculating (17) corresponding angular magnitudes for the consecutive signal-points in the data-sequence (DO);
   - low-pass filtering (17) the angular magnitudes ($\Delta\varphi 3$) with selected filter constants, and integrating the angular magnitudes to form an angle-shift signal (V); and
   - angularly displacing (11) the analysis-intended signal-points successively in correspondence to the angle-shift signal (V) prior to dividing said signal-point and the time-delay (TE).

2. A method according to Claim 1, characterized in that the bit-sequence extracted in the Viterbi-analysis (10) is extracted subsequent to effecting a few calculating stages in the path-memory prior to finally determining the bit-sequence of the signal-point (E1).

3. A method according to Claim 1 or 2, characterized in that the filter-constants are changed successively in dependence on the number of signal-points analyzed during the low-pass filtration (17) of the angular magnitude ($\Delta\varphi 3$).

4. A method according to Claim 1, 2 or 3, characterized in that upon completion of the analysis of a signal-sequence (SO, DO) the magnitude of the angle-shift signal (V) is used to calculate a start-

stants in the filter-and-integrator circuit 17. This adaptation can be effected subsequently, as the number of analyzed signal-points increases and the value of the angle-shift signal V is changed. As before mentioned, the final value of the angle-shift signal in D2 for the terminated signal-sequence can be used for calculating a start-value for the angle-shift signal in the next-following signal-sequence. With respect to the filter constants, the value of the angle-shift signal V obtained for a signal-sequence can also be used to adapt the filter-constants in the next-following signal-sequence. It should be noted that when the transmitted signal-sequence has the format illustrated in Figure 7, it is necessary to store the received signal in a memory, suitably subsequent to A/D-conversion. A signal having the format illustrated in Figure 2 need not be stored.

In the aforedescribed exemplifying embodiments, the transmitted signal-sequence SO, DO has been binary-modulated, as described with reference to Figure 3. The Viterbi-analyzer 10, used for demodulating the signal-sequence, has two possible transitions between the states, corresponding to the two levels in the binary code. The invention can also be applied when the transmitted signal-sequence has several modulation levels, which is often the case when the signal is modulated in accordance with said QAM-modulation. The Viterbi-analyzer, which in this case is used for demodulation and the inventive frequency-control, has several possible transitions between the states. More specifically, the number of transitions is equal to the number of modulation levels of the selected modulation form.

## Claims

1. A method for controlling the frequency of a coherent radio-receiver which receives, via a channel which is subjected to interference, signal-sequences which include at least one synchronizing-sequence and at least one data-sequence, said method comprising the following signal-processing stages:
   - converting (1) a received signal-sequence to a baseband signal
   - A/D-converting (3) the baseband-signal to signal-points in a signal plan intended for analysis;
   - adapting a Viterbi-algorithm (10) having a desired number of states and a path-memory of desired length to the prevailing interferencies in the channel, with the aid of an adaptation signal from the synchronizing-sequence; and
   - Viterbi-analyzing (10) the analysis-intended signal-points in the data sequence individually, with the aid of a relatively large number of calculating-stages for the purpose of finally determining the bit-sequence of the signal-points, said number of stages being contingent on the length of the path-memory,

   characterized in that the method further includes the following signal-processing stages:
   - extracting (14) from each of the signal-points during the Viterbi-analysis, with a delay corresponding to a time-interval (TE), a bit-sequence which has been obtained subsequent to a desired number of calculating stages, said number being restricted by the length of the selected path memory;
   - calculating (14) an extracted signal-point (E3) corresponding to the extracted bit-sequence;
   - dividing (16) the analysis-intended signal-point (E1), corresponding to the extracted signal-point (E3), and delaying (16) said signal-point (E1) by the aforesaid time-interval (TE);
   - comparing (15) the time-delayed (TE), divided signal-point (E1) with the extracted signal-point (E3), and calculating an angular magnitude ($\Delta\varphi 3$) corresponding to the phase-difference of the compared signal-points (E1, E3):
   - calculating (17) corresponding angular magnitudes for the consecutive signal-points in the data-sequence (DO);
   - low-pass filtering (17) the angular magnitudes ($\Delta\varphi 3$) with selected filter constants, and integrating the angular magnitudes to form an angle-shift signal (V); and
   - angularly displacing (11) the analysis-intended signal-points successively in correspondence to the angle-shift signal (V) prior to dividing said signal-point and the time-delay (TE).

2. A method according to Claim 1, characterized in that the bit-sequence extracted in the Viterbi-analysis (10) is extracted subsequent to effecting a few calculating stages in the path-memory prior to finally determining the bit-sequence of the signal-point (E1).

3. A method according to Claim 1 or 2, characterized in that the filter-constants are changed successively in dependence on the number of signal-points analyzed during the low-pass filtration (17) of the angular magnitude ($\Delta\varphi 3$).

4. A method according to Claim 1, 2 or 3, characterized in that upon completion of the analysis of a signal-sequence (SO, DO) the magnitude of the angle-shift signal (V) is used to calculate a start-



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value for the angle-shift signal in the analysis of the next-following signal-sequence.

5. A method according to Claim 1, 2, 3 or 4, characterized in that during the low-pass filtration (17) of the angle-magnitudes ($\Delta\varphi 3$) in a signal-sequence (SO,DO), the filter constants are calculated in dependence on the value of the angle-shift signal (V) of a preceding signal-sequence.

6. A method according to Claims 1, 2, 3, 4 or 5, in which the signal-sequence consists of in time-sequence a data-sequence, the synchronizing sequence and a further data-sequence, and in which the signal-sequence is stored prior to the Viterbi-analysis (10), characterized in that the magnitude of the angle-shift signal (V) upon completion of the analysis of the one data-sequence (D1) constitutes the start-value of the analysis of the other data-sequence (D2).

7. An arrangement for carrying out the method according to Claim 1, including a coherent radio-receiver which, via a channel which is subjected to interference, receives signal-sequences comprising at least one synchronizing-sequence and at least one data-sequence, said arrangement comprising
   - a receiver stage (1) for signal-reception and conversion of a received signal-sequence to a baseband signal,
   - an A/D-converter (3) which is connected to the receiver stage (1) and which converts the baseband signal to signal-points intended for analysis,
   - an adaptive Viterbi-analyzer (10) which is connected to the A/D-converter (3) and to adaptation circuits (correlator circuit 12, filter circuit 13), said Viterbi-analyzer having a desired number of states and a path-memory of desired length and being adapted to prevailing interferencies in the channel with the aid of an adaptation signal derived by the adaptation circuits from the synchronizing-sequence, and in which arrangement the adapted Viterbi-analyzer processes the analysis-intended signal-points in the data-sequence through a relatively large number of calculating-stages, said number being contingent on the length of the path-memory, and thereby finally determines the bit-sequence of the data-sequence, characterized in that the arrangement further comprises
   - a calculation circuit (14) which is connected to the path-memory of the Viterbi-analyzer (10) and to the adaptation circuits (12,13) and which is operative to extract from the path-memory a bit-sequence which belongs to a signal-point (E1) and which has been obtained subsequent to effecting a desired number of calculating-stages corresponding to a delay of a time-interval (TE), said number of calculating stages being restricted by the length of the path-memory, and being further operative to calculate an extracted signal-point (E3) corresponding to said bit-sequence, with the aid of a signal (H) from the adaptation circuits (correlator circuit 12, filter circuit 13);
   - a delay circuit (16) which is connected to the input of the Viterbi-analyzer (10) and which divides that signal-point (E1) of the analysis-intended signal-points which corresponds to the extracted signal-point (E3) and delays said signal-point (E1) by said time-interval (TE);
   - a comparison circuit (15) which is connected to the calculating circuit (14) and the delay circuit (16) and which is operative to compare the time-delayed signal-point (E1) with the extracted signal-point (E3) and calculate an angular magnitude ($\Delta\varphi 3$) which corresponds to the phase-difference of the compared signal-points (E1,E3);
   - a filter-and-integrator circuit (17) which is connected to the comparison circuit (15) and which low-pass filters and integrates the calculated angular-magnitude ($\Delta\varphi 3$) with corresponding angular magnitudes of consecutive analysis-intended signal-points to an angle-shift signal (V); and
   - an angle-shift circuit (11) which is connected to the filter-and-integrator circuit (17) and to the input of the Viterbi-analyzer (10) and which is operative to displace angularly (V) the analysis-intended signal-point (E1) prior to branching said signal to the time-delay circuit (16).

8. An arrangement according to Claim 7, characterized in that the calculating circuit (14) is constructed to extract the bit-sequence from the path-memory subsequent to effecting a few calculating stages in the path-memory and prior to finally determining the bit-sequence (S1) of the data-sequence.

**Patentansprüche**

1. Verfahren zum Steuern der Frequenz eines kohärenten Radio-Empfängers, welcher über einen Kanal, welcher Interferenzen unterliegt, Signalseqeunzen empfängt, welche zumindest eine Synchronisationssequenz und zumindest ei-



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ne Datensequenz beinhalten, wobei das Verfahren die folgenden Signalverarbeitungsstufen umfaßt:

- Umwandeln (1) einer empfangenen Signalsequenz in einem Basisbandsignal;
- A/D-Wandeln (3) des Basisbandsignals in Signalpunkte in einem Signalplan, der zur Analyse vorgesehen ist;
- Anpassen eines Viterbi-Algorithmus (10) mit einer gewünschten Anzahl von Zuständen und eines Wegspeichers erwünschter Länge an die vorherrschenden Interferenzen in dem Kanal mit Hilfe eines Adaptationssignals von der Synchronisationssequenz; und
- Viterbi-Analysieren (10) der zur Analyse vorgesehenen Signalpunkte in der Datensequenz auf individuelle Art und Weise mit der Hilfe einer relativ großen Anzahl von Berechnungsstufen zum Zweck des letztendlichen Bestimmens der Bitsequenz der Signalpunkte, wobei die Anzahl von Stufen abhängt von der Länge des Wegspeichers;

dadurch gekennzeichnet, daß das Verfahren weiterhin die folgenden Verarbeitungsstufen umfaßt:

- Extrahieren ((14) von jedem der Signalpunkte während der Viterbi-Analyse mit einer Verzögerung entsprechend einem Zeitintervall (TE) einer Bitsequenz, welche erhalten wurde folgend einer gewünschten Anzahl von Berechnungsstufen, wobei die Anzahl beschränkt ist durch die Länge des gewählten Wegspeichers;
- Berechnen (14) eines extrahierten Signalpunktes (E3) entsprechend der extrahierten Bitsequenz;
- Teilen (16) des zur Analyse vorgesehenen Signalpunktes (E1) entprechend dem extrahierten Signalpunkt (E3), und Verzögern (16) des Signalpunktes (E1) um das vorhererwähnte Zeitintervall (TE);
- Vergleichen (15) des zeitverzögerten (TE) geteilten Signalpunktes (E1) mit dem extrahierten Signalpunkt (E3) und Berechnen einer Winkelgröße ( delta phi 3) entprechend der Phasendifferenz der verglichenen Signalpunkte (E1,E3);
- Berechnen (17) entsprechende Winkelgrößen für die folgenden Signalpunkte in der Datensequenz (D0);
- Tiefpaß-Filtern (17) der Winkelgrößen (delta phi 3) mit gewählten Filterkonstanten, und Integrieren der Winkelgrößen, um ein Winkelverschiebungsignal V zu bilden; und
- Winkelverrscheiben (11) der zur Analyse vorgesehenen Signalpunkte sukzessiv in Übereinstimmung mit dem Winkelverschiebungssignal (V) vor dem Teilen des Signalpunktes und der Zeitverzögerung (TE).

2. Verfahren nach Anspruch 1, dadurch gekennzeichnet, daß die in der Viterbi-Analyse (10) extrahierte Bitsequenz extrahiert wird folgend dem Bewirken von wenigen Berechnungsstufen in dem Wegspeicher vor dem endgültiegen Bestimmen der Bitsequenz des Signalpunktes (E1).

3. Verfahren nach Anspruch 1 oder 2, dadurch gekennzeichent, daß die Filterkonstanten sukzessiv abhängig von der Anzahl von Signalpunkten analysiert während der Tiefpaßfilterung (17) der Winkelgröße (delta phi 3) geändert werden.

4. Verfahren nach Anspruch 1, 2 oder 3, dadurch gekennzeichnet, daß bei Vervollständigung der Analyse einer Signalsequenz (S0,D0) die Größe des Winkelverschiebungssignals (V) benutzt wird zum Berechnen eines Startwerts für das Winkelverschiebungssignal bei der Analyse der nächstfolgenden Signalsequenz.

5. Verfahren nach Anspruch 1, 2, 3 oder 4, dadurch gekennzeichnet, daß während der Tiefpaßfilterung (17) der Winkelgrößen (delta phi 3) in einer Signalsequenz (S0,D0) die Filterkonstanten berechnet werden in Abhängigkeit von dem Wert des Winkelverschiebungssignals (V) einer vorhergehenden Signalsequenz.

6. Verfahren nach Anspruch 1, 2, 3, 4 oder 5, wobei die Signalsequenz aus einer Zeitsequenz, einer Datensequenz, der Synchronisationsequenz einer weiteren Datensequenz besteht, und wobei die Signalsequenz gespeichert wird vor der Viterbi-Analyse (10), dadurch gekennzeichnet, daß die Größe des Winkelverschiebungssignals (V) bei Vervollständigung der Analyse der einen Datensequenz (D1) den Startwert der Analyse der anderen Datensequenzen (D2) darstellt.

7. Anordnung zum Ausführen des Verfahrens nach Anspruch 1 einschließlich eines kohärenten Radioempfängers, welcher über einen Kanal, der Interferenz unterliegt, Signalsequenzen empfängt, welche zumindest eine Synchronisationssequenz und zumindest eine Datensequenz umfassen, wobei die Anordnung umfaßt:
   - eine Empfängerstufe (1) zum Signalempfang und Umwandlung einer empfangenen Signalsequenz in einem Basisbandsignal;
   - einen A/D-Wandler (3) welcher mit der Empfängersufe (1) verbunden ist und welcher das Basissignal umwandelt in Signalpunkte, die zur Analyse vorgesehen sind;
   - einen adapativen Viterbi-Analysator (10), welcher mit dem A/D-Wandler (3) und mit



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Adaptationsschaltungen (Korrelatorschaltung 12, Filterschaltung 13) verbunden ist, wobei der Viterbi-Analysator eine gewünschte Anzahl von Zuständen hat und einen Wegspeicher erwünschter Länge und angepaßt ist an vorherrschende Interferenzen in dem Kanal mit Hilfe eines Adaptationssignals abgeleitet durch die Adaptationsschaltungen von der Synchronisationsequenz, und wobei beider Anordnung der adaptierte Viterbi-Analysator die zur Analyse vorgesehenen Signalpunkte in der Datensequenz verarbeitet durch eine relativ große Anzahl von Berechnungsstufen, wobei die Anzahl abhängt von der Länge des Wegspeichers, und dadurch letztendlich die Bitsequenz der Datensequenz bestimmt, dadurch gekennzeichnet, daß die Anordnung weiterhin umfaßt:

- eine Berechnungsschaltung (14) welche mit dem Wegspeicher des Viterbi-Analysators (10) und mit den Adaptationsschaltungen (12,13) verbunden ist und welche arbeitet zum Extrahieren einer Bitsequenz von dem Wegspeicher, welche zu einem Signalpunkt (E1) gehört und welche erhalten wurde nach dem Bewirken einer erwünschten Anzahl von Berechnungsstufen entsprechend einer Verzögerung eines Zeitintervalls (TE), wobei die Anzahl der Berechnungsstufen beschränkt ist durch die Länge des Wegspeichers, und welche weiterhin arbeitet zum Berechnen eines extrahierten Signalpunktes (E3) entsprechend der Bitsequenz mit Hilfe eines Signals (H) von den Adaptationsschaltungen (Korrelatorschaltung 12, Filterschaltung 13);
- eine Verzögerungsschaltung (16), welche verbunden ist mit der Eingabe des Viterbi-Analysators (10) und welche diesen Signalpunkt (E1) der zur Analyse vorgesehenen Signalpunkte teilt, welcher dem extrahierten Signalpunkt (E3) entspricht, und den Signalpunkt (E1) um das Zeitintervall (TE) verzögert;
- eine Vergleichsschaltung (15) welche verbunden ist mit der Berechnungstufe (14) und der Verzögerungsschaltung (16) und welche arbeitet zum Vergleichen des verzögerten Signalpunktes (E1) mit dem extrahierten Signalpunkt (E3) und Berechnen einer Winkelgröße (delta phi 3), welche der Phasendifferenz der verglichenen Signalpunkte (E1,E3) entspricht;
- eine Filter- und -Integrationsschaltung (17), welche mit der Vergleichsschaltung (15) verbunden ist und welche die berechnete Winkelgröße (delta phi 3) Tiefpaß-filtert und integriert mit entsprechenden Winkelgrößen der folgenden zur Analyse vorgesehenen Signalpunkte zu einem Winkelverschiebungssignal (V); und
- eine Winkelverschiebungsschaltung (11), welche verbunden ist mit der Filter- und -Integrationsschaltung (17) und mit der Eingabe des Viterbi-Analysators (10) und welche arbeitet zum Verschieben des Winkels (V) des zur Analyse vorgesehenen Signalpunktes (1) vor dem Abzweigen des Signals für die Zeitverzögerungschaltung (16).

8. Anordnung nach Anspruch 7, dadurch gekennzeichnet daß die Berechnungsschaltung (14) konstruiert ist zum Extrahieren der Bitsequenz aus dem Wegspeicher folgend dem Bewirken von wenigen Berechnungsstufen in dem Wegspeicher und vor dem letztendlichen Bestimmen der Bitsequenz (S1) der Datensequenz.

**Revendications**

1. Procédé pour commander la fréquence d'un récepteur radio cohérent qui reçoit, par l'intermédiaire d'un canal soumis à des interférences, des séquences de signaux qui comportent au moins une séquence de synchronisation et au moins une séquence de données, ledit procédé comprenant les étapes de traitement de signaux suivantes:
   - la conversion (1) d'une séquence de signal reçue en un signal en bande de base;
   - la conversion A/N (3) du signal en bande de base en points de signaux dans un plan signal destiné à une analyse;
   - l'adaptation d'un algorithme de Viterbi (10) ayant un nombre souhaité d'états et une mémoire de trajet de la longueur souhaitée, aux interférences affectant le canal, à l'aide d'un signal d'adaptation provenant de la séquence de synchronisation; et
   - l'analyse par la méthode de Viterbi (10) des points de signaux individuels destinés à l'analyse dans la séquence de données, à l'aide d'un nombre relativement grand d'étapes de calcul ayant pour but de déterminer la séquence binaire des points de signaux, ledit nombre d'étapes dépendant de la longueur de la mémoire de trajet, caractérisé en ce que ce procédé comporte en outre les étapes de traitement de signaux suivantes:
   - l'extraction (14), à partir de chacun des points de signaux, pendant l'analyse de Viterbi, avec un retard correspondant à un intervalle de temps (TE), d'une séquence bi-



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naire qui a été obtenue après un nombre souhaité d'étapes de calcul, ledit nombre étant limité par la longueur de la mémoire de trajet sélectionnée;

- le calcul (14) d'un point de signal extrait (E3) correspondant à la séquence binaire extraite;
- la division (16) du point de signal (E1) destiné à l'analyse, correspondant au point de signal extrait (E3), et l'application d'un retard (16) audit point de signal (E1) de l'intervalle de temps (TE) mentionné précédemment;
- la comparaison (15) du point de signal divisé (E1) retardé (TE) avec le point de signal extrait (E3), et le calcul d'une valeur angulaire ($\Delta\phi 3$) correspondant à la différence de phase entre les points de signaux comparés (E1, E3);
- le calcul (17) des valeurs angulaires correspondantes pour les points de signaux consécutifs de la séquence de données (DO);
- le filtrage passe-bas (17) des valeurs angulaires ($\Delta\phi 3$) avec des constantes de filtrage sélectionnées, et l'intégration des valeurs angulaires pour élaborer un signal de décalage angulaire (V); et
- le déplacement angulaire (11) progressif des points de signaux destinés à l'analyse en correspondance avec le signal de décalage angulaire (V) avant division dudit point du signal et avant le retard temporel (TE).

2. Procédé selon la revendication 1, caractérisé en ce que la séquence binaire extraite par l'analyse de Viterbi (10) est extraite après exécution d'un petit nombre d'étapes de calcul dans la mémoire de trajet et avant la détermination finale de la séquence binaire du point de signal (E1).

3. Procédé selon la revendication 1 ou 2, caractérisé en ce que les constantes de filtrage sont progressivement modifiées en fonction du nombre de points de signaux analysés pendant le filtrage passe-bas (17) de la valeur angulaire ($\Delta\phi 3$).

4. Procédé selon la revendication 1, 2 ou 3, caractérisé en ce que, à l'achèvement de l'analyse d'une séquence de signal (SO, DO), la valeur du signal de décalage angulaire (V) est utilisée pour calculer une valeur de départ pour le signal de décalage angulaire lors de l'analyse de la séquence de signal immédiatement suivante.

5. Procédé selon la revendication 1, 2, 3 ou 4, caractérisé en ce que, pendant le filtrage passe-bas (17) des valeurs angulaires ($\Delta\phi 3$) d'une séquence de signal (SO, DO), les constantes de filtrage sont calculées en fonction de la valeur du signal de décalage angulaire (V) d'une séquence de signal précédente.

6. Procédé selon la revendication 1, 2, 3, 4 ou 5, dans lequel la séquence de signal est constituée séquentiellement dans le temps d'une séquence de données, de la séquence de synchronisation et d'une autre séquence de données, et dans lequel la séquence de signal est stockée préalablement à l'analyse de Viterbi (10), caractérisé en ce que la valeur du signal de décalage angulaire (V), à l'achèvement de l'analyse de la séquence de données (D1), constitue la valeur de départ de l'analyse de l'autre séquence de données (D2).

7. Dispositif pour mettre en oeuvre le procédé de la revendication 1, comportant un récepteur radio cohérent qui, par l'intermédiaire d'un canal soumis à des interférences, reçoit une séquence de signaux comprenant au moins une séquence de synchronisation et au moins une séquence de données, ledit dispositif comprenant:
   - un étage récepteur (1) pour la réception de signaux et la conversion d'une séquence de signal reçue en un signal en bande de base,
   - un convertisseur A/N 3 qui est connecté à l'étage récepteur (1) et qui convertit le signal en bande de base en points de signaux destinés à une analyse,
   - un analyseur de Viterbi adaptatif (10) qui est connecté au convertisseur A/N(3) et à des circuits d'adaptation (circuit corrélateur 12, circuit à filtre 13), ledit analyseur de Viterbi ayant un nombre souhaité d'états et une mémoire de trajet de la longueur souhaitée et étant adapté aux interférences affectant le canal, à l'aide d'un signal d'adaptation déterminé par les circuits d'adaptation à partir de la séquence de synchronisation, dispositif dans lequel l'analyseur de Viterbi adapté traite les points de signaux destinés à l'analyse dans la séquence de données au moyen d'un nombre relativement grand d'étapes de calcul, ledit nombre dépendant de la longueur de la mémoire de trajet, et détermine ainsi finalement la séquence binaire de la séquence de données, caractérisé en ce que ce dispositif comprend en outre:
   - un circuit de calcul (14) qui est connecté à la mémoire de trajet de l'analyseur de Viterbi (10) et aux circuits d'adaptation (12, 13) et qui a pour fonction d'extraire de la mémoire de trajet une séquence binaire qui appartient à un point de signal (E1) et qui a été obtenue après l'exécution d'un nombre



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souhaité d'étapes de calcul correspondant à un retard d'un intervalle de temps (TE), ledit nombre d'étapes de calcul étant limité par la longueur de la mémoire de trajet, et ayant en outre pour fonction de calculer un point de signal extrait (E3) correspondant à ladite séquence binaire, à l'aide d'un signal (H) provenant des circuits d'adaptation (circuit corrélateur 12, circuit à filtre 13);

- un circuit à retard (16) qui est connecté à l'entrée de l'analyseur de Viterbi (10) et qui divise le point de signal (E1) des points de signaux destinés à l'analyse qui correspond au point de signal extrait (E3) et retarde ledit point de signal (E1) dudit intervalle de temps (TE);
- un circuit de comparaison (15) qui est connecté au circuit de calcul (14) et au circuit à retard (16) et qui a pour fonction de comparer le point de signal retardé (E1) au point de signal extrait (E3) et de calculer une valeur angulaire ($\Delta\phi 3$) qui correspond à la différence de phase entre les points de signaux comparés (E1, E3);
- un circuit de filtrage et d'intégration (17) qui est connecté au circuit de comparaison (15) et qui filtre par filtrage passe-bas et intègre la valeur angulaire calculée ($\Delta\phi 3$) à partir des valeurs angulaires correspondantes des points de signaux consécutifs destinés à l'analyse, pour donner un signal de décalage angulaire (V); et
- un circuit de décalage angulaire (11) qui est connecté au circuit de filtrage et d'intégration (17) et à l'entrée de l'analyseur de Viterbi (10) et qui a pour fonction de déplacer angulairement (V) le point de signal destiné à l'analyse (E1) avant branchement dudit signal vers le circuit à retard (16).

8. Dispositif selon la revendication 7, caractérisé en ce que le circuit de calcul (14) est conçu pour extraire la séquence binaire de la mémoire de trajet après l'exécution de quelques étapes de calcul dans la mémoire de trajet et avant la détermination finale de la séquence binaire (S1) de la séquence de données.



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