

ABSTRACT

The embodiments of the application provide a clock generation circuit, a memory and a clock duty cycle calibration method; the clock generation circuit comprises: an oscillation circuit, configured to generate a first oscillation signal and a second oscillation signal, a frequency of the first oscillation signal is same as a frequency of the second oscillation signal, and a phase of the first oscillation signal is opposite to a frequency of the second oscillation signal; a comparison unit, configured to receive the first oscillation signal and the second oscillation signal, and compare the duty cycle of the first oscillation signal and/or the duty cycle of the second oscillation signal; and a logical unit, connected to the comparison unit and the oscillation circuit, and configured to control the oscillation circuit according to an output result of the comparison unit, so that the duty cycle reaches a preset range. The embodiments of the application may generate a first oscillation signal and a second oscillation signal with stable duty cycle that may be used for memory testing.

Fig. 2