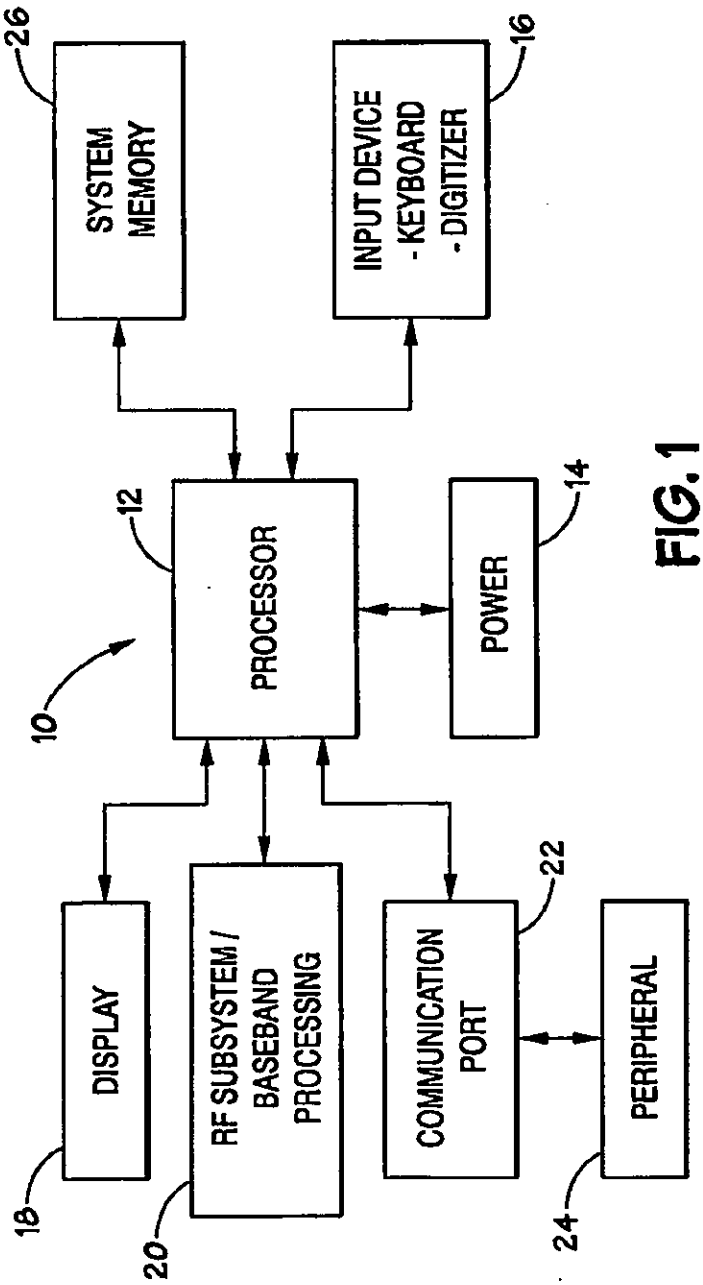

SYSTEM MEMORY
26
INPUT DEVICE
- KEYBOARD
- DIGITIZER
16
PROCESSOR
12
POWER
14
10
DISPLAY
18
RF SUBSYSTEM / BASEBAND PROCESSING
20
COMMUNICATION PORT
22
PERIPHERAL
24

FIG. 1

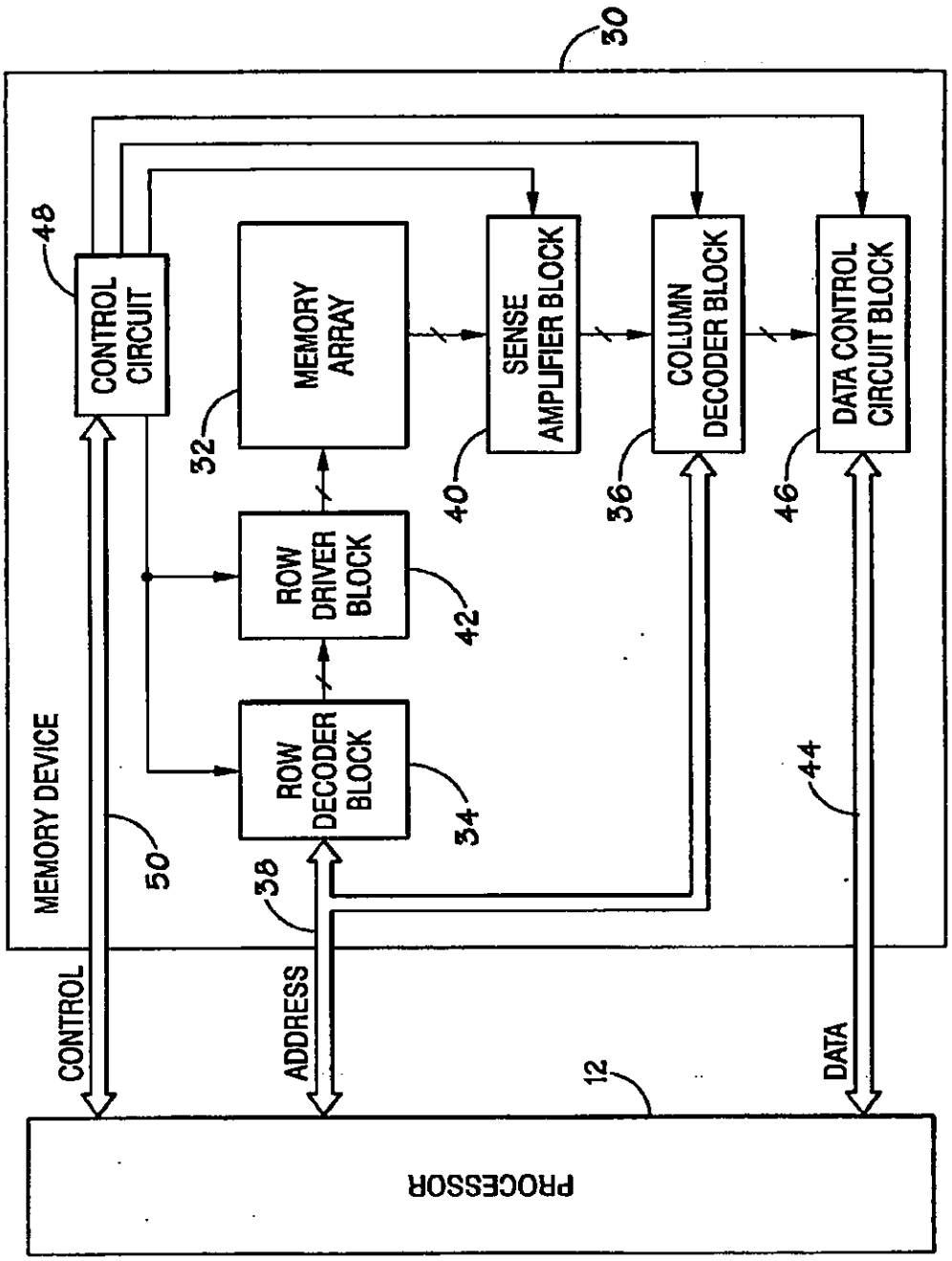

30
48
CONTROL CIRCUIT
MEMORY ARRAY
32
SENSE AMPLIFIER BLOCK
40
COLUMN DECODER BLOCK
36
DATA CONTROL CIRCUIT BLOCK
46
ROW DRIVER BLOCK
42
ROW DECODER BLOCK
34
MEMORY DEVICE
50
38
44
CONTROL
ADDRESS
DATA
12
PROCESSOR

FIG. 2

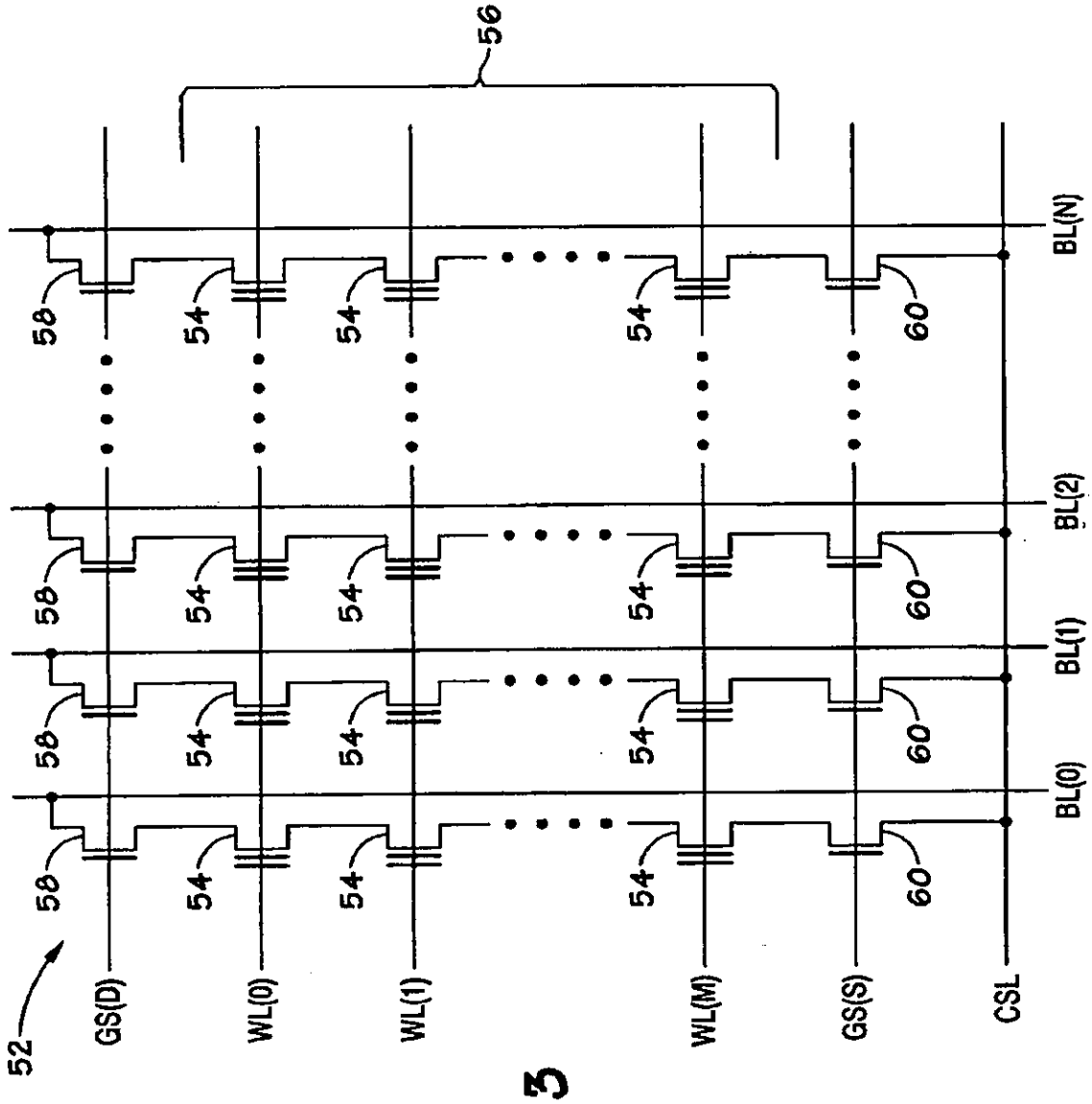



FIG. 3

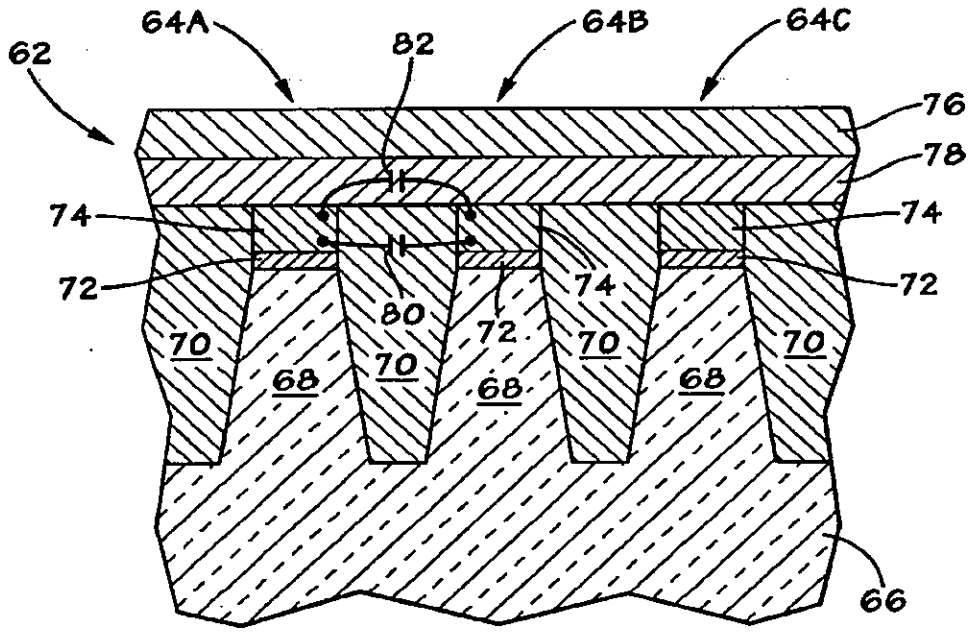

64A
64B
64C
62
82
76
78
74
74
72
72
74
80
72
70
70
70
70
68
68
68
66

FIG. 4

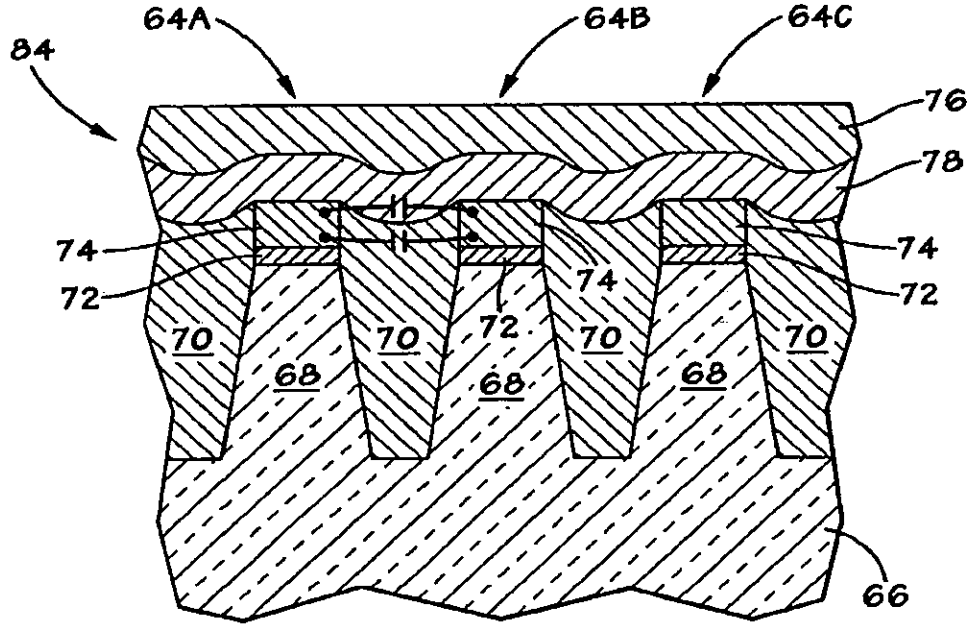

64A
64B
64C
84
76
78
74
74
72
72
74
72
70
70
70
70
68
68
68
66

FIG. 5

FIG. 6

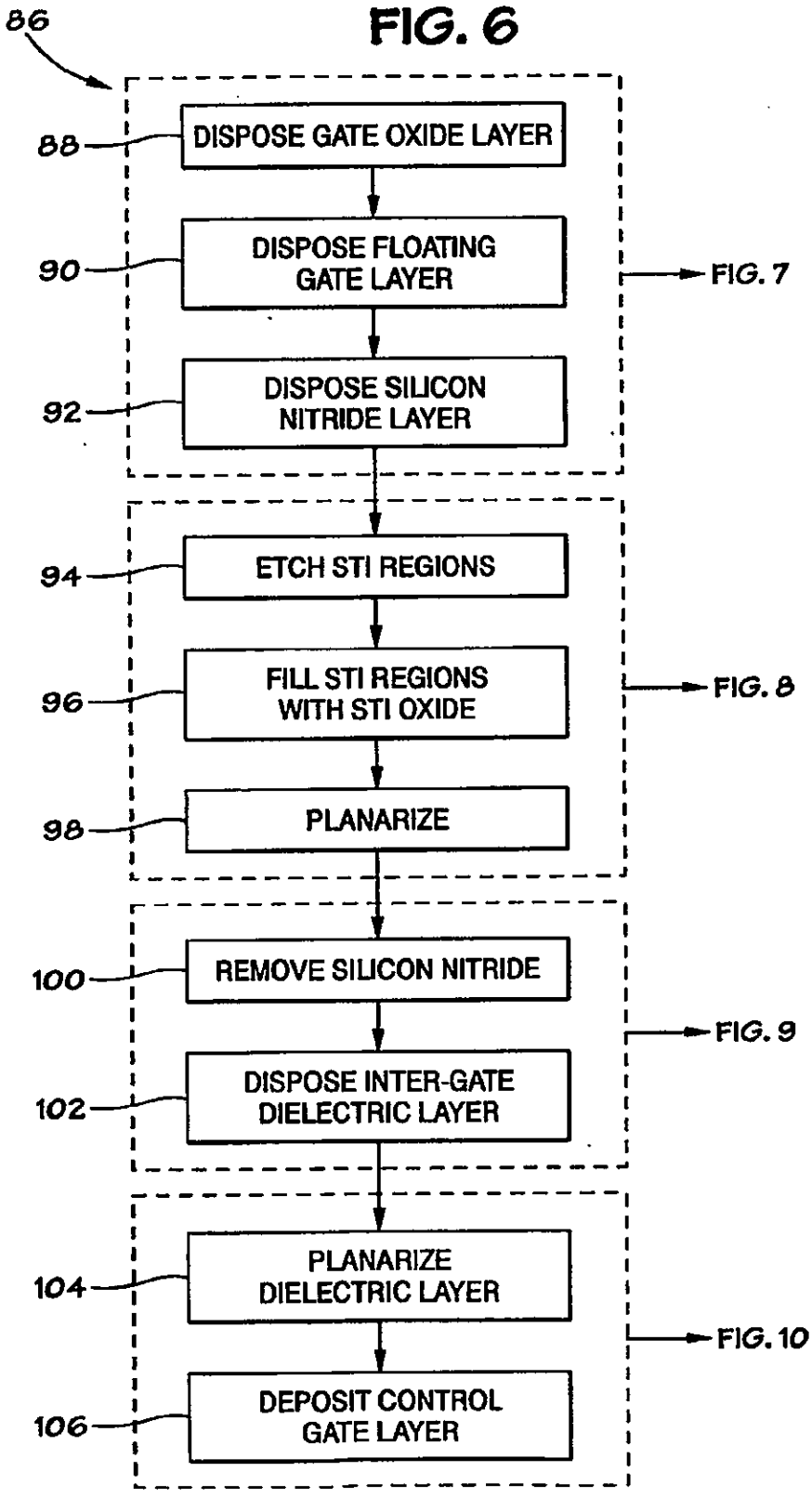
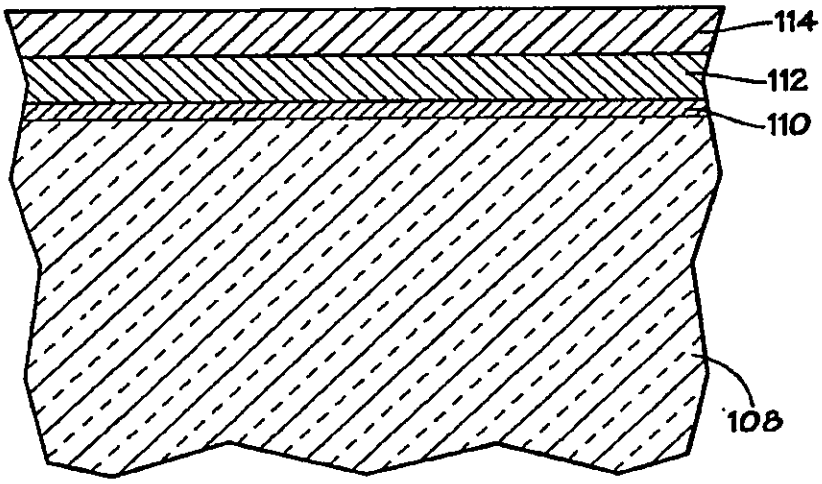

86
88
DISPOSE GATE OXIDE LAYER
90
DISPOSE FLOATING GATE LAYER
92
DISPOSE SILICON NITRIDE LAYER
FIG. 7
94
ETCH STI REGIONS
96
FILL STI REGIONS WITH STI OXIDE
98
PLANARIZE
FIG. 8
100
REMOVE SILICON NITRIDE
102
DISPOSE INTER-GATE DIELECTRIC LAYER
FIG. 9
104
PLANARIZE DIELECTRIC LAYER
106
DEPOSIT CONTROL GATE LAYER
FIG. 10

FIG. 7



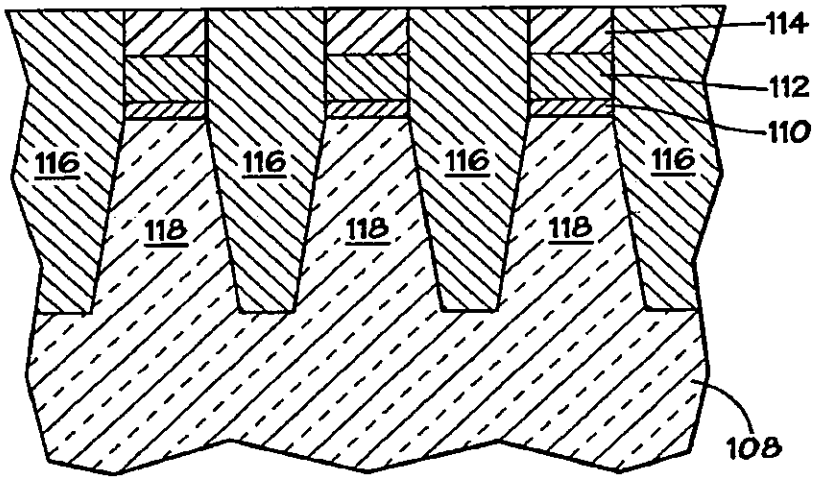
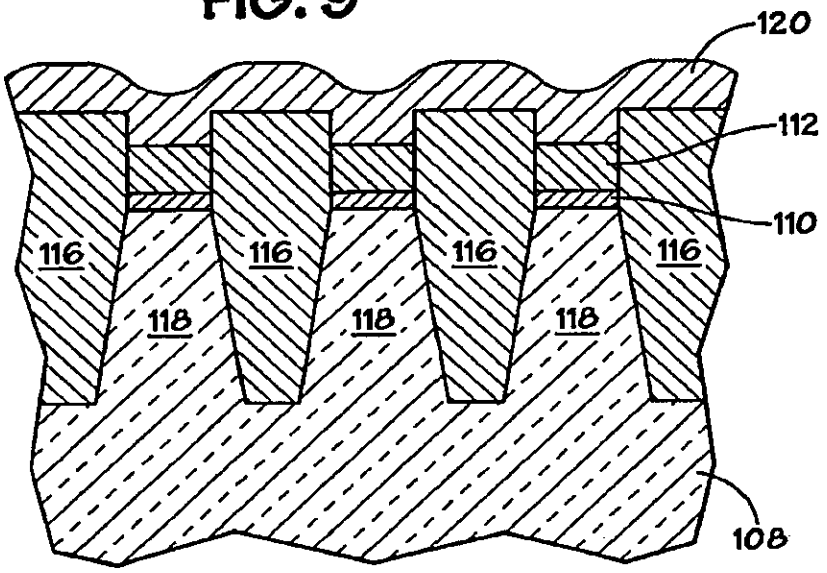




FIG. 8

FIG. 9


120
112
110
116
116
116
116
118
118
118
108

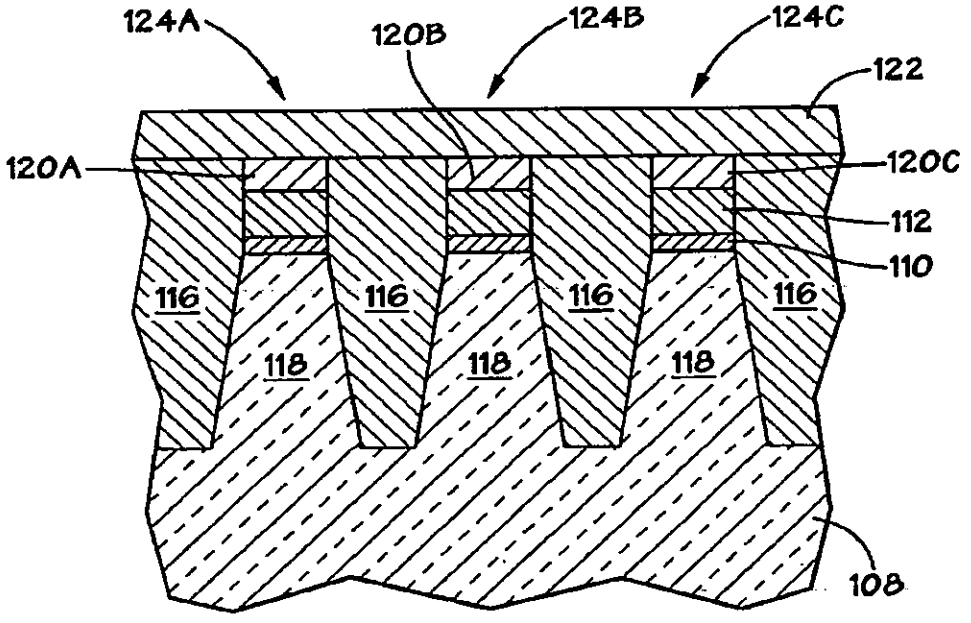

124A
120B
124B
124C
122
120A
120C
112
110
116
116
116
116
118
118
118
108

FIG. 10

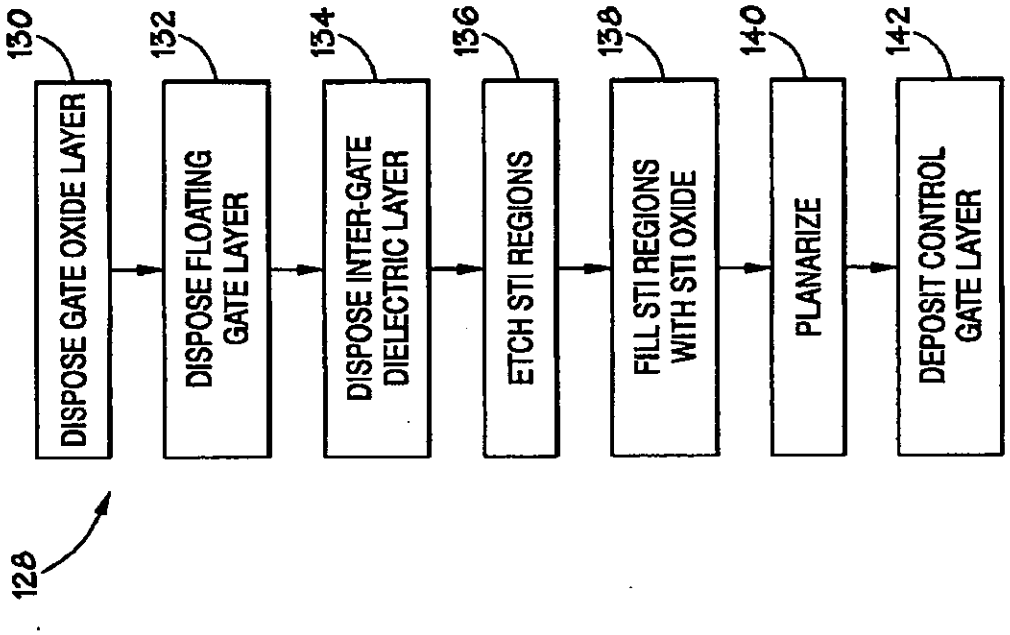

130
DISPOSE GATE OXIDE LAYER
132
DISPOSE FLOATING GATE LAYER
134
DISPOSE INTER-GATE DIELECTRIC LAYER
136
ETCH STI REGIONS
138
FILL STI REGIONS WITH STI OXIDE
140
PLANARIZE
142
DEPOSIT CONTROL GATE LAYER
128

FIG. 12

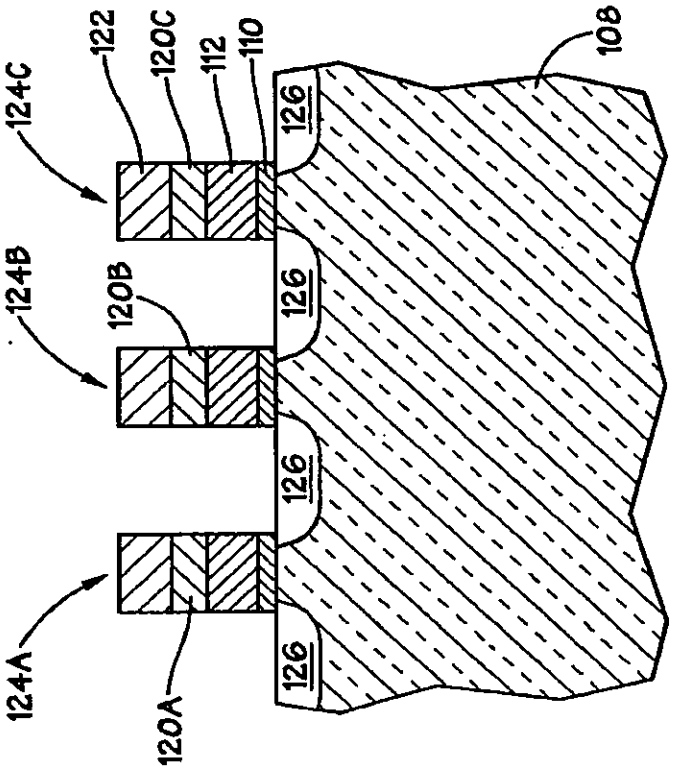

124C
124B
124A
122
120C
112
110
120B
120A
126
126
126
126
108

FIG. 11