ABSTRACT

SELF-ALGINED CONTACT PROCESS USING A POLY-CAP MASK

A method for integrating salicide and self-aligned contact processes in the fabrication of logic circuits with embedded memory is described. Isolation areas are formed on a semiconductor substrate surrounding and electrically isolating device areas. Gate electrodes and associated source and drain regions are formed on and in the semiconductor substrate wherein the gate electrodes have silicon nitride sidewall spacers. A metal silicide layer is formed on the top surface of the gate electrodes and on the top surface of the semiconductor substrate overlying the source and drain regions associated with the gate electrodes using a salicide process. A poly-cap layer is deposited overlying the substrate. The poly-cap layer is selectively removed overlying one of the salicided source and drain regions where a self-aligned contact is to be formed, and overlying another of the salicided source and drain regions and a portion of its associated salicided gate electrode where a butted contact is to be formed. An insulating layer is deposited over the surface of the semiconductor substrate. The insulating layer is etched through to form simultaneously the planned self-aligned contact opening and the planned butted contact opening. The self-aligned contact opening and the butted contact opening are filled with a conducting layer to complete fabrication of the integrated circuit device.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)