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(54) Title: SYSTEM FOR CONCURRENT TEST OF SEMICONDUCTOR DEVICES

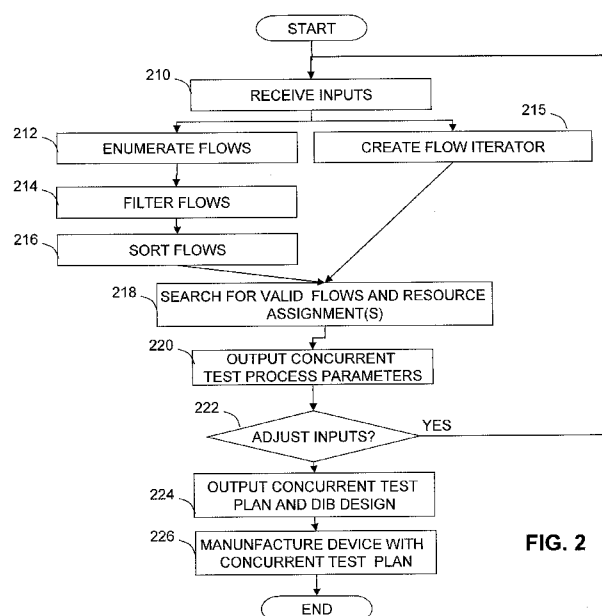


FIG. 2

(57) Abstract: A tool to aid a test engineer in creating a concurrent test plan. The tool may quickly map test system resources to specific pins to satisfy the requirements of a concurrent test. The tool may project test time when such a mapping is possible. When a mapping is not possible, the tool may inform its user, including making suggestions of additional resources that could allow the test system to perform the test or suggestions for other variations in input parameters that would allow a mapping. The tool employs an assignment process in which groups of associated pins are identified, along with associated resource requirements for each group. Groups of test system resources that collectively fulfill a higher level requirement are identified and the assignment is made by mapping resource sets to resource groups, using ordering and matching heuristics to reduce processing time.