CLAIMS

1. A silicon on insulator (SOI) structure, comprising:

an RF-SOI substrate, the RF-SOI substrate comprising

a high resistivity silicon (HR-Si) substrate;

a trap-rich layer overlying the HR-Si substrate;

a buried oxide (BOX) layer overlying the trap-rich layer; and

a thin silicon layer overlying the BOX layer;

a first circuit formed in a first silicon region of the thin silicon layer; and

a first implant in a region of the trap-rich layer that is immediately below the first circuit,

wherein

the first implant is configured to be biased with a first voltage that is based on an operating state of the first circuit,

the SOI structure further comprises a second implant in a region of the trap-rich layer that surrounds the first implant, and

an interface between the first implant and the second implant forms a first junction that is fully contained in the trap-rich layer and separated from the HR-Si substrate by an undoped region of the trap-rich layer.

2. The silicon on insulator (SOI) structure of claim 1, wherein:

the first junction is a p-n junction.

3. The silicon on insulator (SOI) structure of claim 1, wherein:

the first implant is formed in a well of the second implant.

4. The silicon on insulator (SOI) structure of claim 1, wherein:

the SOI structure further comprises a second through box contact (TBC), and

the second TBC penetrates the BOX layer at a second shallow trench isolation (STI) region to contact the second implant.

5. The silicon on insulator (SOI) structure of claim 4, wherein:

the SOI structure further comprises a first through box contact (TBC),

the first TBC penetrates the BOX layer at a first shallow trench isolation (STI) region to contact the first implant, the first TBC contacts the first implant for biasing of the first implant with the first voltage, and

the second STI region is the first STI region.

6. The silicon on insulator (SOI) structure of claim 4, wherein:

the second TBC resistively contacts the second implant for biasing of the second implant with a second voltage.

7. A silicon on insulator (SOI) structure, comprising:

an RF-SOI substrate, the RF-SOI substrate comprising

a high resistivity silicon (HR-Si) substrate;

a trap-rich layer overlying the HR-Si substrate;

a buried oxide (BOX) layer overlying the trap-rich layer; and

a thin silicon layer overlying the BOX layer;

a first circuit formed in a first silicon region of the thin silicon layer;

a first implant in a region of the trap-rich layer that is immediately below the first circuit; and

a second implant in a region of the trap-rich layer that surrounds the first implant,

wherein

the first implant is configured to be biased with a first voltage that is based on an operating state of the first circuit,

the SOI structure further comprises

a second circuit formed in a second silicon region of the thin silicon layer, the second silicon region isolated from the first silicon region; and

a third implant in a region of the trap-rich layer that is immediately below the second circuit, the third implant separated from the first implant by an undoped region of the trap-rich layer, and

the third implant is configured to be biased with a third voltage that is based on an operating state of the second circuit,

the SOI structure further comprises a fourth implant in a region of the trap-rich layer that surrounds the third implant,

an interface between the first implant and the second implant forms a first junction, and

an interface between the third implant and the fourth implant forms a second junction.

8. The silicon on insulator (SOI) structure of claim 7, wherein:

the first junction and the second junction are

separated from one another by an undoped region of the trap-rich layer, and

separated from the HR-Si by an undoped region of the trap-rich layer.

9. The silicon on insulator (SOI) structure of claim 7, wherein:

the first junction and the second junction form back-to-back reversed diodes that are configured to reduce flow of charges between the first and third implants.