[0004] Implementations of the devices can include one or more of the following features. For example, in some implementations, the first interconnect pad includes aluminum.

[0005] In some implementations, the barrier layer includes titanium nitride.

[0006] In some implementations, the superconducting bump bond includes indium.

[0007] In some implementations, the first circuit element includes a rapid single flux quantum (RSFQ) device.

[0008] In some implementations, the first circuit element includes a second quantum circuit element.

[0009] In some implementations, at least one of the first chip and the second chip includes a silicon substrate.

[0010] In some implementations, at least one of the first chip and the second chip includes a sapphire substrate.

[0011] In some implementations, a first surface of the first chip is spaced apart from and faces a first surface of the second chip to form a gap, and a thickness of the gap between the first surface of the first chip and the first surface of the second chip is between about 5 microns (5 micrometers) to about 10 microns (10 micrometers).

[0012] In some implementations, a first surface of the first chip is spaced apart from and faces a first surface of the second chip to form a gap, and a thickness of the gap between the first surface of the first chip and the first surface of the second chip is about 1 micron (1 micrometer).

[0013] In another aspect, the subject matter of the present disclosure can be embodied in methods that include: providing a first chip including a first circuit element; forming a first aluminum interconnect pad on a first surface of the first chip so that the first aluminum interconnect pad is electrically connected to the first circuit element; forming a first titanium nitride barrier layer on the first aluminum interconnect pad; providing a second chip including a second circuit element; forming an indium bump bond; and bonding the first chip to the second chip with the indium bump bond so that the first circuit element is electrically connected to the second circuit element, in which bonding the first chip to the second chip is performed at room temperature.

[0040] In process 200, a first substrate 114 is provided (202). FIG. 3A is a schematic illustrating an example of the first substrate 114. The first substrate 114 can include, for example, a single crystalline silicon wafer in which one or more circuit elements 112 are formed. Alternatively, the substrate 114 and circuit elements 112 can correspond to a die obtained from a wafer that has been diced. As explained herein, the circuit elements 112 can include quantum circuit elements or classical circuit elements. For the present example, it is assumed that the circuit elements 112 are classical circuit elements and the substrate 114 is a single crystalline silicon substrate. The circuit elements 112 can be electrically connected to one or more interconnect pads 116 through interconnects 118. The interconnects 118 can be formed, e.g., from a superconducting material or other electrically conductive material through a combination of photolithography to define openings within the substrate 114, as well as deposition and removal techniques, such as vapor deposition and wet or dry etching, to fill the opening with the interconnect material. Though shown being formed in the body of the substrate 114, the interconnects 118 can be formed on a surface of the substrate 114 instead. The interconnect pads 116 can be formed, e.g., from aluminum or another material that is superconducting. The interconnect pads 116 can also be deposited and defined using a combination of photolithography, and standard deposition and wet or dry etching techniques.

[0041] Next, the surfaces of the interconnect pads 116 are prepared (204). In some implementations, the metal interconnect pads, have a thin native oxide layer on their surface. For instance, aluminum can have a layer of AlO_x. The thin native oxide layer is insulating, reducing the electrical conductivity of the connection to the superconducting bump bond. To remove the native oxide, the surface of the interconnect pad 116 is exposed to an ion milling process. Ion milling includes delivering ions (e.g., Ar ions) to the surface of the interconnect pads 116 from an angle, such that material is sputtered from the surface. Typically, the ion milling process is performed under vacuum conditions. For instance, the ion milling can be performed under a vacuum pressure of 3 mTorr (0.39997 Pa) and temperature of about 28 °C.

[0042] Once the native oxide is removed, a barrier layer 120 is deposited on the prepared surfaces of the interconnect pads 116 (206). The barrier layer includes a material that blocks diffusion of the bump bond material into the interconnect pad 116

and/or vice-versa, but also retains superconductivity. The barrier layer also preferably does not form an alloy itself with either the interconnect pad 116 or the superconducting bump bond to be formed. To reduce decoherence that might be induced in nearby quantum circuit elements by the barrier layer, the barrier layer material may be formed from a superconductor material. For example, the barrier layer material can be formed from titanium nitride (having a superconducting critical temperature of about 4.2 K). Alternatively, the barrier layer material can include a metal that becomes superconducting via the proximity effect, such as platinum or tungsten. Deposition of the barrier layer can include, e.g., performing reactive sputtering. Reactive Sputtering is a process where a target of one chemical composition is sputtered in the presence of a gas or a mixture of gasses (e.g., Ar ions or N_2) that will react with the target material to form a coating of a different chemical composition. Argon is in most cases the main gas and the amount of a reactive gas introduced into a process chamber is controlled to produce a fully reacted compound. As an example, reactive sputtering can be performed using a mixture of Ar and N_2 under a base pressure of about $2*10^{-8}$ Torr (0.0000026665 Pa) and a background pressure of about 3 mTorr (0.39997 Pa) and temperature of about 28 °C. After deposition of the barrier layer material, the barrier layer material may be patterned so as to just cover the surfaces of the interconnect pads 116, and thus form layers 120 as shown in FIG. 3B. Patterning of the barrier layer material can entail using, e.g., photolithography to define the regions where the barrier layer material will remain followed by wet and/or dry etching of the barrier layer material in areas where the barrier layer material is to be removed. Alternatively, a lift-off process can be used, where the barrier layer material is deposited over a layer of patterned photoresist. In regions where the barrier layer material is to be removed, a solvent then is used to effectively "lift-off" the photoresist and barrier layer material coating. In either case, following patterning of the barrier layer material, the chip is exposed to an O_2 plasma to remove any remaining photoresist and/or other organic materials that may be on the surfaces of the chip.

[0043] After deposition and patterning of the barrier layer, the exposed surfaces of the barrier layers 120 can be optionally ion milled (208). Milling removes traces of native oxide on the barrier layer to increase conductivity and the reliability of the ensuing superconducting joint. Subsequently, a layer of superconducting material that

will form the superconducting bump bonds is deposited on the surface of the barrier layers (210). For instance, the superconducting material that will form the bump bonds can include indium (superconducting critical temperature of about 3.4 K). The superconducting material can be deposited using, e.g., a thermal evaporation deposition process under vacuum (e.g., at about $1*10^{-6}$ Torr (0.00013332 Pa)). As with the barrier layer 120, the as-deposited superconducting material 106 may be patterned using a combination of photolithography and wet or dry etching techniques to define the bump bond region 106 as shown in FIG. 3C. Alternatively, the superconducting material that will form the bump bonds is patterned using a lift-off process, in which, prior to deposition of the superconductor bump bond material, a photoresist layer is deposited and patterned. Then, following deposition of the superconductor bump bond material, the resist and undesired superconductor material overlaying the resist are removed using a solvent.

[0044] As shown in the example of FIG. 3D, an additional substrate 110 is provided (212). The additional substrate 110 can also include multiple circuit elements 108. As explained herein, the circuit elements 108 can include quantum circuit elements, such as qubits, for example, superconducting co-planar waveguides, quantum LC oscillators, flux qubits, or SQUIDS, among others. The substrate 110 can be formed from a low-loss dielectric material, such as sapphire or single crystalline silicon, and can be in the form of a wafer or a diced chip. One or more of the circuit elements 108 can be electrically connected to one or more interconnect pads 116 through interconnects 118 that are formed within or on the substrate 110. To reduce decoherence, the interconnects 118 and interconnect pads 116 are formed from a superconducting material, such as aluminum.

[0045] The same process for preparing the interconnect pads 116 and forming a barrier layer 120, as described above with respect to FIGS. 3B-3C, can also be performed on the additional substrate. For instance, the surfaces of the interconnect pads 116 can be prepared using, e.g., ion-milling, a superconducting diffusion barrier 120 is deposited and patterned on the prepared surfaces of the interconnect pads 116, the exposed surfaces of the barrier layer can be further ion-milled. Additionally, a layer of superconducting material that will form the superconducting bump bonds can be optionally deposited on the surface of the barrier layers. As explained herein, the superconducting material that will form the bump bonds can include, e.g., indium,

9. A method comprising:

providing a first chip comprising a first circuit element;

forming a first aluminum interconnect pad on a first surface of the first chip so that the first aluminum interconnect pad is electrically connected to the first circuit element;

forming a first titanium nitride barrier layer on the first aluminum interconnect pad;

providing a second chip comprising a second circuit element;

forming an indium bump bond; and

joining the first chip to the second chip with the indium bump bond so that the first circuit element is electrically connected to the second circuit element, wherein joining the first chip to the second chip is performed at room temperature.

10. The method of claim 9, wherein room temperature is between approximately 18 °C and approximately 30 °C.

11. The method of claim 10, further comprising removing a native oxide from the first aluminum interconnect pad prior to forming the first titanium nitride barrier layer.

12. The method of claim 11, wherein removing the native oxide comprises ion milling a surface of the first aluminum interconnect pad.

13. The method of claim 10, wherein forming the first titanium nitride barrier comprises reactive sputtering titanium nitride on the first aluminum interconnect pad.

14. The method of claim 10, further comprising ion milling a surface of the first titanium nitride barrier layer prior to joining the first chip to the second chip.

15. The method of claim 10, further comprising exposing a surface of the indium bump bond to a H_2 plasma.

16. The method of claim 10, further comprising:

forming a second aluminum interconnect pad on a first surface of the second chip so that the second aluminum interconnect pad is electrically connected to the second circuit element; and

forming a second titanium nitride barrier layer on the second aluminum interconnect pad of the second chip.

17. The method of claim 16, further comprising removing a native oxide from the second aluminum interconnect pad of the second chip prior to forming the second titanium nitride barrier layer.

18. The method of claim 17, wherein removing the native oxide from the second aluminum interconnect pad comprises ion milling a surface of the second aluminum interconnect pad.

19. The method of claim 16, wherein forming the second titanium nitride barrier layer on the second aluminum interconnect pad comprises reactive sputtering titanium nitride on the second aluminum interconnect pad.

20. The method of claim 16, further comprising ion milling a surface of the second titanium nitride barrier layer prior to joining the first chip to the second chip.

21. The method of claim 16, wherein forming the indium bump bond comprises depositing indium on the first titanium nitride barrier, on the second titanium nitride barrier, or on both the first and second titanium nitride barriers.

22. The method of claim 10, wherein the first circuit element comprises a rapid single flux quantum (RSFQ) device and the second circuit element comprises a quantum circuit element.

23. The method of claim 10, wherein the first circuit element comprises first quantum circuit element and the second circuit element comprises a second quantum circuit element.