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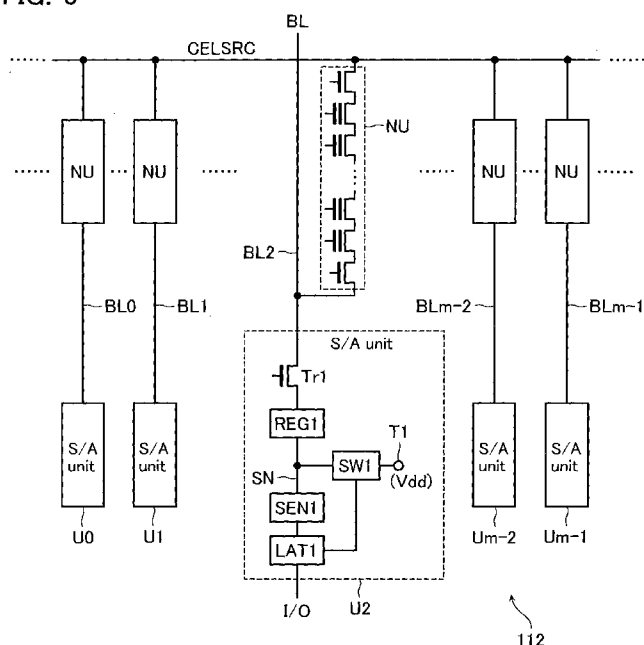
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(54) Title: NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND READ METHOD THEREOF

FIG. 5



(57) Abstract: This nonvolatile semiconductor memory device comprises a memory cell array configured having a plurality of NAND cell units arranged therein, each of the NAND cell units being configured having a plurality of memory cells connected in series therein. A bit line is connected to one end of the NAND cell unit, and a source line is connected to the other end of the NAND cell unit. A sense amplifier circuit is connected to the bit line. The sense amplifier circuit comprises: a first switch circuit connected between a power supply voltage terminal and a sense node; a sense amplifier connected to the sense node; and a latch circuit that latches a signal outputted from the sense amplifier. The first switch circuit is configured to switch to a non-conductive state according to data latched by the latch circuit.