Description

The present invention relates generally to methods of making integrated circuit memories, and more specifically to methods of making memory cells for dynamic random access memory devices.

Dynamic random access memory (DRAMs) are widely used in the electronic industry. DRAM memory cells typically use a field effect transistor as a pass gate, and a capacitor as a storage node. The current state of the DRAM cell is represented by the presence or absence of charge on the storage node. The quality of a DRAM cell is strongly effected by the size of the capacitor. A smaller capacitance for the storage node results in lower signal-to-noise ratios since a smaller charge can be stored on the capacitor. Smaller capacitors also require shorter refresh times for the DRAM cells.

As memory capacities increase, the density of memory cells on an integrated circuit increases and each cell must be made smaller. As cell sizes shrink, problems with small capacitors become more difficult to deal with during cell design. Efforts have been made to improve the capacitance of the storage node by increasing the capacitor plate surface area using a number of techniques. These include the placement of transistors in relatively deep trenches, or pits, excavated from the substrate, and placing capacitors on the sides of vertical pillars. The processing technologies used to fabricate such structures are relatively difficult to control, resulting in a large variability in device properties. In addition, they tend to increase the complexity of the process flow, adding to device cost.

It would be desirable to provide a capacitor suitable for DRAM cells which has an increased capacitance. It would be further desirable to provide such a capacitor which does not greatly increase the overall cell size and which does not add greatly to the complexity of integrated circuit processing.

JP-A-1154551 discloses a semiconductor storage integrated circuit device and a method of manufacturing such a device. By forming a first plate electrode and a first dielectric film on the lower surface of a charge storing electrode of a stacked capacitor and providing a second dielectric film and a second plate electrode on the charge storing electrode the size of the semiconductor storage integrated circuit device is minimised.

JP-A-1022057 discloses a method of manufacturing a multi-layer planar type capacitor having a high degree of integration. This high degree of integration is achieved by stacking polysilicon capacitor plates to increase the area of the capacitor plate.

JP-A-64000756 discloses a semiconductor device incorporating a capacitor device and method of manufacturing a capacitor device having a highly reliable capacitor insulating film. Reliability is achieved by providing a silicon oxide-silicon nitride-silicon oxide insulating film.

US-A-4700457 discloses a semiconductor device comprising a capacitor of a laminated structure and a method of manufacturing thereof, in which first conductive layer and second conductive layer of different materials or different compositions are stacked alternately with dielectric films interposed therebetween and the first conductive layers and the second conductive layers are interconnected respectively.

It is an object of the present invention to provide a capacitor suitable for use with DRAM cells which has an increased capacitance.

It is a further object of the present invention to provide such a capacitor which provides an increased capacitor plate area without increasing the layout area for a DRAM cell.

It is another object of the present invention to provide such a capacitor which uses relatively simple and repeatable process steps, and which is compatible with current N-channel DRAM process flows.

It is yet another object of the present invention to provide such a capacitor which can be fabricated without greatly increasing process complexity and cost.

The present invention provides a method for forming an integrated circuit capacitor on a semiconductor substrate, comprising the steps of:

forming a first insulating layer over the substrate;

forming a polycrystalline silicon lower capacitor plate over the first insulating layer;

forming a second insulating layer over the lower capacitor plate;

forming a polycrystalline silicon buffer layer over the second insulating layer;

forming an opening through the polycrystalline silicon lower capacitor plate and buffer layer and through the first and second insulating layers to expose a selected region of the substrate;

forming sidewall insulating regions in the opening;

forming a polycrystalline silicon charge storage plate over the buffer layer and in the opening, wherein contact is made to the selected region of the substrate;

forming a third insulating layer over the charge storage plate; and

forming a polycrystalline silicon top capacitor plate over the third insulating layer and in contact with the lower capacitor plate.

The features believed characteristic of the invention are set forth in the appended claims. The invention, as well as a preferred mode of use, and further objects and advantages thereof, will best be understood by reference to the following detailed description of an illustratrive embodiment when read in conjunction with the accompanying drawings, wherein:

Figures 1-7 illustrate a preferred process flow for fabricating a capacitor according to the method of the

present invention.

The process steps and structures described below do not form a complete process flow for manufacturing integrated circuits. The present invention can be practiced in conjunction with integrated circuit fabrication techniques currently used in the art, and only so much of the commonly practiced process steps are included as are necessary for an understanding of the present invention The figures representing cross-sections of portions of an integrated circuit during fabrication are not drawn to scale, but instead are drawn so as to illustrate the important features of the invention.

Referring to **Figure 1**, a process is shown for fabricating a capacitor according to the present invention for utilization with N-channel DRAM cells. A DRAM cell is fabricated in a P-type substrate **10**. As known in the art, a field effect transistor pass gate is formed by forming a thin gate oxide layer **12** followed by a gate polycrystalline silicon layer **14**. Polycrystalline silicon layer **14** may include a silicide layer, such as titanium or tantalum disilicide, to improve conductivity as known in the art. The pass gates, comprising polycrystalline silicon layer **14** and gate oxide layer **12**, are then patterned, followed by a lightly-doped drain (LDD) implant to form LDD regions **16, 18**. Sidewall oxide spacer regions **20** are then formed, followed by a heavy implant to form an active source/drain region **22**. To this point, processing has followed the usual steps known in the art.

Next, a dielectric layer **24**, preferably a low temperature oxide deposited to a depth of approximately 2,000Å, is deposited over the surface of the chip. This is followed by a second layer of polycrystalline silicon **26**, preferably deposited to a depth of approximately 1,500Å, which is then doped N-type by implant. A thin dielectric layer **28** is then formed over the surface of the chip.

Layer **28** is preferably an oxide-nitride-oxide layer as known in the art. Other dielectric layers, such as nitride-oxide, may be used if desired. This layer may be formed by growing an oxide layer on the polycrystalline silicon layer **26**, followed by deposition of a thin nitride layer. Further oxidation of the nitride layer forms an upper oxide layer, giving the desired oxide-nitride-oxide sandwich. This form of dielectric is preferred because it allows a thinner dielectric to be formed, and has a higher dielectric constant than oxide alone. Also, the oxide-nitride-oxide dielectric has a lower pinhole density than a thin oxide alone.

After formation of dielectric layer **28**, another polycrystalline silicon layer 30 is deposited over the surface of the chip. This layer **30** is used as a buffer layer, and will be partially incorporated into the storage node of the cell capacitor.

Referring to **Figure 2**, the next step is to pattern and etch a contact opening **32**. This opening is located near the pass gate **14**, and is shown in **Figure 2** as being located approximately half way between such feature and field oxide region **34**. Contact opening **32** is formed by an anisotropic etch through all of the layers **30, 28, 26, 24** to open up region **18** within the substrate **10**.

Next, the chip is oxidized to grow an oxide layer **36** on all exposed surfaces. **Figure 3** shows details of the oxide layer **36** as grown along one sidewall of contact opening **32**. Insulating layer **28** is comprised of oxide layer **38**, nitride layer **40**, and oxide layer **42**. As shown in **Figure 3**, formation of oxide layer **36** results in formation of a small bird's beak **44** between polycrystalline silicon layer **30** and nitride layer **40**, and another bird's beak **46** between nitride layer **40** and polycrystalline silicon layer **26**. The effect of these bird's beaks **44, 46** is to separate the polycrystalline layers **26,30** at their edges, where electric fields are generally most intense.

If the high temperature oxide growth step is not desired, a lower temperature CVD oxide can be grown instead. Although the bird's beak formations are not grown, an adequate insulative layer is still provided.

Referring to **Figure 4**, the oxide layer **36** is anisotropically etched to form sidewall dielectric regions **48** along the sides of contact opening **32**. This etch removes all of the oxide layer **36** from over polycrystalline silicon buffer layer **30**. A third polycrystalline silicon layer **50** is then grown over the surface of the chip, making contact with active region **18** within the contact opening **32**. Third polycrystalline silicon layer **50** and buffer layer **30** are now the same layer functionally. A partial dielectric layer **52** is then formed over the surface of the chip. Layer **52** consists of a thin grown oxide layer, followed by a deposited nitride layer. These are the first two layers of an oxide-nitride-oxide dielectric sandwich formed as illustrated in **Figure 3**, but the upper oxide layer is not yet formed.

Referring to **Figure 5**, the chip is then patterned and etched to define the charged storage plate of the capacitor. Regions **54** and **56** are etched down to polycrystalline silicon layer **26** using an anisotropic etch. Region **54** will be used later to make contact with the active region **22**. Following the etch, an oxidation step is performed which converts layer **52** into an oxide-nitride-oxide dielectric, and grows an oxide layer **58** over the remaining surfaces of the chip. This includes a growth of oxide on the sidewalls of etched regions **54** and **56**. The sidewalls of such regions are very similar to the sidewall regions shown in **Figure 3**, with small bird's beaks being formed on either side of the middle nitride layer in dielectric sandwich layers **28** and **52**. As described in connection with **Figure 3**, a CVD oxide can be deposited instead of growing a thermal oxide.

Referring to **Figure 6**, the newly grown oxide layer is anisotropically etched to form sidewall dielectric regions **60** along side openings **54** and **56**. These di-

electric regions **60**, as described above, are similar to sidewall regions **48** within contact opening **32**. In the alternative, a mask can be used to define openings in the oxide layer **58** to allow contact to be made with polycrystalline layer **26**. A fourth layer of polycrystalline silicon **62** is grown over the surface of the chip, and doped N-type. Layer **62** makes contact with layer **26**. Region **64** is then anisotropically etched, using a mask, through polycrystalline silicon layers **62** and **26**, to expose oxide layer **24**. A corresponding etch region (not shown) is made just beyond the right edge of the drawing of **Figure 6**.

At this point, the capacitor has been entirely defined. Polycrystalline silicon layer **26** defines the bottom ground plate of the capacitor, and polycrystalline silicon layer **62** defines the top ground plate of the capacitor. The charge storage plate of the capacitor is formed by polycrystalline silicon layers **30** and **50**, and makes contact with active region **18**. The charge storage plate is completely separated from the upper and lower capacitor ground plates by dielectric regions **52** and **28**, and sidewall regions **48** and **60**, and is in contact with layer **18**.

Referring to **Figure 7**, after definition of the capacitor a dielectric layer **66** is formed over the surface of the chip. This dielectric layer **66** is preferably a reflow glass, such as PSG or BPSG. Contact opening **68** is then formed through glass layer **66** and oxide layer **24** to make contact with active region **22**. Metal layer **70** is then deposited and patterned on the surface of the chip. As known in the art, deposition of metal layer **70** can include an aluminum layer with one or more refractory metal layers.

High temperature oxide growth and deposition steps cause a diffusion of the N-type impurity from polycrystalline silicon layer **50** into the active region **18**. Since region **18** and diffused region **72** are both N-type, no shorting or undesired junctions are formed in this area.

Using the method described above, a capacitor has been formed which has ground plates above and below a charge storage capacitor plate. This approximately doubles the capacitance of the charge storage node without increasing the overall area of the DRAM cell. Although multiple polycrystalline silicon layers are formed, no complex processing steps, such as thin film deposition on the sidewalls of a trench or pillar, are required.

In addition to increasing the capacitance of the DRAM cell without increasing its area, the charge storage node is surrounded by upper and lower capacitor plates. These upper and lower capacitor plates are grounded, which provides improved electrical isolation for the charge storage node. The DRAM cell is thus less vulnerable to being influenced by changing signals on the word and bit lines of the device.

While the invention has been particularly shown and described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the scope of the invention as defined by the appended claims.

Claims

1. A method for forming an integrated circuit capacitor on a semiconductor substrate, comprising the steps of:

   forming a first insulating layer (24) over the substrate (10);

   forming a polycrystalline silicon lower capacitor plate (26) over the first insulating layer (24);

   forming a second insulating layer (28) over the lower capacitor plate (26);

   forming a polycrystalline silicon buffer layer (30) over the second insulating layer (28);

   forming an opening (32) through the polycrystalline silicon lower capacitor plate (26) and buffer layer (30) and through the first (24) and second (28) insulating layers to expose a selected region of the substrate (10);

   forming sidewall insulating regions (48) in the opening (32);

   forming a polycrystalline silicon charge storage plate (50) over the buffer layer (30) and in the opening (32), wherein contact is made to the selected region of the substrate (10);

   forming a third insulating layer (52) over the charge storage plate (50); and

   forming a polycrystalline silicon top capacitor plate (62) over the third insulating layer (52) and in contact with the lower capacitor plate (26).

2. The method of claim 1, wherein said step of forming sidewall insulating regions (48) in the opening (32) comprises:

   forming an insulating layer (36) over the buffer layer (30) and in the opening (32); and

   anisotropically etching the insulating layer (36) to form insulating sidewalls (48) within the contact opening (32).

3. The method of claim 2, wherein said insulating layer forming step comprises the step of:

   growing a thermal oxide over the buffer layer (30) and in the opening (32).

4. The method of claim 2, wherein said insulating layer forming step comprises the step of:

   depositing a CVD oxide over the buffer layer (30) and in the opening (32).

5. The method of any one of claims 1 to 4, wherein

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electric regions **60**, as described above, are similar to sidewall regions **48** within contact opening **32**. In the alternative, a mask can be used to define openings in the oxide layer **58** to allow contact to be made with polycrystalline layer **26**. A fourth layer of polycrystalline silicon **62** is grown over the surface of the chip, and doped N-type. Layer **62** makes contact with layer **26**. Region **64** is then anisotropically etched, using a mask, through polycrystalline silicon layers **62** and **26**, to expose oxide layer **24**. A corresponding etch region (not shown) is made just beyond the right edge of the drawing of **Figure 6**.

At this point, the capacitor has been entirely defined. Polycrystalline silicon layer **26** defines the bottom ground plate of the capacitor, and polycrystalline silicon layer **62** defines the top ground plate of the capacitor. The charge storage plate of the capacitor is formed by polycrystalline silicon layers **30** and **50**, and makes contact with active region **18**. The charge storage plate is completely separated from the upper and lower capacitor ground plates by dielectric regions **52** and **28**, and sidewall regions **48** and **60**, and is in contact with layer **18**.

Referring to **Figure 7**, after definition of the capacitor a dielectric layer **66** is formed over the surface of the chip. This dielectric layer **66** is preferably a reflow glass, such as PSG or BPSG. Contact opening **68** is then formed through glass layer **66** and oxide layer **24** to make contact with active region **22**. Metal layer **70** is then deposited and patterned on the surface of the chip. As known in the art, deposition of metal layer **70** can include an aluminum layer with one or more refractory metal layers.

High temperature oxide growth and deposition steps cause a diffusion of the N-type impurity from polycrystalline silicon layer **50** into the active region **18**. Since region **18** and diffused region **72** are both N-type, no shorting or undesired junctions are formed in this area.

Using the method described above, a capacitor has been formed which has ground plates above and below a charge storage capacitor plate. This approximately doubles the capacitance of the charge storage node without increasing the overall area of the DRAM cell. Although multiple polycrystalline silicon layers are formed, no complex processing steps, such as thin film deposition on the sidewalls of a trench or pillar, are required.

In addition to increasing the capacitance of the DRAM cell without increasing its area, the charge storage node is surrounded by upper and lower capacitor plates. These upper and lower capacitor plates are grounded, which provides improved electrical isolation for the charge storage node. The DRAM cell is thus less vulnerable to being influenced by changing signals on the word and bit lines of the device.

While the invention has been particularly shown and described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the scope of the invention as defined by the appended claims.

Claims

1. A method for forming an integrated circuit capacitor on a semiconductor substrate, comprising the steps of:

   forming a first insulating layer (24) over the substrate (10);

   forming a polycrystalline silicon lower capacitor plate (26) over the first insulating layer (24);

   forming a second insulating layer (28) over the lower capacitor plate (26);

   forming a polycrystalline silicon buffer layer (30) over the second insulating layer (28);

   forming an opening (32) through the polycrystalline silicon lower capacitor plate (26) and buffer layer (30) and through the first (24) and second (28) insulating layers to expose a selected region of the substrate (10);

   forming sidewall insulating regions (48) in the opening (32);

   forming a polycrystalline silicon charge storage plate (50) over the buffer layer (30) and in the opening (32), wherein contact is made to the selected region of the substrate (10);

   forming a third insulating layer (52) over the charge storage plate (50); and

   forming a polycrystalline silicon top capacitor plate (62) over the third insulating layer (52) and in contact with the lower capacitor plate (26).

2. The method of claim 1, wherein said step of forming sidewall insulating regions (48) in the opening (32) comprises:

   forming an insulating layer (36) over the buffer layer (30) and in the opening (32); and

   anisotropically etching the insulating layer (36) to form insulating sidewalls (48) within the contact opening (32).

3. The method of claim 2, wherein said insulating layer forming step comprises the step of:

   growing a thermal oxide over the buffer layer (30) and in the opening (32).

4. The method of claim 2, wherein said insulating layer forming step comprises the step of:

   depositing a CVD oxide over the buffer layer (30) and in the opening (32).

5. The method of any one of claims 1 to 4, wherein

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said second insulating layer forming step comprises the steps of:

forming a first oxide layer (42) on the polysilicon lower capacitor plate (26);

forming a nitride layer (40) over the oxide layer (42); and

forming a second oxide layer (38) over the nitride layer (40).

6. The method of any one of claims 1 to 5, wherein said charge storage plate forming step comprises the steps of:

forming the polycrystalline silicon charge plate layer (50) over the buffer layer (30) and in the opening (32);

masking the storage plate layer (50) in the opening (32) and an adjacent area; and

etching the polycrystalline silicon charge storage layer (50), the polycrystalline silicon buffer layer (30), and the second insulator (28) to define the charge storage plate.

7. The method of any one of claims 1 to 6, wherein said third insulating layer forming step includes the step of forming insulating sides (60) of the charge storage plate (50) and buffer layers (30).

8. The method of claim 7, wherein said sidewall forming step comprises the steps of:

forming an insulating layer (52,58) over the charge storage node; and

anisotropically etching the insulating layer (58) to form sidewall insulating regions (60).

9. The method of claim 7, wherein said sidewall forming step comprises the steps of:

forming a first oxide layer over the polycrystalline silicon charge storage layer (50);

forming a nitride layer over the oxide layer;

patterning and etching the oxide layer, the nitride layer, and the charge storage (50) and buffer layers (30) to define the charge storage node; and

forming a second oxide layer (52,58) over the charge storage node.

10. The method of claim 9, further comprising the step of:

anisotropically etching the second oxide layer to form sidewall insulating regions (60) on the charge storage node.

Patentansprüche

1. Verfahren zum Herstellen eines integrierten Schaltungskondensators auf einem Halbleitersubstrat mit den folgenden Schritten:

über dem Substrat (10) wird eine erste Isolationsschicht (24) ausgebildet;

über der ersten Isolationsschicht (24) wird eine untere Kondensatorplatte (26) von polykristallinem Silicium ausgebildet;

über der unteren Kondensatorplatte (26) wird eine zweite Isolationsschicht (28) ausgebildet;

über der zweiten Isolationsschicht (28) wird eine Pufferschicht (30) aus polykristallinem Silicium ausgebildet;

eine Öffnung (32) wird durch das polykristalline Silicium der unteren Kondensatorplatte (26) und der Pufferschicht (30) und durch die erste (24) und zweite (28) Isolationsschicht gebildet, um einen ausgewählten Bereich des Substrats (10) freizulegen;

in der Öffnung (32) werden Seitenwandisolationsbereiche (48) ausgebildet;

eine Ladungsspeicherplatte (50) aus polykristallinem Silicium wird über der Pufferschicht (30) und in der Öffnung (32) ausgebildet, wobei ein Kontakt zu dem ausgewählten Bereich des Substrats (10) hergestellt wird;

über der Ladungsspeicherplatte (50) wird eine dritte Isolationsschicht (52) ausgebildet; und

über der dritten Isolationsschicht (52) und in Kontakt mit der unteren Kondensatorplatte (26) wird eine obere Kondensatorplatte (62) aus polykristallinem Silicium ausgebildet.

2. Verfahren nach Anspruch 1, in dem der Schritt des Ausbildens von Seitenwandisolationsbereichen (48) in der Öffnung (32) umfaßt:

über der Pufferschicht (30) und in der Öffnung (32) wird eine Isolationsschicht (36) ausgebildet; und

die Isolationsschicht (36) wird anisotrop geätzt, um isolierende Seitenwände (48) innerhalb der Kontaktöffnung (32) auszubilden.

3. Verfahren nach Anspruch 2, in dem der Schritt zur Ausbildung der Isolationsschicht den folgenden Schritt umfaßt:

ein thermisches Oxyd wird über der Pufferschicht (30) und in der Öffnung (32) aufgewachsen.

4. Verfahren nach Anspruch 2, in dem der Schritt zur Ausbildung der Isolationsschicht den folgenden Schritt umfaßt:

über der Pufferschicht (30) und in der Öffnung (32) wird ein CVD-Oxyd abgeschieden.

5. Verfahren nach einem der Ansprüche 1 bis 4, in dem der Schritt zur Ausbildung der zweiten Isolationsschicht folgende Schritte umfaßt:

auf der unteren Kondensatorplatte (26)

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aus Polysilicium wird eine erste Oxydschicht (42) ausgebildet;

über der Oxydschicht (42) wird eine Nitridschicht (40) ausgebildet; und

über der Nitridschicht (40) wird eine zweite Oxydschicht (38) ausgebildet.

6. Verfahren nach einem der Ansprüche 1 bis 5, in dem der Schritt zur Ausbildung der Ladungsspeicherplatte die folgenden Schritte umfaßt:

die Ladungsplattenschicht (50) aus polykristallinem Silicium wird über der Pufferschicht (30) und in der Öffnung (32) ausgebildet;

die Speicherplattenschicht (50) wird in der Öffnung (32) und einem benachbarten Bereich maskiert; und

die Ladungsspeicherschicht (50) aus polykristallinem Silicium, die Pufferschicht (30) aus polykristallinem Silicium und der zweite Isolator (28) werden geätzt, um die Ladungsspeicherplatte festzulegen.

7. Verfahren nach einem der Ansprüche 1 bis 6, in dem der Schritt zur Ausbildung der dritten Isolationsschicht den Schritt enthält, isolierende Seiten bzw. Kanten (60) der Ladungsspeicherplatte (50) und der Pufferschichten (30) auszubilden.

8. Verfahren nach Anspruch 7, in dem der Schritt zur Ausbildung der Seitenwand die folgenden Schritte umfaßt:

über dem Ladungsspeicher-Knoten bzw. Knotenpunkt wird eine Isolationsschicht (52, 58) ausgebildet; und

die Isolationsschicht (58) wird anisotrop geätzt, um isolierende Seitenwandbereiche (60) auszubilden.

9. Verfahren nach Anspruch 7, in dem der Schritt zur Ausbildung der Seitenwand die folgenden Schritte umfaßt:

eine erste Oxydschicht wird über der Ladungsspeicherschicht (50) aus polykristallinem Silicium ausgebildet;

über der Oxydschicht wird eine Nitridschicht ausgebildet;

die Oxydschicht, die Ladungsspeicher-(50) und Pufferschichten (30) werden mit einem Muster versehen und geätzt, um den Ladungsspeicher-Knotenpunkt festzulegen; und

über dem Ladungsspeicher-Knotenpunkt wird eine zweite Oxydschicht (52, 58) ausgebildet.

10. Verfahren nach Anspruch 9, das ferner folgenden Schritt umfaßt:

die zweite Oxydschicht wird anisotrop geätzt, um auf dem Ladungsspeicher-Knotenpunkt Seitenwandisolationsbereiche (60) auszubilden.

Revendications

1. Procédé pour former un condensateur de circuit intégré sur un substrat en semi-conducteur, comprenant les étapes consistant à :

former une première couche isolante (24) recouvrant le substrat (10) ;

former une armature inférieure de condensateur en silicium polycristallin (26) sur la première couche isolante (24) ;

former une deuxième couche isolante (28) sur l'armature inférieure de condensateur (26) ;

former une couche intermédiaire en silicium polycristallin (30) sur la deuxième couche isolante (28) ;

former une ouverture (32) à travers l'armature inférieure de condensateur en silicium polycristallin (26) et la couche intermédiaire (30) et à travers les première (24) et deuxième (28) couches isolantes pour exposer une zone sélectionnée du substrat (10) ;

former des zones isolantes de paroi latérale (48) dans l'ouverture (32) ;

former une armature de conservation de charge en silicium polycristallin (50) sur toute la couche intermédiaire (30) et dans l'ouverture (32), en établissant un contact avec la zone sélectionnée du substrat (10) ;

former une troisième couche isolante (52) sur l'armature de conservation de charge (50) ; et

former une armature supérieure de condensateur en silicium polycristallin (62) sur la troisième couche isolante (52) et en contact avec l'armature inférieure de condensateur (26).

2. Procédé selon la revendication 1, dans lequel ladite étape consistant à former des zones isolantes de paroi latérale (48) dans l'ouverture (32) comprend :

la formation d'une couche isolante (36) sur toute la couche intermédiaire (30) et dans l'ouverture (32) ; et

l'attaque anisotropique de la couche isolante (36) pour former des parois latérales isolantes (48) à l'intérieur de l'ouverture de contact (32).

3. Procédé selon la revendication 2, dans lequel ladite étape de formation de couche isolante comprend l'étape consistant à :

faire croître un oxyde thermique sur la couche intermédiaire (30) et dans l'ouverture (32).

4. Procédé selon la revendication 2, dans lequel ladite étape de formation de couche isolante

comprend l'étape consistant à :

déposer par dépôt chimique en phase vapeur un oxyde sur toute la couche intermédiaire (30) et dans l'ouverture (32).

5. Procédé selon l'une quelconque des revendications 1 à 4, dans lequel ladite étape de formation de ladite deuxième couche isolante comprend les étapes consistant à :

former une première couche d'oxyde (42) sur l'armature inférieure de condensateur en polysilicium (26) ;

former une couche de nitrure (40) sur toute la couche d'oxyde (42) ; et

former une deuxième couche d'oxyde (38) sur toute la couche de nitrure (40).

6. Procédé selon l'une quelconque des revendications 1 à 5, dans lequel ladite étape de formation d'armature de conservation de charge comprend les étapes consistant à :

former la couche d'armature de conservation de charge en silicium polycristallin (50) sur toute la couche intermédiaire (30) et dans l'ouverture (32) ;

masquer la couche d'armature de conservation de charge (50) dans l'ouverture (32) et dans une zone adjacente ; et

attaquer la couche d'armature de conservation de charge en silicium polycristallin (50), la couche intermédiaire en silicium polycristallin (30) et la deuxième couche isolante (28) pour définir l'armature de conservation de charge.

7. Procédé selon l'une quelconque des revendications 1 à 6, dans lequel ladite étape de formation de troisième couche isolante comprend l'étape consistant à former des parois latérales isolantes (60) autour de l'armature de conservation de charge (50) et des couches intermédiaires (30).

8. Procédé selon la revendication 7, dans lequel ladite étape de formation de parois latérales comprend les étapes consistant à :

former une couche isolante (52, 58) sur tout le point de conservation de charge ; et

attaquer de manière anisotropique la couche isolante (58) pour former des zones de paroi latérale isolantes (60).

9. Procédé selon la revendication 7, dans lequel ladite étape de formation de parois latérales comprend les étapes consistant à :

former une première couche d'oxyde sur toute la couche de conservation de charge en silicium polycristallin (50) ;

former une couche de nitrure sur toute la couche d'oxyde ;

conformer et attaquer la couche d'oxyde, la couche de nitrure et les couches intermédiaires (30) et de conservation de charge (50), pour définir le point de conservation de charge ; et

former une deuxième couche d'oxyde (52, 58) sur tout le point de conservation de charge.

10. Procédé selon la revendication 9, comprenant en outre l'étape consistant à :

attaquer de manière anisotropique, la deuxième couche d'oxyde pour former des zones de paroi latérale (60) isolantes sur le point de conservation de charge.