[06] In one exemplary embodiment of a semiconductor switch, the phase change material is used for the semiconducting channel where an ON state corresponds to the phase change material being in the metal phase and an OFF state corresponds to the phase change material being in the insulator phase. An externally controllable voltage differential applied across the semiconducting channel generates a field that controls the phase of the phase change material.

[06a] In an ~~first aspect~~embodiment, the present disclosure provides a semiconductor comprising: a semiconducting channel with first and second opposing ends and first and second opposing lateral sides, the semiconducting channel supporting the flow of current from the first end to the second end through the semiconducting channel while the semiconducting channel is in a metal phase; the semiconducting channel made of a phase change material of $Mo_xW_{1-x}Te_2$; the phase change material being in one of metal and insulator phases when no field exists due to no voltage differential across the first and second lateral sides and being in the other of metal and insulator phases when a field due a voltage differential greater than a phase change voltage differential exists across the first and second lateral sides, no substantial current flows from the first end to the second end while the semiconducting channel is in the insulator phase.

[07] In another ~~second aspect~~embodiment, the present disclosure provides a field effect transistor (FET) comprising a semiconducting channel with spaced apart source and drain regions on its surface; a dielectric layer disposed on the surface of the semiconducting channel between the source and drain regions, and a gate region disposed on an opposing surface of the dielectric layer, the gate region being disposed between the source and drain regions. The source, gate and drain regions each comprising $Mo_xW_{1-x}Te_2$ phase change material with metal contacts disposed on each to facilitate electrical connections with the source, gate and drain regions. An externally controllable voltage differential generates a field applied to at least some of the phase change materials to control the phase of the phase change material.

[07a] In an ~~third~~ aspect, the present disclosure provides a field effect transistor (FET) apparatus comprising: an FET device including: a semiconducting channel; spaced apart source and drain regions disposed on a surface of the semiconducting channel; a dielectric layer disposed on the surface of the semiconducting channel between the source and drain regions; a gate region disposed on a surface of the dielectric layer opposite the surface of the semiconducting channel and between the source and drain regions; the source, gate and drain regions each being a metallic region; a control region disposed on the surface of the dielectric layer between the gate region and the drain region, the control region not connected to the gate region, the control region comprising $Mo_xW_{1-x}Te_2$ phase change material which has a semiconductor phase and an insulator phase selectable based on whether a control voltage field, which is independent from a field produced by a voltage applied at the drain region, is or is not present across the control region; the control region in the semiconductor phase functioning as a shield to passivate traps at the surface of the semiconducting channel between the gate region and the drain region; the control region in the insulator phase enhancing high frequency response of the FET by not presenting a physically active region adjacent the gate region, the phase change material being changed from one of semiconductor and insulator phases to the other of semiconductor and insulator phases at room temperature dependent on whether a voltage differential greater than a predetermined phase change voltage exists across the phase change material.

[08] In a further exemplary embodiment, an FET includes an additional control terminal disposed between the gate and the drain where the additional control terminal is made of $Mo_xW_{1-x}Te_2$ phase change material. An externally controllable voltage differential generates a field applied to the phase change material to control the phase of the phase change material between metal and insulator phases. The additional control terminal in the semiconductor phase functioning as a shield to passivate traps at the surface of the semiconducting channel between the gate region and the drain region. The additional control terminal in the insulator phase enhances high frequency response of the FET by not presenting a physically active region adjacent the gate region.

Claims

1. A semiconductor comprising:

a semiconducting channel with first and second opposing ends and first and second opposing lateral sides, the semiconducting channel supporting the flow of current from the first end to the second end through the semiconducting channel while the semiconducting channel is in a metal phase;

the semiconducting channel made of a phase change material of $Mo_xW_{1-x}Te_2$;

the phase change material being in one of metal and insulator phases when no field exists due to no voltage differential across the first and second lateral sides and being in the other of metal and insulator phases when a field due a voltage differential greater than a phase change voltage differential exists across the first and second lateral sides, no substantial current flows from the first end to the second end while the semiconducting channel is in the insulator phase.

2. The semiconductor of claim 1 where the semiconductor functions as an ON/OFF switch, an ON state corresponding to the phase change material being in the metal phase and an OFF state corresponding to the phase change material being in the insulator phase.

3. The semiconductor of claim 1 further comprising:

a substrate that supports the semiconducting channel;

first and second metallic pads;

a first dielectric material disposed on the substrate and engaging the first lateral side, the first dielectric material separating the first metallic pad from the first lateral side;

a second dielectric material disposed on the second lateral side, the second dielectric material separating the second metallic pad from the second lateral side;

the first and second metallic pads forming a sandwich with the semiconducting channel and facilitating the application of the field across the semiconducting channel upon a voltage differential being established at the first metallic pad relative to the second metallic pad.

~~4. The semiconductor of claim 2 wherein a transition between ON and OFF states, that corresponds to a transition between semiconductor and insulator phases, progresses at a rate of greater than one decade of current flow for every 60 millivolts of voltage differential across the semiconducting channel.~~

~~5. The semiconductor of claim 4 wherein the transition between ON and OFF states progresses at a greater rate of current flow for each unit change of voltage differential across the semiconducting channel as compared to a conventional FET not using phase change material.~~

~~6. The semiconductor of claim 1 wherein the phase change material is changed from one of metal and insulator phases to the other of metal and insulator phases while the semiconducting channel remains at substantially room temperature.~~

~~7. A field effect transistor (FET) comprising:~~

~~a semiconducting channel;~~

~~spaced apart source and drain regions disposed on a surface of the semiconducting channel;~~

~~a dielectric layer disposed on the surface of the semiconducting channel between the source and drain regions;~~

~~a gate region disposed on a surface of the dielectric layer opposite the surface of the semiconducting channel, the gate region disposed between the source and drain regions;~~

~~the source, gate and drain regions each comprising $Mo_xW_{1-x}Te_2$ phase change material;~~

~~metal contacts disposed on each of the source, gate and drain regions to facilitate electrical connections with the source, gate and drain regions.~~

~~8. The FET of claim 7 wherein the x in the material composition formula is a positive number less than or equal to 1.0, the value of x differing for the material utilized~~

~~in the source and gate regions with the source region having a lower x value than the x value for the gate region.~~

~~9. The FET of claim 8 wherein the value of x in the material composition formula for the respective regions is as follows:~~

~~for the source region, $0.7 < x < 0.8$,~~

~~for the gate region, $0.9 < x < 1.0$,~~

~~for the drain region, $0.9 < x < 1.0$.~~

~~10. The semiconductor of claim 7 wherein the phase change material is changed from one of metal and insulator phases to the other of metal and insulator phases at room temperature dependent on whether a voltage differential greater than a predetermined phase change voltage exists across the phase change material.~~

1~~1~~. A field effect transistor (FET) apparatus comprising:

an FET device including:

a semiconducting channel;

spaced apart source and drain regions disposed on a surface of the semiconducting channel;

a dielectric layer disposed on the surface of the semiconducting channel between the source and drain regions;

a gate region disposed on a surface of the dielectric layer opposite the surface of the semiconducting channel and between the source and drain regions;

the source, gate and drain regions each being a metallic region;

a control region disposed on the surface of the dielectric layer between the gate region and the drain region, the control region not connected to the gate region, the control region comprising $Mo_xW_{1-x}Te_2$ phase change material which has a semiconductor phase and an insulator phase selectable based on whether a control voltage field, which is independent from a field produced by a voltage applied at the drain region, is or is not present across the control region;

the control region in the semiconductor phase functioning as a shield to passivate traps at the surface of the semiconducting channel between the gate region and the drain region;

the control region in the insulator phase enhancing high frequency response of the FET by not presenting a physically active region adjacent the gate region.

the phase change material being changed from one of semiconductor and insulator phases to the other of semiconductor and insulator phases at room temperature dependent on whether a voltage differential greater than a predetermined phase change voltage exists across the phase change material.

~~1~~2. The FET apparatus of claim 1~~1~~ further comprising: ~~wherein the x in the material composition formula is a positive number less than or equal to 1.0, the value of x being between xx and yy~~

first and second voltage sources coupled to the first and second contacts, respectively, the first voltage source determining an operating voltage of the gate region to source region, the second voltage source providing a control voltage to the control region, one voltage of the second voltage source causing the control region to be in the semiconductor phase and another voltage of the second voltage source causing the control region to be in the insulator phase.

~~1~~3. The FET apparatus of claim ~~1~~1 wherein the gate region and the control region do not abut each other and are spaced apart.

~~1~~4. The FET apparatus of claim ~~1~~1 wherein the x in the material composition formula is a positive number less than or equal to 1.0, the value of x differing for the material utilized in the source and gate regions with the source region having a lower x value than the x value for the gate region ~~the gate region and the control region abut each other and are electrically connected to each other~~.

~~1~~5. The FET apparatus of claim 1~~1~~ wherein ~~the phase change material is changed from one of metal and insulator phases to the other of metal and insulator phases at room~~

~~temperature dependent on whether a voltage differential exists across the phase change material~~the value of x in the material composition formula for the respective regions is as follows:

for the source region, $0.7 < x < 0.8$,

for the gate region, $0.9 < x < 1.0$,

for the drain region, $0.9 < x < 1$.