

Abstract

This disclosure relates to a data transmission circuit and method, and a memory device. The circuit includes a data memory unit of a mode register and a data memory unit of an array region. The data memory unit of the mode register is configured to output data of the mode register in response to a first clock signal; an output terminal of the data memory unit of the array region and an output terminal of the data memory unit of the mode register are both connected to the first node, the data memory unit of the array region is configured to receive data of the array region in response to a first pointer signal, and to output the data of the array region in response to a second pointer signal. This disclosure can precisely control the data of the mode register and the data of the array region to output through a respective output channel in turn.

Cover use (FIG. 1)