

CHIP TRANSFER PROCESS

TECHNICAL FIELD

The invention relates to a process for transferring chips from a substrate, known as the pseudo-donor substrate, to a receiver substrate.

PRIOR ART

In the field of microelectronics, optics or optoelectronics, the design of multilayer structures sometimes requires the transfer of tiles that are in the form of portions of a layer, from a donor substrate to a support or receiver substrate.

This type of process is generally referred to as tiling, and involves the partial transfer of a layer taken from the donor substrate to form one or more tiles arranged in a predetermined pattern or location on the support substrate.

Such tiling may be rendered necessary by a size difference between the donor substrate and the support substrate. Specifically, due to this size difference, it is not possible to transfer a layer of the donor substrate covering the entire surface of the support substrate.

A well known layer transfer process is the Smart Cut™ process, in which an embrittlement area delimiting the layer to be transferred is formed by implanting atomic species into the donor substrate, the donor substrate is bonded to the support substrate, and the donor substrate is detached along the embrittlement area to transfer the layer from the donor substrate to the support substrate. However, this process assumes that the donor substrate and the support substrate have an identical size.

Now, while silicon substrates are available in relatively large sizes, typically 300 mm in diameter, other materials of interest are currently only available in the form of smaller, bulk substrates, for example 10 or 15 cm in diameter. Moreover, these materials of interest are sometimes particularly expensive, and so it is desirable to minimize any waste formed during transfer. Such is the case in particular with III-V semiconductor materials, comprising nitrides (for example, in the case of binary compounds, indium nitride (InN), gallium nitride (GaN) and aluminium nitride (AlN)), arsenides (for example, in the case of binary compounds, indium arsenide (InAs), gallium arsenide (GaAs) and aluminium arsenide (AlAs)), and phosphides (for example, in the case of binary compounds, indium phosphide (InP), gallium phosphide (GaP) and aluminium phosphide (AlP)).

Instead of transferring an entire layer of the donor substrate, a solution based on the Smart Cut™ process consists in taking one or more tiles from at least one donor substrate and transferring said tiles to an intermediate support, to form a “pseudo-donor substrate”, forming an embrittlement area in each tile by implanting atomic species, bonding the pseudo-donor substrate to a receiver substrate via the tiles, and detaching each tile along the embrittlement area so as to transfer a portion of each tile to the receiver substrate.

To allow bonding of the pseudo-donor substrate to the receiver substrate, the free surface of all the tiles must lie in the same plane. To this end, prior to bonding, CMP (chemical-mechanical polishing) may be performed, preferentially preceded by grinding of the pseudo-donor substrate. Chemical-mechanical polishing combines the mechanical action of a polishing pad and an abrasive powder with the chemical action of a polishing solution containing the abrasive powder (together, the abrasive powder and the solution are referred to as a slurry) to planarize the surface of the tile assembly.

However, if the distance between the tiles is large, typically greater than or equal to 250 μm , the polishing pad, which has a certain flexibility, becomes partially inserted into the gap between the tiles and thus erodes the edges of the tiles. This edge rounding reduces the useful surface area of the chips transferred onto the receiver substrate.

Conversely, the tile edges degrade the polishing pad very quickly, necessitating frequent replacement of the polishing pad and increasing the cost of the chemical-mechanical polishing operation.

To avoid such edge rounding of the tiles, it is thus desirable to form a pseudo-donor substrate in which the distance between tiles is less than or equal to 250 μm .

However, depending on the applications of the final structure comprising the receiver substrate and the chips, it may be necessary to have a distance between the chips greater than 250 μm , for example greater than 1 mm, or even more.

One solution then consists in reducing the size of the chips transferred onto the donor substrate, by applying a photolithography mask to locally protect one part of the chip surface and expose another part of the chip surface. Localized etching of the part of the chips exposed by the mask may then be performed, with the effect of reducing the chip size and increasing the distance between adjacent chips.

This process is not entirely satisfactory, however, as it requires great precision in mask placement and significantly increases the time for manufacture of the final structure. Moreover, it consumes a significant amount of chip material, which is generally expensive. This process is thus not economically feasible on an industrial scale.

SUMMARY OF THE INVENTION

One aim of the invention is thus to design a chip transfer process which avoids chip edge rounding, even when the chips are far apart, which is readily industrially usable and which minimizes chip material consumption.

To this end, the invention proposes a process for transferring chips from tiles arranged on a support substrate onto a receiver substrate, which comprises:

- forming a substrate, known as a pseudo-donor substrate, comprising the support substrate and the tiles, in which two adjacent tiles are separated by a first distance,
- performing chemical-mechanical polishing of the tiles,

- forming an embrittlement area in at least a part of the tiles so as to delimit a respective chip,
- bonding the pseudo-donor substrate to the receiver substrate via the tiles,
- detaching the tiles along the embrittlement area so as to transfer a respective chip onto the receiver substrate, with two adjacent chips being separated by a second distance greater than the first distance,

said process being characterized in that it comprises, prior to bonding, localized roughening of the surface of the tiles and/or of the receiver substrate to render areas of said surface incapable of bonding, so as to prevent the transfer of chips into said areas.

Localized roughening enables areas to be formed at the bonding interface, in which adhesion between the tiles and the receiver substrate is insufficient to allow chip transfer into these areas. Consequently, it allows chips to be selectively transferred to the receiver substrate, from a high density of tiles in the pseudo-donor substrate to a lower density of chips in the final structure. Insofar as only the desired chips are transferred onto the receiver substrate, there is no waste of chip material.

According to other advantageous but optional features, optionally combined where technically possible:

- roughening is performed by localized laser irradiation of the surface of the receiver substrate;
- laser irradiation is performed with a laser having a wavelength of between 100 nm and 550 nm, preferably between 250 nm and 400 nm, with pulse durations of between 1 ns and 10 μ s, preferably between 10 ns and 500 ns;
- the process comprises applying a pattern-defining mask and irradiating the surface through the mask;
- the pattern is chosen to delimit a plurality of areas on the receiver substrate separated by roughened areas facing the same tile, so as to allow the tile to be divided into several chips according to said pattern;
- the first distance is less than or equal to 250 μ m, preferably less than or equal to 100 μ m;
- the second distance is greater than or equal to 1 mm, preferentially greater than or equal to 2 mm;
- the formation of the embrittlement area is performed by implantation of ionic species;
- the pseudo-donor substrate comprises a first group and a second group of tiles;
- the process comprises successive transfer of the tiles of the first group and of the tiles of the second group onto at least one receiver substrate;
- the process comprises:
 - selective implantation of ionic species into the tiles of the first group to form an embrittlement area so as to delimit a chip in said tiles of the first group,
 - localized roughening of a first receiver substrate facing the tiles of the second group,

- bonding of the pseudo-donor substrate to the first receiver substrate,
- detachment of the tiles of the first group along the embrittlement area to transfer the respective chips onto the first receiver substrate,
- from the pseudo-donor substrate resulting from the detachment of the tiles of the first group, selective implantation of ionic species into the tiles of the second group to form an embrittlement area so as to delimit a chip in said tiles of the second group,
- localized roughening of a second receiver substrate facing the tiles of the first group,
- bonding of the pseudo-donor substrate to the second receiver substrate,
- detachment of the tiles of the second group along the embrittlement area to transfer the respective chips onto the second receiver substrate;
- only the chips of the first group of tiles are transferred to the receiver substrate and the pseudo-donor substrate is recycled into a new transfer of the chips of the first group of tiles;
- the tiles of the first and second groups are formed from different materials;
- the tiles of the first group have a higher crystallinity than the tiles of the second group;
- the tile materials of the first and second groups have substantially the same material removal rate and chemical reactivity with respect to chemical-mechanical polishing;
- the tiles comprise:
 - a semiconductor material, such as a III-V material, notably indium nitride (InN), gallium nitride (GaN), aluminium nitride (AlN), indium arsenide (InAs), gallium arsenide (GaAs), aluminium arsenide (AlAs), indium phosphide (InP), gallium phosphide (GaP) or aluminium phosphide (AlP), or a IV or IV-IV material, notably germanium or silicon carbide (SiC),
 - a piezoelectric material, such as lithium tantalate (LiTaO₃), lithium niobate (LiNbO₃), potassium sodium niobate (K_xNa_{1-x}NbO₃ or KNN), barium titanate (BaTiO₃), quartz, lead titanate-zirconate (PZT), a compound of lead-magnesium niobate and lead titanate (PMN-PT), zinc oxide (ZnO), aluminium nitride (AlN) or aluminium-scandium nitride (AlScN), and/or
 - an electrically insulating material, such as diamond, strontium titanate, yttriated zirconia or sapphire.

BRIEF DESCRIPTION OF THE FIGURES

Other features and advantages of the invention will become apparent from the detailed description which follows, with reference to the appended drawings, in which:

- Figure 1 shows a top view and a cross-sectional view of a pseudo-donor substrate according to one embodiment of the invention;
- Figure 2 shows a top view and a cross-sectional view of the pseudo-donor substrate of Figure 1 and a receiver substrate, prior to bonding;
- Figure 3 shows a cross-sectional view and a bottom view of the receiver substrate after transferring chips from the pseudo-donor substrate;

- Figure 4 shows a cross-sectional view and a top view of a pseudo-donor substrate according to an embodiment in which the tiles are divided into two groups;

- Figures 5A to 5F schematically illustrate the steps involved in two successive transfers of chips from the pseudo-donor substrate of Figure 4;

- Figure 6 shows a cross-sectional view and a top view of a pseudo-donor substrate according to an embodiment comprising tiles of interest and sacrificial tiles;

- Figure 7 shows a top view and cross-sectional view of the pseudo-donor substrate of Figure 1 and a receiver substrate, prior to bonding, in an embodiment in which an area of the receiver substrate has been roughened to form a pattern facing a tile of the pseudo-donor substrate.

For reasons of legibility of the figures, the various elements have not necessarily been represented to scale. Elements denoted by the same reference sign from one figure to another denote similar elements, which are thus not described each time.

DETAILED DESCRIPTION OF EMBODIMENTS

Figures 1 to 3 illustrate the general principle of the invention.

With reference to Figure 1, a pseudo-donor substrate 10 is formed by arranging tiles 1 on a support substrate 2.

The support substrate acts as a mechanical support for the tiles. The support substrate may be made of silicon, glass or sapphire (non-limiting list). The layer represented around the support substrate 2 in Figure 1 is an oxide layer, which is generally present around silicon substrates, but such a layer is optional.

The support substrate advantageously has a diameter greater than or equal to 150 mm, preferably greater than or equal to 200 mm, and more preferably greater than or equal to 300 mm.

Preferably, at least some of the tiles are formed from an expensive material available only in small sizes. Optionally, the tiles may be formed from a stack of such materials.

The tiles may advantageously comprise at least one of said materials:

- a semiconductor material, such as a III-V material, notably indium nitride (InN), gallium nitride (GaN), aluminium nitride (AlN), indium arsenide (InAs), gallium arsenide (GaAs), aluminium arsenide (AlAs), indium phosphide (InP), gallium phosphide (GaP) or aluminium phosphide (AlP), or a IV or IV-IV material, notably germanium or silicon carbide (SiC),

- a piezoelectric material, such as lithium tantalate (LiTaO₃), lithium niobate (LiNbO₃), potassium sodium niobate (K_xNa_{1-x}NbO₃ or KNN), barium titanate (BaTiO₃), quartz, lead titanate-zirconate (PZT), a compound of lead-magnesium niobate and lead titanate (PMN-PT), zinc oxide (ZnO), aluminium nitride (AlN) or aluminium-scandium nitride (AlScN), and/or

- an electrically insulating material, such as diamond, strontium titanate, yttriated zirconia or sapphire.

As shall be seen below, the tiles may be identical or formed from different materials.

In the illustrations shown, the tiles have four straight edges and are arranged at regular intervals from each other to form a grid comprising a set of parallel lines and columns. It will be noted, however, that this arrangement of tiles is for illustrative purposes only; thus, the tiles may optionally have different shapes, or be arranged at different distances from each other. Moreover, the tiles are not necessarily square, but may have any other shape suitable for their intended use, with or without a straight edge. For example, the tiles may have a rectangular, circular or other shape composed of lines and/or curves.

The tiles are spaced from each other, with a distance d_1 between the facing edges of two adjacent tiles. The distance d_1 may be identical between all tiles, or it may vary.

The distance d_1 is less than or equal to 250 μm , preferably less than or equal to 100 μm .

To form the pseudo-donor substrate, the tiles may be cut from one or more respective donor substrates, and placed on a temporary support by means of a robot (a technique known as “Pick and Place”). Advantageously, the tiles have the same thickness as the respective donor substrate. In general, the thickness of the tiles is between 50 μm and 1 mm, for example of the order of 300 to 650 μm , depending on the thickness of the donor material. The diameter of the donor substrate(s) is generally smaller than that of the temporary substrate and the support substrate.

The temporary support is formed, for example, from one of the following materials: adhesive tape held in place by a frame, silicon or glass (non-limiting list).

The tiles are then bonded to the support substrate, and the temporary support is then removed to expose the opposite surface of the tiles. Advantageously, the bonding of the tiles to the support substrate is direct, but it is possible to use a bonding layer between the tiles and the support substrate.

Alternatively, the tiles can be assembled directly on the support substrate with sufficient precision using the robot and alignment marks arranged on the support substrate. Use of the temporary support is thus avoided, as is the transfer of the tiles from the temporary support to the support to form the pseudo-donor substrate.

Chemical-mechanical polishing is then performed on the free surface of the tiles.

Optionally, this chemical-mechanical polishing may be preceded by a step to planarize the tiles by mechanical abrasion (“grinding”). Such planarization may notably be advantageous when the tiles have different thicknesses, so as to bring their free surfaces substantially into the same plane, or to reduce the thickness of the tiles. However, if the tiles have coplanar free surfaces, it is possible to dispense with such planarization and to perform chemical-mechanical polishing directly.

Chemical-mechanical polishing allows the surface of the tiles to be smoothed out to obtain a roughness that is compatible with bonding to a receiver substrate. Said roughness is typically less than 0.5 nm RMS. Such roughness is conventionally measured using an atomic force microscope

(AFM) over a field of $1\ \mu\text{m} \times 1\ \mu\text{m}$. Other measurement methods, such as optical interferometry, may also be used.

When the distance between the tiles is sufficiently small, the polishing pad acts essentially in the plane of the free surface of the tiles, without becoming inserted between the tiles. Consequently, the edges of the tiles remain straight (non-rounded). If such is not the case, the edges of the tiles may be rounded.

An embrittlement area is formed in at least a part of the tiles so as to delimit a chip to be transferred onto a receiver substrate.

The embrittlement area is typically formed by ion implantation, preferably of hydrogen and/or helium. A person skilled in the art is capable of defining the operating conditions for this implantation, depending on the tile material and the thickness of the chip to be transferred.

Formation of the embrittlement area is preferably performed after chemical-mechanical polishing, but may optionally be performed beforehand.

The receiver substrate may be a silicon substrate, but other materials may also be considered. In particular, the choice of material may be guided by the intended application (for example, to address issues of electrical and/or thermal conductivity in the final structure). The receiver substrate material may also be chosen as a function of its compatibility with respect to the tile material, for example with a coefficient of thermal expansion close to that of the tiles. For example, the receiver substrate may comprise gallium arsenide, sapphire or glass (non-limiting list).

The receiver substrate advantageously has a diameter identical to that of the pseudo-donor substrate support, but may optionally have a larger diameter.

To arrange the chips on the receiver substrate with an inter-chip distance greater than the inter-chip distance on the support substrate, localized bonding of the pseudo-donor substrate to the receiver substrate is performed. The term “localized bonding” means that adhesion between the tiles and the receiver substrate does not take place over the entire surface of the tiles in contact with the receiver substrate, but only over a given part of said surface. Chip transfer to the receiver substrate only occurs in those areas in which adhesion is sufficient.

To control the location of transferred chips, the surface of the tiles or receiver substrate is roughened in areas in which no chips are to be transferred. The roughened surface typically has a roughness greater than 0.5 nm RMS, preferably greater than 2 nm RMS, making it incapable of bonding. This thus allows selective bonding of tiles only in the non-roughened areas.

Roughening is advantageously performed by laser irradiation. The wavelength of the laser used can be chosen between 100 nm and 550 nm, preferably between 250 nm and 400 nm. Irradiation is performed in the form of pulses, typically lasting between 1 ns and 10 μs , more advantageously between 10 ns and 500 ns. For a silicon substrate treated at room temperature by a laser with a wavelength of 308 nm, with a pulse duration of 160 ns, the energy density provided is of the order of $1.9\ \text{J}/\text{cm}^2$ over areas measuring $15 \times 15\ \text{mm}^2$. The energy density corresponds to the

melting threshold of the irradiated material. A person skilled in the art is capable of adjusting the energy density as a function of the laser at his disposal and the material to be treated.

Preferably, irradiation is applied to the receiver substrate rather than to the tiles, so as not to affect the properties of the tiles, notably when they are made of a III-V material.

Roughened areas may be defined solely by controlled scanning of the laser beam over the surface of the receiver substrate, notably when the areas to be roughened have dimensions of about a few millimetres. Alternatively, and in particular for more precise control of the size and/or shape of the areas to be roughened, irradiation can be performed through a mask applied to the receiver substrate, the mask comprising apertures facing the areas to be roughened.

Figure 2 illustrates the receiver substrate 3, on which roughened areas 30 have been formed opposite certain tiles of the pseudo-donor substrate.

It will be noted that the non-roughened areas do not necessarily have the same size or shape as the tiles. Specifically, it is possible to roughen a part of the surface of the receiver substrate facing a tile, for example corresponding to the periphery of said tile, so as to allow transfer of a chip smaller in size than that of the tile (the part of the tile in contact with the roughened area not being transferred due to lack of adhesion).

In the cross-sectional view of Figure 2, the roughened areas 30 have been represented in slight relief relative to the rest of the surface of the receiver substrate 3 for ease of visualization, but they are generally coplanar with the rest of this surface.

Bonding involves aligning the pseudo-donor substrate and the receiver substrate, so as to ensure that the roughened areas face the tiles, and then placing the receiver substrate and tiles in contact.

For this alignment, the flat or notch that is generally present at the periphery of the substrates is in principle sufficient. Alternatively, the bonding machine may take into account the edges of the tiles to perform the alignment, or use alignment patterns placed on the receiver substrate.

After placing the pseudo-donor substrate and receiver substrate tiles in contact, the chips are detached along the embrittlement area. In a manner known *per se* (Smart Cut™ process), detachment may be initiated via heat treatment, mechanical and/or chemical action at the embrittlement area.

This detachment, and transfer of the chips to the receiver substrate, only takes place in areas in which there is sufficient adhesion between the tiles and the receiver substrate, i.e. in non-roughened areas. In roughened areas, transfer does not take place, so the chips remain entirely on the support substrate.

Thus, as shown in Figure 3, only part of the chips 1' have been transferred to the receiver substrate 3. As a result, the distance d2 between two adjacent chips 1' on the receiver substrate 3 is greater than the initial distance d1 between the tiles of the pseudo-donor substrate 10.

The distance d_2 may be greater than or equal to 1 mm, preferentially greater than or equal to 2 mm.

The remainder of the pseudo-donor substrate, which includes the remainder of the tiles from which the chips have been detached, and the tiles from which the chips have not been detached, may optionally be recycled into a new chip transfer process.

Various embodiments of the invention will now be described.

In the case illustrated in Figures 2 and 3, only part of the chips have been transferred. The remainder of the pseudo-donor substrate thus comprises tiles of two different thicknesses.

To recycle the pseudo-donor substrate, it is thus necessary to perform mechanical abrasion to bring all the tiles back to the same thickness, and then chemical-mechanical polishing to obtain a surface smooth enough for bonding.

However, this recycling process means that a thickness of material corresponding to the thickness of the chips is consumed on the tiles that have not been bonded.

Various solutions can be envisaged to optimize the use of the tiling material and/or to avoid wasting tiling material, notably when the latter is expensive.

A first solution consists in using the pseudo-donor substrate several times to transfer chips onto one or more receiver substrates.

As shown in Figure 4, the tiles are spread over the surface of the support substrate in two groups. For example, the pseudo-donor substrate comprises alternating tiles 11 of a first group and tiles 12 of a second group. The distance d_1 between two adjacent tiles, notably from two different groups, is less than or equal to 250 μm . On the other hand, the distance between two adjacent tiles of the same group is greater than 250 μm , preferably greater than 1 mm.

The tiles of both groups may be formed from the same material or stack of materials. Alternatively, the tiles of the two groups may be formed from two different materials or stacks of materials. For example, the tiles of the first group may comprise one semiconductor material and the tiles of the second group may comprise another semiconductor material, or a piezoelectric material.

The chips are transferred in two steps, depending on the group to which they belong.

In a first step, an embrittlement area 110 is selectively formed in the tiles 11 of the first group. To this end, a mask 4, for example made of graphite, is placed opposite the surface of the tiles, the mask comprising apertures facing the tiles 11 of the first group (Figure 5A). Ion implantation is then performed through the mask, so as to form the embrittlement area 110 in the tiles 11 of the first group, but not in the tiles 12 of the second group.

Elsewhere, the surface of the receiver substrate is locally roughened in the areas intended for contact with the tiles of the second group.

With reference to Figure 5B, the pseudo-donor substrate is bonded to the receiver substrate. Due to the roughening, adhesion occurs only between the tiles 11 of the first group and the receiver substrate 3.

The tiles 11 of the first group are detached along the respective embrittlement area 110, so that the chips 11' can be transferred onto the receiver substrate 3 (Figure 5C). The receiver substrate 3 thus comprises chips 11' separated by a distance d_2 greater than d_1 .

The pseudo-donor substrate may be reused directly for a second chip transfer step.

An embrittlement area 120 is selectively formed in the tiles 12 of the second group. To this end, a mask 4, for example made of graphite, is placed opposite the surface of the tiles, the mask comprising apertures facing the tiles 12 of the second group (Figure 5D). Ion implantation is then performed through the mask, so as to form the embrittlement area 120 in the tiles of the second group, but not in the remainder of the tiles of the first group.

Moreover, the surface of a receiver substrate is locally roughened, in the areas intended for contact with the tiles of the first group. The receiver substrate may be the same as the receiver substrate used in the first step, for example when the chips of the first and second groups are intended to be transferred to different areas of the receiver substrate. In this case, the relative orientation of the pseudo-donor substrate and the receiver substrate may be different between the two chip transfer steps, depending on the desired arrangement in the final structure. Alternatively, for the second step, a receiver substrate different from that used in the first step can be used.

With reference to Figure 5E, the pseudo-donor substrate is bonded to the receiver substrate. Due to the roughening, adhesion occurs only between the tiles 12 of the second group and the receiver substrate 3.

The tiles 12 of the second group are detached along the respective embrittlement area 120, so that the chips 12' can be transferred onto the receiver substrate (Figure 5F). The receiver substrate 3 thus comprises chips 12' separated by a distance d_2 greater than d_1 .

As the surface of the tiles in the second group has been polished prior to the first chip transfer step, it is capable of bonding and thus no chemical-mechanical polishing is required between the two chip transfer steps.

On conclusion of the second step, the pseudo-donor substrate can be recycled into two new chip transfer steps as described above, notably by chemical-mechanical polishing.

Needless to say, it would be possible to envisage more than two groups of tiles and consequently more than two chip transfer steps.

A second way of saving on tiling material consists in using a different material for tiles that are not intended for chip transfer.

As illustrated in Figure 6, the pseudo-donor substrate 10 is formed by arranging on the support substrate 2 tiles 1 of interest, which are intended for transferring a chip onto the receiver substrate, and tiles 5 of another material, generally less expensive than the material of the tiles of

interest. These other tiles 5 are sacrificial tiles, intended only to fill the gaps between the tiles of interest to ensure that the distance d_1 between two adjacent tiles is less than $250\text{ }\mu\text{m}$, so as to avoid rounding the edge of the tiles of interest during chemical-mechanical polishing, and to avoid damaging the polishing pad. Preferably, each tile of interest is surrounded by sacrificial tiles on each of its edges, so as to allow homogeneous polishing of said tile of interest.

The sacrificial tiles may consist of a material of the same composition as that of the tiles of interest, but may have lower crystallinity. For example, if the tiles of interest are made of single-crystal InP, the sacrificial tiles may be made of polycrystalline InP, or of single-crystal InP with a high dislocation content. An advantage of using the same material for both the tiles of interest and the sacrificial tiles is that all the tiles behave similarly with respect to chemical-mechanical polishing, notably with the same hardness and material removal rate. It is thus possible to perform homogeneous polishing of all the tiles.

Alternatively, the sacrificial tiles may be formed from a material with a different composition from that of the tiles of interest. In this case, the material of the sacrificial tiles should preferably be chosen to have a behaviour close to that of the material of the tiles of interest with respect to chemical-mechanical polishing, notably in terms of material removal rate (the ratio of removal rates typically needing to be less than 2) and chemical reactivity with respect to the slurry. In practice, a person skilled in the art knows how to find suitable material pairs for the tiles of interest and the sacrificial tiles either by choosing the slurry and adapting the material of the sacrificial tiles accordingly, or by choosing the material of the sacrificial tiles and conducting a study to determine or even tailor a slurry to have a similar material removal rate and chemical reactivity.

The pseudo-donor is subjected to ion implantation at least in the tiles of interest, so as to delimit thereon the chips to be transferred.

Depending on the behaviour of the sacrificial tiling material with respect to implantation, notably in terms of blistering, implantation may be performed simultaneously in the sacrificial tiles.

Alternatively, notably if the material of the sacrificial tiles generates sparge-related defects, implantation is performed only in the tiles of interest, using a mask as described in the preceding embodiment.

Blistering is a phenomenon known to those skilled in the art, in which ionic species implanted in the material deform its free surface under the effect of a heat treatment. The bubbles thus formed are thus liable to impair bonding.

The receiver substrate is subjected to localized roughening, so as to roughen the surface facing the sacrificial tiles.

The pseudo-donor substrate is bonded to the receiver substrate. Due to the roughening, adhesion occurs only between the tiles of interest and the receiver substrate.

When the tiles are detached along the embrittlement area, only the chips from the tiles 1 of interest are transferred to the receiver substrate, whether or not the sacrificial tiles 5 have an embrittlement area.

On the receiver substrate 3, the chips 1' are thus separated by a distance d_2 greater than d_1 .

The pseudo-donor substrate may be recycled into a new use of the tiles of interest. To this end, if necessary, mechanical abrasion is performed to make the sacrificial tiles flush with the tiles of interest, and chemical-mechanical polishing is then performed to make the surface of the tiles of interest capable of bonding.

Another application of roughening is the production of chips with shapes and/or sizes different from those of the tiles. Specifically, since transfer occurs only in sufficiently smooth areas, a tile can be broken down into a plurality of smaller chips by bonding it to a surface having alternately smooth and roughened areas.

This principle is illustrated schematically in Figure 7, which shows a magnified view of two facing areas on the receiver substrate and on the pseudo-donor substrate. The area on the pseudo-donor substrate corresponds to a single tile 1. The area 32 of the receiver substrate 3, on the other hand, comprises several areas of different roughness: smooth areas 31, capable of bonding the tile, and roughened areas 30 extending between the smooth areas, which are incapable of bonding. In the illustrated embodiment, these areas are arranged in a chessboard pattern, but it goes without saying that they could take on any other shape, depending on the desired shape of the chips.

Once the tile 1 has been bonded to said area 32 of the receiver substrate, and the tile detached along the embrittlement area, only those portions of the tile actually bonded to the receiver substrate are transferred onto the receiver substrate, forming chips.

The minimum size of the roughened areas depends on the laser used.

It may be useful to use a mask allowing more precise control of the size and shape of the areas to be roughened, notably when they have a size of less than 100 μm . The mask comprises apertures corresponding to the areas to be roughened, so as to allow irradiation of the receiver substrate surface only at these apertures, and to protect the rest of the receiver substrate surface.

Naturally, the embodiments presented above may be combined.

As regards the bonding conditions between the tiles and the receiver substrate, a person skilled in the art may use any known technique that is suitable for the materials under consideration. For example, he may form a dielectric layer, such as SiO_2 , Al_2O_3 , AlN or SiN , on the surface of the tiles and/or the receiver substrate, so as to perform oxide-to-oxide bonding. Alternatively, a person skilled in the art may use an intermediate bonding layer, such as a metal or a polymer. Bonding may be performed preferably at atmospheric pressure, but bonding under vacuum may be performed if necessary. A person skilled in the art may also perform annealing so as to reinforce the bonding energy.

CLAIMS

1. Process for transferring chips from tiles arranged on a support substrate onto a receiver substrate, which comprises:

- forming a substrate (10), known as the pseudo-donor substrate, comprising the support substrate (2) and the tiles (1, 11, 12), in which two adjacent tiles are separated by a first distance (d1),
- performing chemical-mechanical polishing of the tiles (1),
- forming an embrittlement area (110, 120) in at least a part of the tiles (1, 11, 12) so as to delimit a respective chip (1', 11', 12'),
- bonding the pseudo-donor substrate (10) to the receiver substrate (3) via the tiles (1, 11, 12),
- detaching the tiles (1, 11, 12) along the embrittlement area (110, 120) so as to transfer a respective chip (1', 11', 12') onto the receiver substrate (3), two adjacent chips being separated by a second distance (d2) greater than the first distance (d1),

said process being characterized in that it comprises, prior to bonding, localized roughening of the surface of the tiles (1, 11, 12) and/or of the receiver substrate (3) to render areas (30) of said surface incapable of bonding, so as to prevent the transfer of chips into said areas.

2. Process according to claim 1, wherein roughening is performed via localized laser irradiation of the surface of the receiver substrate (3).

3. Process according to claim 2, wherein laser irradiation is performed with a laser having a wavelength of between 100 nm and 550 nm, preferably between 250 nm and 400 nm, in pulses having a duration of between 1 ns and 10 μ s, preferably between 10 ns and 500 ns.

4. Process according to claim 2, comprising the application of a pattern-defining mask and irradiation of the surface through the mask.

5. Process according to claim 4, wherein the pattern is chosen to delimit a plurality of areas of the receiver substrate separated by roughened areas facing the same tile, so as to allow the tile to be divided into several chips according to said pattern.

6. Process according to one of claims 1 to 5, wherein the first distance (d1) is less than or equal to 250 μ m, preferably less than or equal to 100 μ m.

7. Process according to one of claims 1 to 6, wherein the second distance (d2) is greater than or equal to 1 mm, preferentially greater than or equal to 2 mm.

8. Process according to one of claims 1 to 7, wherein the formation of the embrittlement area is performed by implantation of ionic species.

9. Process according to one of claims 1 to 8, wherein the pseudo-donor substrate comprises a first and a second group of tiles (11, 12).

10. Process according to claim 9, wherein tiles (11) from the first group and tiles (12) from the second group are successively transferred onto at least one receiver substrate.

11. Process according to claim 10 in combination with claim 8, comprising:

- selective implantation of ionic species in the tiles (11) of the first group to form an embrittlement area (110) so as to delimit a chip (11') in said tiles of the first group,
- localized roughening of a first receiver substrate (3) facing the tiles (12) of the second group,
- bonding of the pseudo-donor substrate to the first receiver substrate (3),
- detachment of the tiles (11) of the first group along the embrittlement area (110) to transfer the respective chips (11') onto the first receiver substrate (3),
- from the pseudo-donor substrate resulting from the detachment of the tiles of the first group, selective implantation of ionic species in the tiles (12) of the second group to form an embrittlement area (120) so as to delimit a chip (12') in said tiles of the second group,
- localized roughening of a second receiver substrate facing the tiles of the first group,
- bonding of the pseudo-donor substrate to the second receiver substrate,
- detachment of the tiles from the second group along the embrittlement area to transfer the respective chips onto the second receiver substrate.

12. Process according to claim 9, wherein only the chips (11') from the first group of tiles are transferred onto the receiver substrate (3), and the pseudo-donor substrate (10) is recycled for a new transfer of the chips from the first group of tiles (11).

13. Process according to one of claims 9 to 12, wherein the tiles (11, 12) of the first and second groups are formed from different materials.

14. Process according to claim 12, wherein the tiles (11) of the first group have a higher crystallinity than the tiles (12) of the second group.

15. Process according to either of claims 13 and 14, wherein the materials of the tiles (11, 12) of the first and second groups have the same material removal rate and chemical reactivity with respect to chemical-mechanical polishing.

16. Process according to one of claims 1 to 15, wherein the tiles (1, 11, 12) comprise:

- a semiconductor material, such as a III-V material, notably indium nitride (InN), gallium nitride (GaN), aluminium nitride (AlN), indium arsenide (InAs), gallium arsenide (GaAs), aluminium arsenide (AlAs), indium phosphide (InP), gallium phosphide (GaP) or aluminium phosphide (AlP), or a IV or IV-IV material, notably germanium or silicon carbide (SiC),

- a piezoelectric material, such as lithium tantalate (LiTaO_3), lithium niobate (LiNbO_3), potassium sodium niobate ($\text{K}_x\text{Na}_{1-x}\text{NbO}_3$ or KNN), barium titanate (BaTiO_3), quartz, lead titanate-zirconate (PZT), a compound of lead-magnesium niobate and lead titanate (PMN-PT), zinc oxide (ZnO), aluminium nitride (AlN) or aluminium-scandium nitride (AlScN), and/or

- an electrically insulating material, such as diamond, strontium titanate, yttriated zirconia or sapphire.