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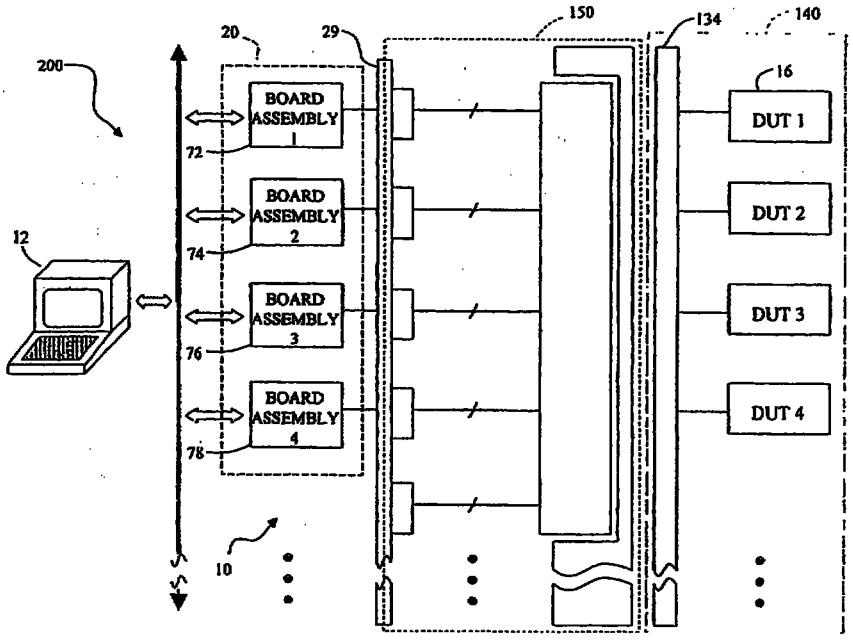
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(54) Title: SEMICONDUCTOR PARALLEL TESTER



(57) Abstract: A semiconductor parallel tester is disclosed for simultaneously testing a plurality of DUTs secured to a handling apparatus. The test system includes a system controller for initiating system test signals and a pin electronics assembly responsive to the system test signals to generate test pattern signals for application to the plurality of DUTs. The system further includes a signal interface defining a plurality of direct signal paths between the handling apparatus and the pin electronics assembly.

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