

# PATENT SPECIFICATION

(11) 1 459 922

- (21) Application No. 941/74 (22) Filed 9 Jan. 1974  
 (31) Convention Application No. 7301421 (32) Filed 1 Feb. 1973 in  
 (33) Netherlands (NL)  
 (44) Complete Specification published 31 Dec. 1976  
 (51) INT CL<sup>3</sup> H04N 3/16  
 (52) Index at acceptance

H4T 1D 1X11 2D2 2E4P 2E4X 2U2X  
 H2F 23E1T 23E2R 23E2T1 23E4A 23EY



## (54) TELEVISION LINE-OUTPUT CIRCUIT

(71) We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED, of Abacus House, 33 Gutter Lane, London, E.C.2., a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to a circuit arrangement for generating a line frequency sawtooth deflection current having a trace period and including a sawtooth network comprising a diode, the deflection coil, a trace capacitor and a retrace capacitor, the circuit arrangement also including supply terminals for receiving a supply voltage from source and a controlled switch which is non-conductive during the retrace period.

Such a circuit arrangement is typically described in United States Patent Specification 3,444,426. For the correction of the raster distortion in the horizontal direction, the so-called East-West correction of the displayed image in television display apparatus the supply voltage is the sum of a direct voltage and a field frequency parabolic voltage. The latter voltage originates from the field deflection current generator which forms part of the same television display apparatus. As a result the line deflection current undergoes the field frequency modulation which is desired for this correction.

A drawback of the known circuit arrangement is that the retrace pulses which are present during the retrace period across an inductor arranged between the switching means and the supply voltage source are also field frequency modulated. A winding is coupled to this inductor with which these pulses are transformed and are applied to a rectifier for generating the EHT for the acceleration anode of the television display apparatus. An unwanted modulation of the EHT thus occurs. This also applies to auxiliary voltages which can be generated in known manner by other windings coupled to the inductor.

A further drawback of the known arrangement is that it requires a good stabilisation

circuit for the supply voltage in order that both the direct voltages and the field frequency component thereof remain constant in spite of the inevitable fluctuations of the voltage derived from the electrical means and applied to the stabilisation circuit and in spite of the possible variations of the loads on the windings.

The former drawback may be obviated by known arrangements in which two generators are used one of which provides at least the East-West modulated share of the signal and which are decoupled relative to each other by means of a bridge circuit. In this case a transformer is necessary and the balance must be adjusted by means of a bridge coil which balance must remain under all circumstances.

It is an object of the invention to provide an arrangement in which the supply voltage need not be stabilized nor field frequency modulated.

The invention provides a circuit arrangement of the type described in the opening paragraph which is additionally provided with a second sawtooth network comprising a second diode, a second coil, a second trace capacitor and a second retrace capacitor, the retrace period for the current when flowing through the second coil being approximately equal to the retrace period for the deflection current, the sawtooth networks being connected together such that the first mentioned and second diodes are connected in series with the same conductivity direction, the series arrangement of the diodes being connected in parallel across the controlled switch and control means for varying the voltage across one of the trace capacitors.

It will be evident that the invention need not be limited to providing the East-West correction but may also be used, for example, for stabilisation against supply voltage variations or for generating a correction difference current and generally for obtaining any required variation of the voltage across the trace capacitor.

The invention will be further described, by way of example, with reference to the accompanying drawings, in which:

55

60

65

70

75

80

85

90

95

100

Figure 1 shows a television display apparatus with a first embodiment of the circuit arrangement according to the invention, and

Figures 2 to 7 show further embodiments of the circuit arrangement according to the invention.

The television display apparatus of Figure 1 has an RF tuning unit 1 for connection to an aerial 2, an IF amplifier 3, a detector 4 and a video amplifier with a colour decoder 5 which applies the colour signals to a colour display tube 6. This tube has an acceleration anode 7 and is provided with a coil  $L_x$  for the horizontal (line frequency) deflection and a coil  $L_y$  for the vertical (field frequency) deflection.

Line synchronizing pulses, which are applied to a line oscillator 9, are separated by means of a sync separator 8 from the output signal from the detector 4, whilst separated field synchronizing pulses are applied to a field oscillator 10. Oscillator 10 controls a field output stage 11 which supplies the field deflection current for coil  $L_y$ . Line oscillator 9 controls a driver stage  $D_x$  which applies line switching pulses to a controlled switch, for example, a switching transistor  $T_x$  of a line deflection output circuit to be further described and which provides the line deflection circuit for the coil  $L_x$ .

A trace capacitor  $C_t$  is arranged in series with line deflection coil  $L_x$  whilst a Diode  $D$  with the given conductivity direction and a retrace capacitor  $C_r$  are connected in parallel with the series arrangement thus constituted. Capacitor  $C_r$  may alternatively be arranged in parallel with coil  $L_x$ . These four circuit elements represent the main components of the line deflection section. This section may be additionally provided, for example, in known manner with one or more transformers for mutual coupling of the elements, with circuits for centring and linearity correction and the like.

One (the lower) end or a tap of a primary winding  $L_1$  of a transformer  $T$  is connected to the collector of transistor  $T_x$  which is of the npn type and is connected to the junction A of elements  $D$ ,  $C_r$  and  $L_x$ . The positive terminal of a direct voltage source B whose negative terminal is connected to ground is connected to the other (upper) end of winding  $L_1$ .

The ends of elements  $D$ ,  $C_r$  and  $C_t$  not connected to deflection coil  $L_x$  are connected to the junction of a diode  $D'$ , a capacitor  $C'$ , and a coil  $L'$ . A capacitor  $C'$  is arranged in series with coil  $L'$ , the free ends of elements  $D'$ ,  $C'$  and  $C_t$  being connected to ground. The conductivity direction of diode  $D'$  is the same as that for diode  $D$  so that the anode of diode  $D'$  is connected to ground. Elements  $D'$ ,  $L'$ ,  $C'$  and  $C_t$  constitute a network which is of the same as or the equivalent of the network constituted by the ele-

ments  $D$ ,  $L_x$ ,  $C_r$  and  $C_t$ , but optionally at a different impedance level.

A modulation source  $M_x$  is arranged in parallel with the capacitor  $C'$ . This modulation source includes a transistor  $T_x'$  whose emitter is connected to ground and whose collector is connected to the junction of coil  $L'$  and capacitor  $C'$ , as well as a driver stage  $D_x'$  controlling the base electrode of  $T_x'$  which stage has its input connected to the field output stage 11. Driver stage  $D_x'$  derives from the signals of the field output stage a field frequency parabolically varying modulation control signal, which control signal serves to provide for East-West raster correction in the line deflection current. This signal varies at the field frequency but may be considered to be constant during a line period. Since the raster distortion to be corrected is generally pin-cushion shaped it is known that the introduced modulation must be such that the amplitude of the line deflection current varies in a parabolic manner over a field period while the peak (maxima) of the parabola occurs in the middle of the field trace time.

Other windings across which voltages are present serving as supply voltages for other parts of the television display apparatus are wound on the core of transformer  $T$ . One of these windings, winding  $L_2$ , is shown in Figure 1 and generates the EHT for the acceleration anode 7 of television display tube 6 with the aid of an EHT rectifier  $D_1$  across a smoothing capacitance  $C_1$ . The auxiliary supply voltages thus obtained and the EHT must not be subjected to the same field frequency modulation as the line deflection current.

After the commencement of the trace (line scan) period diodes  $D$  and  $D'$  conduct. The voltage across capacitors  $C_t$  and  $C'$  is applied to coil  $L_x$  and  $L'$ , respectively, so that a saw-tooth current flows through each coil. The current  $i_x$  through coil  $L_x$  is the line deflection current. Before the middle of the trace period the base of transistor  $T_x$  receives a control signal so that it is rendered conducting. Approximately in the middle of the trace period the two currents reverse their direction. If current  $i_x$  is larger than the current  $i'$  through coil  $L'$ , current  $i_x$  flows through transistor  $T_x$ , while the difference  $i_x - i'$  flows through diode  $D'$ . Diode  $D$  is connected in parallel with the series arrangement of the transistor  $T_x$  (being in the bottomed state) and diode  $D'$  and as the mean voltage across diode  $D$  is substantially zero it does not conduct. In the reverse case in which current  $i'$  is larger than current  $i_x$ , current  $i'$  flows through transistor  $T_x$  and the difference  $i' - i_x$  flows through diode  $D$  and diode  $D'$  then does not conduct.

At the end of the trace period transistor  $T_x$  and hence the diode which was conduct-

ing are cut off. A substantially sinusoidal retrace (flyback) voltage is produced across capacitors  $C_r$  and  $C'_r$ . At the instant when these voltages become zero again diodes D and D' simultaneously become conducting: this is the commencement of a new trace period. The condition therefor is that the retrace periods determined by diodes D and D' and elements  $C_r$ ,  $L_r$ ,  $C_t$  and  $C'_r$ ,  $L'$ ,  $C'_t$  are substantially equal, which is the case when the resonant frequencies of the individual networks are equal, whereby the retrace period is a known function of the resonant frequency.

Since transistor  $Tr'$  is connected in parallel with capacitor  $C'_t$ , there is, as it were, a field frequency varying load on the voltage  $v'$  present across this capacitor. When the capacitance of this capacitor is chosen to be such that its impedance at field frequency is not negligibly small relative to the output impedance of source  $M_1$ , voltage  $v'$  and also the voltage  $v$  across capacitor  $C_t$  will vary at the field frequency, provided that capacitor  $C_t$  is chosen in the same manner as capacitor  $C'_t$ . The sum of the mean values of voltages  $v$  and  $v'$  is in fact equal to the voltage  $V_B$  of source B since no direct voltage can remain present across the inductors  $L_1$ ,  $L_r$  and  $L'$ . The amplitude of current  $i_r$  undergoes the same variation as the voltage  $v$ . The control signal for transistor  $Tr'$  must be such that voltage  $v$  and consequently the field frequency envelope of current  $i_r$  has the above-mentioned desired shape.

Voltage  $v$  is substantially equal to the mean value of the voltage present across capacitor  $C_r$  and is proportional to the retrace voltage thereacross. Voltage  $v'$  is also substantially equal to the mean value of the voltage present across capacitor  $C'_r$  and is proportional to the retrace voltage thereacross. As already stated, the retrace periods of networks D,  $C_r$ ,  $L_r$ ,  $C_t$  and D',  $C'_r$ ,  $L'$ ,  $C'_t$  are substantially equal. Both retrace voltages are therefore equal in frequency and shape and both proportionally constants are equal. The voltage  $v_A$  at point A is equal to the sum of the voltages present across capacitors  $C_r$  and  $C'_r$  and the peak value of voltage  $v_A$  relative to its mean value i.e. the voltage  $V_B$  of source B, is in the same relation as are the retrace voltages across the capacitors  $C_r$  and  $C'_r$  relative to voltages  $v$  and  $v'$ . If voltage  $V_B$  is constant, the peak value of voltage  $v_A$  is also constant. It follows that the amplitude of the voltage present across winding  $L_1$  is also constant which means that the EHT on electrode 7 as well as the auxiliary supply voltages do not undergo a field frequency modulation in spite of the modulation of deflection current  $i_r$ .

The variation of voltage  $v'$  is opposite to that of the voltage  $v$  so that voltage  $v'$  must be minimum in the middle of the field

trace time. The same result as above may alternatively be achieved by not providing the modulation source in parallel with the capacitor  $C'_t$  but with capacitor  $C_t$  in which the polarity of the control signal of transistor  $Tr'$  must be reversed relative to the control signal for Figure 1. Another modification is that in which transistor  $Tr'$  is not provided as a varying load but as a current or voltage source. The latter case occurs when transistor  $Tr'$  is arranged, for example, as an emitter follower.

In practice the ratio between the inductances of coils  $L_r$  and  $L'$  will be chosen to be approximately equal to the ratio of the mean trace voltages which are desired thereacross. When for example the total trace voltage  $v+v'$  is approximately 150 volts, the inductance of coil  $L'$  may be equal to a quarter of that of coil  $L_r$  in case of a mean direct voltage component of voltage  $v'$  of approximately 30 V, a practical example being approximately 270  $\mu$ H and 1.2 mH. By adjusting the direct voltage component of voltage  $v'$  the width of the picture displayed is adjusted while the amplitude of the field frequency component is adjusted to provide an undistorted picture.

It has been assumed in the foregoing that the voltage  $V_B$  is constant. This means that this voltage must be stabilized against fluctuations in the electrical mains, possible variations of the different loads on transformer T and against hum voltages originating from the mains. Such a stabilisation is not necessary with the embodiment of Figure 2. In Figure 2 only the important circuit elements are shown. The arrangement includes the same networks D,  $C_r$ ,  $L_r$ ,  $C_t$  and D',  $C'_r$ ,  $L'$ ,  $C'_t$  and modulation source  $M_1$  in Figure 1. The junction A of the collector of transistor Tr and the former network is connected through a choke  $L_3$  to source B. Furthermore Figure 2 includes a third similar network D'',  $C''_r$ ,  $L''$ ,  $C''_t$  which is in series between the two former networks and ground to which, in the same manner as with source  $M_1$ , a stabilisation circuit S is connected to the third network which has the same retrace period as the two former networks. Stabilisation circuit S has a terminal 12 to which information is applied regarding either variations in the voltage  $v+v'$ , or those in the peak value of the voltage  $v_A$  present across the series arrangement of networks D,  $C_r$ ,  $L_r$ ,  $C_t$  and D',  $C'_r$ ,  $L'$ ,  $C'_t$ . It includes a reference voltage source with which this information is compared so that the required variation of the voltage  $v''$  present across capacitor  $C''_t$  is obtained whilst voltage  $v_A$  is maintained constant without the voltage at the collector of transistor T, being constant. The primary winding  $L_1$  of transformer T and a series decoupling capacitor are arranged in parallel with the series arrangement of networks D,  $C_r$ ,  $L_r$ ,

70

75

80

85

90

95

100

105

110

115

120

125

130

$C_1$  and  $D'$ ,  $C'_1$ ,  $L'$ ,  $C'_1$ . The EHT and the auxiliary supply voltages derived from the transformer T are thus independent of the variations in the voltage  $V_B$ . As is the case in Figure 1 they are also free from field frequency modulation, while current  $i_x$  undergoes the desired modulation. It will be evident that the arrangement of Figure 2 may alternatively be used without network  $D'$ ,  $C'_1$ ,  $L'$ ,  $C'_1$ , for example in a monochrome television display apparatus when the correction for pin-cushion distortion in the East-West direction can be obtained by permanent magnets. In this case the voltage  $v$  is maintained constant so that the retrace voltage is suitable for generating the EHT.

Figure 3 shows a further modification of the arrangement according to the invention in which, as with Figure 2, voltage  $V_B$  need not be stabilized. In this Figure use is made of a circuit arrangement which is described in the publication "IEEE Transactions on Broadcast and Television Receivers", August 1972, vol. BTR-18 No. 3, pages 177 to 182 and which is a combination of a line deflection and a switched supply voltage stabilizing circuit. A diode  $D_2$  having the same conductivity direction as the collector current of the transistor is arranged in series between point A and transistor  $T_1$ , while the primary winding  $L_1$  of transformer T is arranged between source B and the junction of transistor  $T_1$  and diode  $D_2$ . The series arrangement of a diode  $D_2$  and a secondary winding  $L_2$  of transformer T is arranged between point A and ground, the cathode of diode  $D_2$  being connected to point A. The winding sense of the windings of transformer T shown is denoted by polarity dots in the Figure. Driver circuit Dr has a comparison stage and a modulator so that the conductivity time of transistor Tr can be controlled.

The peak value of voltage  $v_A$  may be maintained constant in the embodiment of Figure 3 in spite of variations in the voltage  $V_B$  and in spite of the field frequency modulation of voltages  $v$  and  $v'$  if the voltage at the junction of coil  $L_1$  and capacitor  $C_1$  is applied through a lowpass filter F to the comparison stage of driver circuit Dr. This is shown by broken lines in the Figure. The output signal from the lowpass filter is in fact the mean value of the voltage  $v+v'$ . A condition therefor is that filter F does not pass a line frequency component but passes a possibly present field frequency component. Instead of using voltage  $v+v'$ , voltage  $v_A$  may be applied to filter F. In a further alternative shown in Figure 3 the control is brought about by a voltage across a secondary winding  $L_3$  of transformer T which is rectified by means of a peak rectifier  $D_3$ ,  $C_3$ , the direct voltage thus obtained being applied to driver circuit Dr to control the periods of conduction of transistor Tr. The amplitude

of the voltage across winding  $L_3$  and consequently voltage  $v_A$  which is proportional thereto is maintained constant by this control. It is alternatively possible to peak rectify voltage  $v_A$  and employ the resulting rectified voltage in a similar way.

It may be noted that it is possible in the embodiments of Figures 2 and 3 to give the voltage  $v_A$  any desired variation by an appropriate control of the circuits S and D.

A further embodiment is shown in part in Figure 4a in which the section to the left of point A (not shown) can be formed in the same manner as in Figure 1 or in Figure 3. In Figure 4a line deflection coil  $L_1$  is divided into two equal coil halves  $L_{11}$  and  $L_{12}$  which are incorporated in two substantially identical networks  $d_1$ ,  $C_{11}$ ,  $L_{11}$ ,  $C_{11}$  and  $d_2$ ,  $C_{12}$ ,  $L_{12}$ ,  $C_{12}$ . These networks are arranged in series with the network  $D'_1$ ,  $C'_1$ ,  $L'_1$ ,  $C'_1$  for the East-West correction in which modulation source  $M_1$  is arranged in parallel with capacitor  $C'_1$ . A second modulation source  $M_2$  may be arranged in parallel with capacitor  $C_{12}$  for causing such a variation of the voltage across this capacitor that a correction difference current  $i_x$  in one coil half for example  $L_{11}$  is added to deflection current  $i_y$  and is subtracted from deflection current  $i_y$  in the other coil half, for example,  $L_{12}$ . As is known coil halves  $L_{11}$  and  $L_{12}$  then generate a correction quadripolar field which eliminates deflection errors. Such a quadripolar field is described in our Patent Specification Serial No. 1,230,162 in which the instantaneous intensity of current  $i_x$  is proportional to the product of the instantaneous intensities of the two deflection currents and by which anisotropic astigmatic deflection errors can be reduced or eliminated. The peak value of voltage  $v_A$  across the series arrangement of the three networks is maintained constant as has been described with reference to Figure 1, 2 or 3.

The embodiment of Figure 4a has the drawback that a DC component of correction current  $i_x$  flows through coil half  $L_{12}$  but not through coil half  $L_{11}$  which may in itself cause errors. The embodiment of Figure 4b does not have this drawback: here the modulation source  $M_2$  is connected through a choke  $L_2$  to the junction of diodes  $d_1$  and  $d_2$ , coil  $L_2$  blocking line frequency signals but not field frequency signals. The output voltage from source  $M_2$  is field frequency sawtooth shaped. Capacitor  $C_{12}$  is included between coil  $L_2$  and the junction of coil halves  $L_{11}$  and  $L_{12}$  so that this capacitor forms part of the two networks. A field frequency modulated line frequency pulsatory voltage is produced at the junction of diodes  $d_1$  and  $d_2$ . The envelope of the retrace voltage across a diode for example  $d_2$  is a decreasing sawtooth and that of the retrace voltage across the other diode, for example,

$d_1$  is an increasing sawtooth. The sum of these voltages shown in the Figure is in fact constant. The currents produced by these voltages through coils  $L_{y1}$  and  $L_{y2}$  are proportional to the integral of the line frequency voltages across the coils and are therefore sawtooth shaped. Thus these currents are the desired currents  $i_y + i_x$  and  $i_y - i_x$ . It will be evident that other known correction difference currents can be generated in a similar manner.

Figure 5 shows a modification in which the circuit arrangement according to the invention generates a current for the raster correction in the vertical direction, the so-called North-South correction, of the displayed picture. The deflection network  $D$ ,  $C_r$ ,  $L_y$ ,  $C_t$  is in series with the network  $D'$ ,  $C'_r$ ,  $L'_y$ ,  $C'_t$  for the East-West correction and with a third similar network  $D''$ ,  $C''_r$ ,  $L''_y$ ,  $C''_t$ . Modulation source  $M_2$  is connected in parallel with capacitor  $C''_t$  and produces a field frequency sawtooth signal whilst modulation source  $M_1$  is connected in parallel with the series arrangement of capacitors  $C'_t$  and  $C''_t$  and produces a field frequency parabolic signal. Because the sum of the voltages across capacitors  $C_t$ ,  $C'_t$  and  $C''_t$  is constant (=the constant direct voltage component of voltage  $v_A$ ) and because the sum of the voltages across the capacitors  $C'_t$  and  $C''_t$  varies parabolically, the voltage across capacitor  $C_t$  also varies parabolically and no sawtooth component is present in this voltage. Consequently a field frequency sawtooth component is not present in the line deflection current.

A line frequency pulsatory voltage having a field frequency sawtooth envelope is present across a winding  $L''_2$  which is coupled to winding  $L''_1$ . A line frequency pulsatory voltage with a constant amplitude which is provided by a winding  $L_2$  of transformer  $T$  is subtracted from this voltage. These waveforms are shown in Figure 5. Winding  $L''_2$  is connected in series with a coil  $L_3$  and the field deflection coil  $L'_y$  which coil is connected to the field deflection current generator 11. A capacitor  $C_3$  is arranged between the junction of coils  $L_3$  and  $L'_y$  and ground while the connection terminal of coil  $L'_y$  to generator 11 is connected to ground by means of an absorption circuit 13 for line frequency signals whilst the junction of winding  $L''_2$  and coil  $L_3$  is connected to ground through windings  $L''_2$  and  $L_2$  for field frequency signals. The voltage present between the junction of winding  $L''_2$  and coil  $L_3$  is line frequency pulsatory with a field frequency sawtooth envelope which becomes zero in the middle of the field trace time.

A line frequency sinusoidal voltage having a field frequency sawtooth envelope is produced in known manner across the capacitor  $C_3$ , which voltage produces a cosine-shaped current through field deflection coil  $L'_y$  which

current is superimposed on the field deflection current and has substantially the required parabolic shape. This current is therefore the North-South correction current.

No requirement has been imposed in the foregoing on the capacitors  $C_t$  and  $C'_t$  except for the fact that the impedance thereof must not be too small at field frequency. In practice the capacitor  $C_t$  is used for the so-called S correction. It is known for example from the publication "Philips Application Information No. 268: All Transistor 110° Colour Television" that the linearity of the line deflection can be improved when the S-correction which is modulated more by an East-West component than by the deflection current which can be realized with the modification of Figure 6. In this Figure capacitor  $C'_t$  forms part of the two networks  $D$ ,  $C_r$ ,  $L_y$ ,  $C_t$  and  $D'$ ,  $C'_r$ ,  $L'_y$ ,  $C'_t$  while modulation source  $M_1$  is connected through a coil  $L_3$  to the junction of diodes  $D$  and  $D'$ . The ratio of the capacitances of the capacitors  $C_t$  and  $C'_t$  is given by the desired modulation of the S-correction which modulation is in turn determined by the geometrical properties of the television display tube. The embodiment of Figure 1 cannot be used in this case because the junction of capacitor  $C_t$  and coil  $L'_y$  is connected to ground during the line trace time. This is not the case in Figure 6 due to the presence of capacitor  $C'_t$ . Similarly as in the embodiment of Figure 4b no direct current flows through coil  $L'_y$  in Figure 6.

In the embodiments described the appropriate inductor present between point A and the positive terminal of source B and consequently being in parallel across the networks, has not been taken into account. This is justified as long as this inductor has a high impedance at the line frequency. However, this parallel impedance cannot be considered to be infinitely large, when a parasitic capacitance, which is not negligible, is present across this inductor, for example, choke  $L_3$  in Figure 2, to which capacitance is contributed by the part of the circuit arrangement around the switch, for example, transistor  $Tr$  or a thyristor, as well as by the EHT rectifier circuit. The result is that the resonant frequencies of the individual networks are no longer equal and consequently neither are their retrace times. It is evident that the retrace periods will be equal when the resonant frequency of the circuit constituted by the said inductor and the capacitance present thereacross is equal to those of the networks.

However, the real capacitance  $C_p$  may be so large that the resonant frequency is too low. During the retrace period both capacitor  $C_p$  and the total primary inductor  $L_p$  of transformer  $T$  in Figure 1 are in parallel across the series arrangements  $C_r$ ,  $C'_r$  and  $L_y$ ,  $L'_y$  (the capacitances of capacitors  $C_t$  and

17

18  
6

C', are too large to have an essential influence). Capacitors C<sub>1</sub> and C', thus constitute a capacitor potential divider so that the above-described circuit may be replaced in known manner by a circuit having an inductive potential divider. This is shown in Figure 7. A capacitor C<sub>4</sub> is arranged between point A and ground and a capacitor C<sub>5</sub> is arranged between a tap on the winding L<sub>1</sub> and the junction of diodes D and D', the capacitors C<sub>4</sub> and C', being emitted from the circuit. The capacitances of capacitors C<sub>4</sub> and C<sub>5</sub> and the position of the tap can be determined in a simple manner with reference to capacitor C<sub>2</sub> and the previously required capacitances of capacitors C<sub>1</sub> and C'. It may be noted that capacitors C<sub>4</sub> and C<sub>5</sub> actually take over the task of the retrace capacitors of the two networks.

In the embodiment of Figure 7 the series arrangement of L<sub>1</sub>, C<sub>1</sub> is not connected to the junction of elements C', and L' but to a tap on coil L' for the following reason. In the middle of the field trace period the East-West modulation is deepest. When in addition, as described above, the S correction is more modulated than the deflection current, it is possible without this step for the current through diode D' to become negative, i.e. diode D' would stop conducting. When this step is used, a current flows through this diode which is the sum of the current in the original embodiment and of a current proportional to current i<sub>1</sub> and has therefore a greater intensity. The position of the tap may be chosen to be such that it is ensured that diode D' continues to conduct under all circumstances during the first half of the line trace time. Such a step is also possible for the embodiments of Figures 4b and 6 in which the retrace capacitors can be formed as in Figure 7 or in another manner (for example by means of a capacitor connected in parallel with coil L<sub>1</sub> and one between the tap of coil L' and ground).

#### WHAT WE CLAIM IS:—

1. A circuit arrangement for generating a line frequency sawtooth deflection current having a trace period and a retrace period through a deflection coil, said arrangement including a first sawtooth network comprising a first diode, said deflection coil, a trace capacitor and a retrace capacitor, a second sawtooth network comprising a second diode, a second coil, a second trace capacitor and a second retrace capacitor, the retrace period for the current when flowing through the second coil being approximately equal to the retrace period for the deflection current, the arrangement also including supply terminals for receiving a supply voltage from a source and a controlled switch which is non-conducting during the retrace period, said sawtooth networks being connected together such that

the first and second diodes are connected in series with the same conductivity direction, the series arrangement of the diodes being connected in parallel across the controlled switch, and control means for varying the voltage across one of the trace capacitors.

2. A circuit arrangement as claimed in Claim 1, including a further sawtooth network having a further diode, a further coil, a further trace capacitor and a further retrace capacitor, the retrace period for the current when flowing through the further coil being approximately equal to the retrace period of the deflection current when flowing through the deflection coil, the sawtooth networks being connected together such that their diodes are connected in series with the same conductivity direction, the series arrangement of the diodes being connected in parallel across the controlled switch and control means for varying the voltage across all except one of the trace capacitors.

3. A circuit arrangement as claimed in any of Claims 1 or 2, in which the controlled switch is connected in parallel with the series arrangement of the diodes in the sawtooth network through a further diode, the junction of the further diode and the controlled switch being connected through a first winding of a transformer to one of the supply terminals whilst a second winding of the transformer is connected through an additional diode to the sawtooth networks, the conducting periods of the controlled switch being controllable.

4. A circuit arrangement as claimed in Claim 3, having means for deriving a voltage proportional to the voltage present during the retrace period across the series arrangement of the diodes of the sawtooth networks for controlling the conducting periods of the controlled switch.

5. A circuit arrangement as claimed in Claim 2, in which in operation the voltage present during the retrace period across the first and second diodes is substantially constant, the primary winding of an EHT transformer being connected across said diodes.

6. A circuit arrangement as claimed in Claim 2, provided with first control means for controlling the voltage across one of said trace capacitors and second control means element for controlling the voltage across one of the other trace capacitors in response to variations in voltage across two of said trace capacitors.

7. A circuit arrangement as claimed in any of the preceding Claims, in which the trace capacitor for one sawtooth is formed by a plurality of capacitors one of which also constitutes the trace capacitor for another sawtooth network.

8. A circuit arrangement as claimed in Claim 7, in which the coils of two of the sawtooth networks are each substantially identical line deflection coils.



18  
6  
C', are too large to have an essential influence). Capacitors  $C_r$  and  $C'_r$  thus constitute a capacitor potential divider so that the above-described circuit may be replaced in known manner by a circuit having an inductive potential divider. This is shown in Figure 7. A capacitor  $C_4$  is arranged between point A and ground and a capacitor  $C_5$  is arranged between a tap on the winding  $L_1$  and the junction of diodes D and D', the capacitors  $C_r$  and  $C'_r$  being emitted from the circuit. The capacitances of capacitors  $C_4$  and  $C_5$  and the position of the tap can be determined in a simple manner with reference to capacitor  $C_p$  and the previously required capacitances of capacitors  $C_r$  and  $C'_r$ . It may be noted that capacitors  $C_4$  and  $C_5$  actually take over the task of the retrace capacitors of the two networks.

20 In the embodiment of Figure 7 the series arrangement of  $L_r$ ,  $C_r$  is not connected to the junction of elements  $C'_r$  and  $L'$  but to a tap on coil  $L'$  for the following reason. In the middle of the field trace period the East-West modulation is deepest. When in addition, as described above, the S correction is more modulated than the deflection current, it is possible without this step for the current through diode D' to become negative, i.e. diode D' would stop conducting. When this step is used, a current flows through this diode which is the sum of the current in the original embodiment and of a current proportional to current  $i$ , and has therefore a greater intensity. The position of the tap may be chosen to be such that it is ensured that diode D' continues to conduct under all circumstances during the first half of the line trace time. Such a step is also possible for the embodiments of Figures 4b and 6 in which the retrace capacitors can be formed as in Figure 7 or in another manner (for example by means of a capacitor connected in parallel with coil  $L_r$  and one between the tap of coil  $L'$  and ground).

#### WHAT WE CLAIM IS:—

1. A circuit arrangement for generating a line frequency sawtooth deflection current having a trace period and a retrace period through a deflection coil, said arrangement including a first sawtooth network comprising a first diode, said deflection coil, a trace capacitor and a retrace capacitor, a second sawtooth network comprising a second diode, a second coil, a second trace capacitor and a second retrace capacitor, the retrace period for the current when flowing through the second coil being approximately equal to the retrace period for the deflection current, the arrangement also including supply terminals for receiving a supply voltage from a source and a controlled switch which is non-conducting during the retrace period, said sawtooth networks being connected together such that

the first and second diodes are connected in series with the same conductivity direction, the series arrangement of the diodes being connected in parallel across the controlled switch, and control means for varying the voltage across one of the trace capacitors.

2. A circuit arrangement as claimed in Claim 1, including a further sawtooth network having a further diode, a further coil, a further trace capacitor and a further retrace capacitor, the retrace period for the current when flowing through the further coil being approximately equal to the retrace period of the deflection current when flowing through the deflection coil, the sawtooth networks being connected together such that their diodes are connected in series with the same conductivity direction, the series arrangement of the diodes being connected in parallel across the controlled switch and control means for varying the voltage across all except one of the trace capacitors.

3. A circuit arrangement as claimed in any of Claims 1 or 2, in which the controlled switch is connected in parallel with the series arrangement of the diodes in the sawtooth network through a further diode, the junction of the further diode and the controlled switch being connected through a first winding of a transformer to one of the supply terminals whilst a second winding of the transformer is connected through an additional diode to the sawtooth networks, the conducting periods of the controlled switch being controllable.

4. A circuit arrangement as claimed in Claim 3, having means for deriving a voltage proportional to the voltage present during the retrace period across the series arrangement of the diodes of the sawtooth networks for controlling the conducting periods of the controlled switch.

5. A circuit arrangement as claimed in Claim 2, in which in operation the voltage present during the retrace period across the first and second diodes is substantially constant, the primary winding of an EHT transformer being connected across said diodes.

6. A circuit arrangement as claimed in Claim 2, provided with first control means for controlling the voltage across one of said trace capacitors and second control means element for controlling the voltage across one of the other trace capacitors in response to variations in voltage across two of said trace capacitors.

7. A circuit arrangement as claimed in any of the preceding Claims, in which the trace capacitor for one sawtooth is formed by a plurality of capacitors one of which also constitutes the trace capacitor for another sawtooth network.

8. A circuit arrangement as claimed in Claim 7, in which the coils of two of the sawtooth networks are each substantially identical line deflection coils.

19

7

1,459,922

7

5 9. A circuit arrangement as claimed in any of Claims 1 or 2, in which the control means for varying the voltage across a trace capacitor is a stabilizing circuit for stabilizing the voltage present during the retrace period across the diodes of the further sawtooth networks.

10 10. A circuit arrangement for generating a line frequency sawtooth deflection current through a deflection coil, substantially as herein described with reference to the accompanying drawings.

15 11. Television display apparatus including a circuit arrangement as claimed in any of the preceding Claims and a field deflection current generator, in which the control means is a modulation source connected to the field deflection current generator.

20 12. Television display apparatus as claimed in Claim 11, in which the voltage across a trace capacitor is varied by a field frequency parabolic component.

25 13. Television display apparatus as claimed in Claim 11, in which the voltage across a trace capacitor is varied by a field frequency sawtooth-shaped component.

14. Television display apparatus substantially as herein described with reference to the accompanying drawings.

C. A. CLARK,  
Chartered Patent Agent,  
Century House,  
Shaftesbury Avenue,  
London, W.C.2.  
Agent for the Applicants.

Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1976.  
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.



\* C L M S \*