CLAIMS

1. A semiconductor structure, comprising:

a substrate, on which a stacked structure is provided, wherein

the stacked structure comprises a plurality of memory cell groups arranged in a first direction, each of the memory cell groups comprising multiple layers of memory cells arranged in a second direction, and the stacked structure further comprises a plurality of horizontal signal lines arranged in the second direction, each of the horizontal signal lines being in contact with one layer of the memory cells; and

a plurality of leading wire posts arranged in the first direction, wherein the plurality of leading wire posts and the plurality of horizontal signal lines are arranged along a third direction, and the leading wire posts are connected to the horizontal signal lines.

2. The semiconductor structure according to claim 1, wherein each horizontal signal line is at least connected to one of the leading wire posts, and wherein the plurality of horizontal signal lines are connected to the plurality of leading wire posts in one-to-one correspondence.

3. The semiconductor structure according to claim 1, wherein the leading wire posts connected to different horizontal signal lines are different in length in the second direction, and bottoms of the leading wire posts are contacted with the horizontal signal lines.

4. The semiconductor structure according to claim 1, wherein adjacent leading wire posts are arranged at an equal spacing in the first direction; or,

a spacing between the adjacent leading wire posts is in proportion to an area of a directly facing region between the adjacent leading wire posts.

5. The semiconductor structure according to claim 1, wherein the stacked structure further comprises: multiple etching barrier layers arranged in the second direction, each etching barrier layer being contacted with a bottom surface of at least one of the leading wire posts; or

wherein the stacked structure further comprises: a dielectric layer, at least located on a side wall of a leading wire post facing a horizontal signal line, a lower surface of the dielectric layer being higher than the horizontal signal line connected to the leading wire post.

6. The semiconductor structure according to claim 1, wherein each memory cell comprises a channel region and source/drain doped regions arranged in the third direction, the source/drain doped regions being located on two sides of the channel region.

7. The semiconductor structure according to claim 6, wherein the horizontal signal line is a bit line, the bit line being contacted with the source/drain doped regions.

8. The semiconductor structure according to claim 7, wherein the leading wire post and the memory cell are respectively located on two opposite sides of the horizontal signal line arranged in the third direction.

9. The semiconductor structure according to claim 8, wherein a width of the leading wire post in the first direction is greater than or equal to that of the memory cell group; and/or

the width of the leading wire post in the first direction is greater than or equal to a spacing between adjacent memory cell groups; and/or

the width of the leading wire post in the first direction is greater than that of the leading wire post in the third direction; or

wherein the leading wire posts and the memory cell groups are directly opposite in the third direction; or the leading wire posts and the memory cell groups are arranged alternatively in the first direction.

10. The semiconductor structure according to claim 7, wherein the leading wire post and the memory cell are located on a same side of the horizontal signal line, and a width of the leading wire post in the third direction is greater than that of the leading wire post in the first direction.

11. The semiconductor structure according to claim 7, wherein horizontal signal lines of two adjacent stacked structures are arranged opposite, a leading wire post is located between horizontal signal lines of the adjacent stacked structures, and horizontal signal lines of the same layers of the adjacent stacked structures are electrically connected through at least one of the leading wire posts.

12. The semiconductor structure according to claim 6, wherein the horizontal signal line is a word line, the word line being contacted with the channel region, and wherein

adjacent leading wire posts are located on different sides of the horizontal signal line;

or

all the leading wire posts are located on the same side of the horizontal signal line.

13. A semiconductor structure, comprising:

a substrate, on which a stacked structure is provided, wherein

the stacked structure comprises a plurality of memory cell groups arranged in a first direction, each of the memory cell groups comprising multiple layers of memory cells arranged in a second direction, and the stacked structure further comprises a plurality of horizontal signal lines arranged in the second direction, each of the horizontal signal lines being in contact with one layer of the memory cells; and

a plurality of leading wire posts arranged in the first direction and extending along the second direction, wherein orthographic projections of the plurality of leading wire posts on a surface of the substrate and orthographic projections of the horizontal signal lines on the surface of the substrate are at least partially overlapped, and the leading wire posts are connected to the horizontal signal lines.

14. The semiconductor structure according to claim 13, wherein at least one of the leading wire posts penetrates through at least one of the horizontal signal lines.

15. The semiconductor structure according to claim 13, wherein each horizontal signal line comprises a contact region and an exposed region arranged in the third direction, a leading wire post is contacted with the contact region, and the third direction is perpendicular to the second direction and parallel to the surface of the substrate, and

wherein the horizontal signal line has two opposite sides arranged in the third direction, the exposed region is located on one side of the two opposite sides, the contact region is located on the other side of the two opposite sides, and the leading wire post is protruded relative to the contact region.

16. The structure according to claim 13, wherein each memory cell comprises a channel region and source/drain doped regions arranged in a third direction, the source/drain doped regions being located on two sides of the channel region.

17. The semiconductor structure according to claim 13, wherein the horizontal signal line has

two opposite sides arranged in a third direction, each layer of memory cells in the memory cell group comprises two memory cells, and the two memory cells are respectively located in two opposite sides of the horizontal signal line arranged in the third direction.

18. A method for manufacturing a semiconductor structure, comprising:

providing a substrate;

forming a stacked structure on the substrate, wherein the stacked structure comprises a plurality of memory cell groups arranged in a first direction, each of the memory cell groups comprising multiple layers of memory cells arranged in a second direction, and further comprises a plurality of horizontal signal lines arranged in the second direction, each of the horizontal signal lines being in contact with one layer of the memory cells; and

forming a plurality of leading wire posts arranged in the first direction, wherein the plurality of leading wire posts and the plurality of horizontal signal lines are arranged along a third direction, and the leading wire posts are connected to the horizontal signal lines.

19. A method for manufacturing a semiconductor structure, comprising:

providing a substrate;

forming a stacked structure on the substrate, wherein the stacked structure comprises a plurality of memory cell groups arranged in a first direction, each of the memory cell groups comprising multiple layers of memory cells arranged in a second direction, and further comprises a plurality of horizontal signal lines arranged in the second direction, each of the horizontal signal lines being in contact with one layer of the memory cells; and

forming a plurality of leading wire posts arranged in the first direction and extending along the second direction, wherein orthographic projections of the plurality of leading wire posts on a surface of the substrate and orthographic projections of the horizontal signal lines on the surface of the substrate are at least partially overlapped, and the leading wire posts are connected to the horizontal signal lines.

20. A memory chip, comprising the semiconductor structure according to any one of claims 1-12 or the semiconductor structure according to any one of claims 13-17.