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ABSTRACT



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Disclosed is a semiconductor integrated circuit device constructed of MOSFETs in which there is attained a harmony between increase in consumption power due to a leakage current and operating speed of the MOSFETs in a suitable manner, and among a plurality of signal paths in the semiconductor integrated circuit device, a path which has a margin in delay is constructed with MOSFETs each with a high threshold voltage, while a path which has no margin in delay is constructed with MOSFETs each with a low threshold voltage which has a large leakage current but a high operating speed, in light of a delay with which a signal is transmitted along a signal path.