CLAIMS

~~**WHAT IS CLAIMED IS:**~~

1. A substrate comprising:

~~———~~a first portion of the substrate including a first plurality of metal layers~~;~~,

~~———~~wherein the first plurality of metal layers includes a first plurality of interconnects located on a first surface of the first portion of the substrate, and

wherein the first plurality of interconnects are part of a metal layer located on the first surface of the first portion of the substrate;

a second portion of the substrate including a second plurality of metal layers,

wherein the second plurality of metal layers includes a second plurality of interconnects located on a second surface of the second portion of the substrate, and

wherein the second plurality of interconnects are part of another metal layer located on the second surface of the second portion of the substrate;

a plurality of insulating layers configured to separate the first plurality of metal layers and the second plurality of metal layers; ~~and~~

a first plurality of posts and a plurality of solder interconnects ~~are~~ coupled together such that (i) the first plurality of posts and the plurality of solder interconnects couple the first portion of the substrate to the second portion of the substrate, and (ii) the first surface of the first portion of the substrate faces the second surface of the second portion of the substrate; and

a mold located between the first portion of the substrate and the second portion of the substrate, wherein the mold is coupled to the first surface of the first portion of the substrate and the second surface of the second portion of the substrate.

2. The substrate of claim 1, further comprising:

~~———~~a first metal layer of the first plurality of metal layers includes a first plurality of traces embedded in the first portion of the substrate; and

~~———~~a second metal layer of the second plurality of metal layers includes a second plurality of traces embedded in the second portion of the substrate.

3. The substrate of claim 2:

~~———~~wherein the first metal layer is a top layer of the substrate, and the first plurality of traces are configured to couple to a surface mount circuit component; and

———wherein the second metal layer is a bottom layer of the substrate and the second plurality of traces are configured to couple to another surface mount circuit component.

4. The substrate of claim 2:

wherein the first plurality of posts are located on an inner metal layer of the substrate; and

wherein the substrate further comprises a second plurality of ~~interconnects~~posts that are located on another inner metal layer of the substrate.

5. The substrate of claim 1, ~~further comprising:~~

~~a gap between~~wherein the first ~~portion of the substrate~~plurality interconnects and the second ~~portion~~plurality of interconnects are encapsulated by the ~~substrate;~~mold, and

wherein the mold includes a ~~mold configured to fill the gap~~non-conductive paste and/or a non-conductive film.

6. The substrate of claim 1,

wherein the plurality of solder interconnects are located inside of the substrate, and

wherein the plurality of solder interconnects are located between the first portion of the substrate and the second portion of the substrate.

~~6. The substrate of claim 4, wherein the plurality of interconnects comprises a plurality of solder interconnects.~~

7. The substrate of claim 6, wherein the plurality of solder interconnects are at least partially surrounded by solder resist, wherein the solder resist is located inside of the substrate.

8. The substrate of claim ~~7, further comprising:~~1,

~~a gap between~~wherein the first plurality of ~~posts;~~metal layers from the first portion of the substrate includes three or more metal layers, and

~~a mold configured to fill~~wherein the ~~gap between the first~~second plurality of ~~posts~~metal layers from the second portion of the substrate includes three or more metal layers.

9. The substrate of claim ~~4, wherein the plurality of interconnects comprises~~1, further comprising a second plurality of posts, wherein the first plurality of posts are ~~over the second plurality of posts.~~

~~10. The substrate of claim 9, wherein the first plurality of posts are conductively~~ coupled to the second plurality of posts ~~by a conductive film.~~ through the plurality of solder interconnects.

~~11. The substrate of claim 9, further comprising:~~

~~a gap between the first portion of the substrate and the second portion of the substrate, the gap also between each one of the first plurality of posts and each one of the second plurality of posts; and~~

~~a mold configured to fill the gap.~~

~~12~~10. The substrate of claim 1, wherein the substrate is incorporated into a device selected from a group consisting of a music player, a video player, an entertainment unit, a navigation device, a communications device, a mobile device, a mobile phone, a smartphone, a personal digital assistant, a fixed location terminal, a tablet computer, a computer, a wearable device, a laptop computer, a server, an internet of things (IoT) device, and a device in an automotive vehicle.

~~13~~11. A method of fabricating a substrate, comprising:

~~———~~forming a first portion of the substrate including forming a first plurality of metal layers comprising a metal layer that is located on a first surface of the first portion of the substrate;

~~———~~forming a second portion of the substrate including forming a second plurality of metal layers comprising another metal layer that is located on a second surface of the second portion of the substrate;

forming a plurality of insulating layers configured to separate the first plurality of metal layers and the second plurality of metal layers; ~~and~~

forming a first plurality of posts and a plurality of solder interconnects~~, and~~ ;

coupling the first plurality of posts to the plurality of solder interconnects such that (i) the first portion of the substrate and the second portion of the substrate are coupled together~~.~~, and (ii) the first surface of the first portion of the substrate faces the second surface of the second portion of the substrate, wherein coupling the first plurality of posts to the plurality of solder interconnects forms a gap between the first portion of the substrate and the second portion of the substrate; and

filling the gap with a mold, such that the mold is coupled to the first surface of the first portion of the substrate and the second surface of the second portion of the substrate.

~~14~~12. The method of claim ~~13~~11, further comprising:

~~———~~forming a first plurality of traces embedded in the first portion of the substrate, the first plurality of traces formed in a first metal layer of the first plurality of metal layers; and

~~———~~forming a second plurality of traces embedded in the second portion of the substrate, the second plurality of traces formed in a second metal layer of the second plurality of metal layers.

~~15~~13. The method of claim ~~14~~12:

~~———~~wherein the first metal layer is a top layer of the substrate, and the first plurality of traces are configured to couple to a surface mount circuit component; and

~~———~~wherein the second metal layer is a bottom layer of the substrate and the second plurality of traces are configured to couple to another surface mount circuit component.

~~16~~14. The method of claim ~~13, further comprising:~~

~~forming a gap between the first portion of the substrate and the second portion of the substrate; and~~

~~filling the gap with a mold.~~

~~17. The method of claim 15~~11, wherein the ~~plurality of interconnects include a plurality of solder interconnects.~~mold includes a non-conductive paste and/or a non-conductive film.

~~18~~15. The method of claim ~~17, further comprising surrounding the plurality of interconnects, at least partially, by solder resist.~~

~~19. The method of claim 18~~11, wherein the plurality of solder interconnects are located inside of the substrate.

16. The method of claim 15, wherein the plurality of solder interconnects are at least partially surrounded by solder resist, wherein the solder resist is located inside the substrate.

17. The method of claim 16, wherein coupling the first plurality of posts to the plurality of solder interconnects comprises coupling the first plurality of posts to a second plurality of posts

through the plurality of solder interconnects, wherein the first plurality of posts are located over the second plurality of posts.

~~20~~18. The method of claim ~~19~~11, wherein the first ~~plurality~~portion of ~~posts are conductively coupled to~~the substrate and the second ~~plurality~~portion of ~~posts by a conductive film.~~ the substrate are fabricated using an embedded trace substrate process.

~~21. The method of claim 19, further~~19. A substrate comprising:

~~forming a gap between the~~a first portion of the substrate ~~and the second portion of the substrate, the gap also between each one of~~including a first plurality of metal layers, wherein the first plurality of metal layers includes a first plurality of traces located on a first surface of the first portion of the substrate;

a second portion of the substrate including a second plurality of metal layers, wherein the second plurality of metal layers includes a second plurality of traces located on a second surface of the second portion of the substrate;

a plurality of insulating layers configured to separate the first plurality of metal layers and the second plurality of metal layers;

a first plurality of posts and ~~each one of the~~ a second plurality of posts~~;~~ coupled together through a conductive film such that (i) the first plurality of posts and the second plurality of posts couple the first portion of the substrate to the second portion of the substrate, and (ii) the first surface of the first portion of the substrate faces the second surface of the second portion of the substrate; and

~~filling the gap with a mold.~~a mold located between the first portion of the substrate and the second portion of the substrate, wherein the mold is coupled to the first surface of the first portion of the substrate and the second surface of the second portion of the substrate.

20. The substrate of claim 19,

wherein the first plurality traces and the second plurality of traces are encapsulated by the mold,

wherein the conductive film includes an anisotropic conductive film and/or an adhesive, and

wherein the mold includes a non-conductive paste and/or a non-conductive film.

21. The substrate of claim 19,

wherein the first plurality of metal layers from the first portion of the substrate includes three or more metal layers, and

wherein the second plurality of metal layers from the second portion of the substrate includes three or more metal layers.